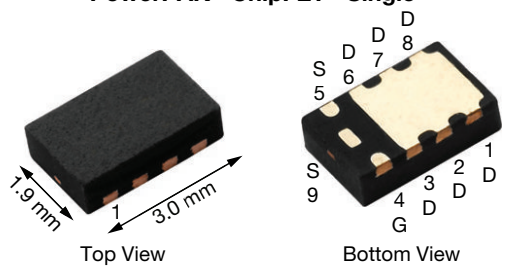
N-Channel 40 V (D-S) MOSFET

PowerPAK® ChipFET® Single



FEATURES

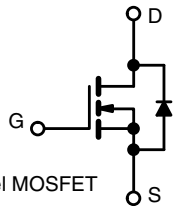
- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Thermally enhanced PowerPAK ChipFET package
  -Compact footprint area - less than 6.09 mm^2
  -Thin 0.8 mm profile
- 56 % lower $R_{DS(ON)}$ than the prior generation
- Material categorization:
  for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00775
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00947
Q_g typ. (nC)	12.6
I_D (A) [a, g]	25
Configuration	Single

APPLICATIONS

- DC/DC converters
- Motor drive control
- Synchronous rectification
- Battery management
- Load switch



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK ChipFET
Lead (Pb)-free and halogen-free	Si5448DU-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	+20 / -16	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	25 [a]	A
	T_C = 70 °C		25 [a]	
	T_A = 25 °C		15.9 [b, c]	
	T_A = 70 °C		12.7 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	100	
Continuous source-drain diode current	T_C = 25 °C	I_S	25 [a]	
	T_A = 25 °C		2.6 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	15	
Single pulse avalanche energy		E_{AS}	11.25	mJ
Maximum power dissipation	T_C = 25 °C	P_D	31	W
	T_C = 70 °C		20	
	T_A = 25 °C		3.1 [b, c]	
	T_A = 70 °C		2 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	34	40	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	4	4	

Notes

a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 90 °C/W.
g. T_C = 25 °C.

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	40	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	21.2	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.1	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.5	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V / -16 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 70 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \leq$ 10 V, V_{GS} = 10 V	20	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	-	0.00646	0.00775	Ω
		V_{GS} = 4.5 V, I_D = 10 A	-	0.00790	0.00947	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 15 A	-	80	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	-	1765	-	pF
Output capacitance	C_{oss}		-	278	-	
Reverse transfer capacitance	C_{rss}		-	45	-	
Total gate charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 15 A	-	26.2	40	nC
		V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 15 A	-	12.6	20	
Gate-source charge	Q_{gs}		-	5.1	-	
Gate-drain charge	Q_{gd}		-	2.5	-	
Gate resistance	R_g	f = 1 MHz	0.3	1.5	3	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1.7 Ω, $I_D \cong$ 12 A, V_{GEN} = 10 V, R_g = 1 Ω	-	10	20	ns
Rise time	t_r		-	35	53	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1.7 Ω, $I_D \cong$ 12 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	15	30	
Rise time	t_r		-	60	90	
Turn-off delay time	$t_{d(off)}$		-	18	36	
Fall time	t_f		-	33	50	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	25	A
Pulse diode forward current	I_{SM}		-	-	100	
Body diode voltage	V_{SD}	I_S = 13 A, V_{GS} = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 13 A, dI/dt = 100 A/µs, T_J = 25 °C	-	33	50	ns
Body diode reverse recovery charge	Q_{rr}		-	30	45	nC
Reverse recovery fall time	t_a		-	18	-	ns
Reverse recovery rise time	t_b		-	15	-	

Notes

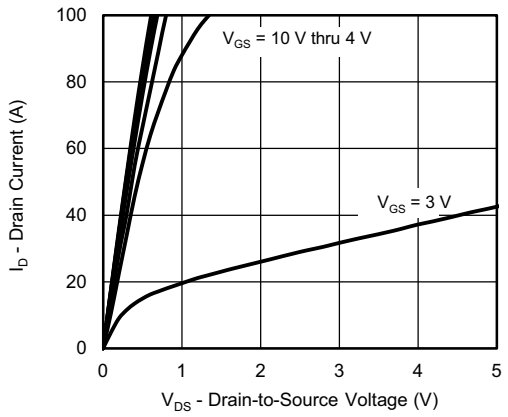
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

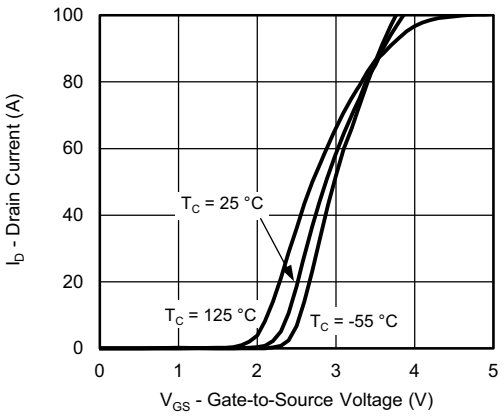
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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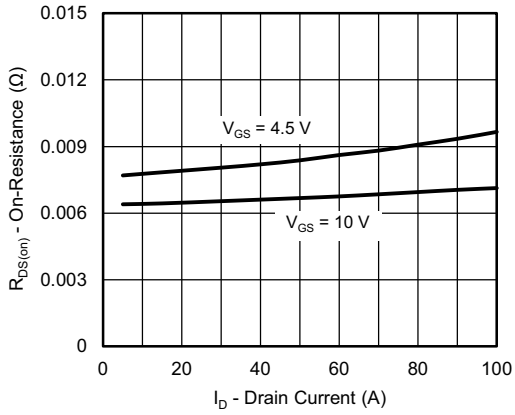
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



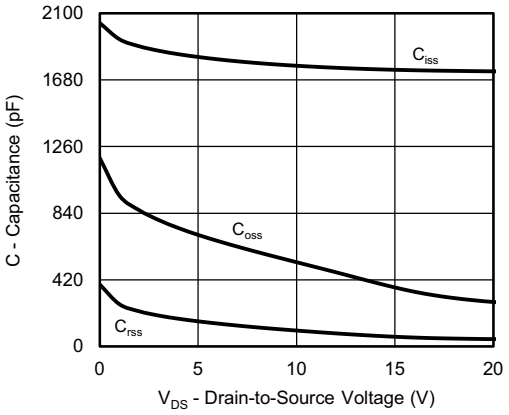
Output Characteristics



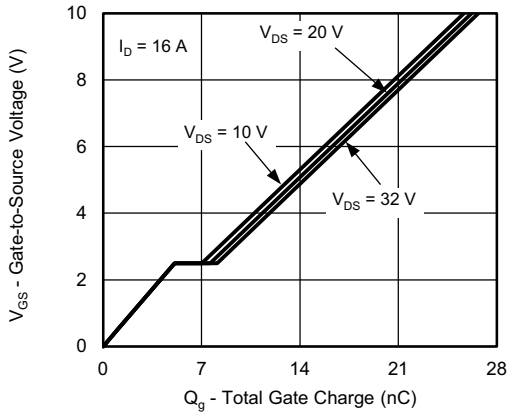
Transfer Characteristics



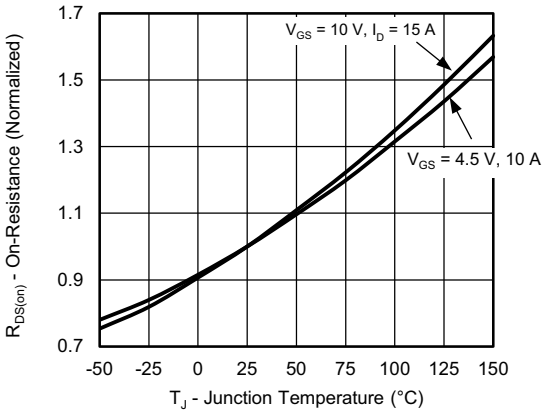
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



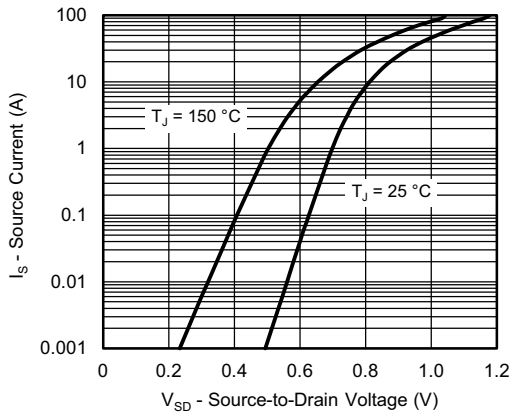
Gate Charge



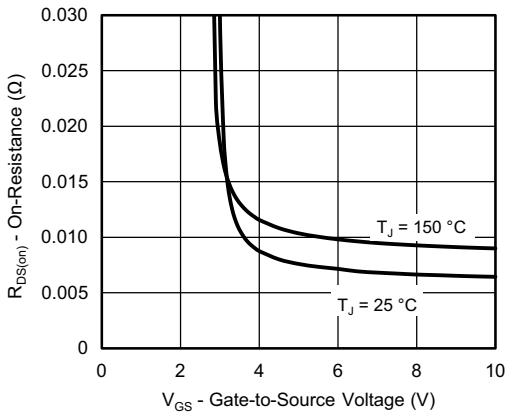
On-Resistance vs. Junction Temperature

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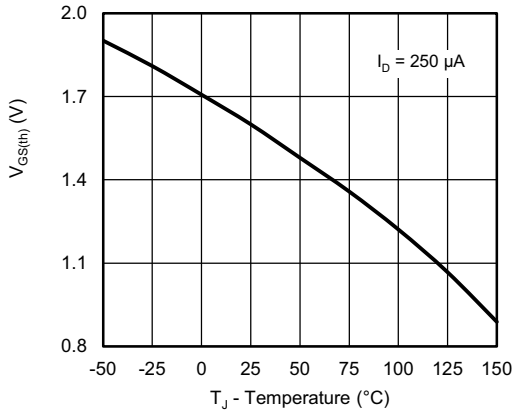
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



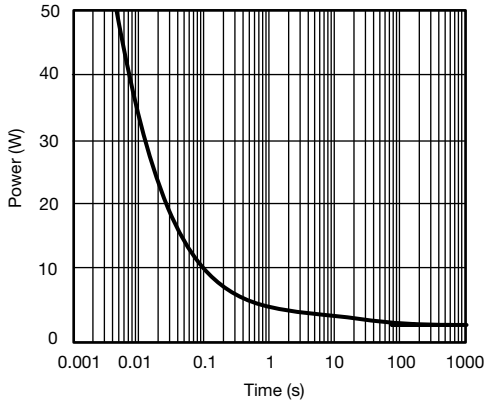
Source-Drain Diode Forward Voltage



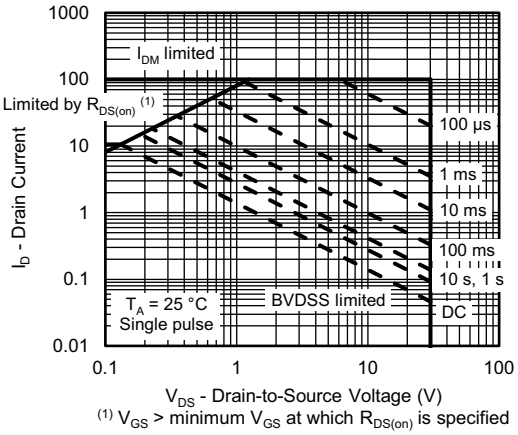
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



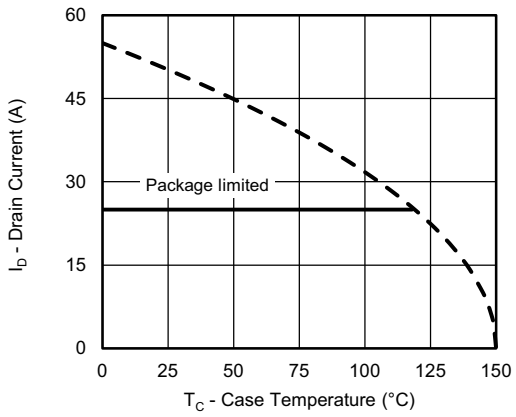
Single Pulse Power, Junction-to-Ambient



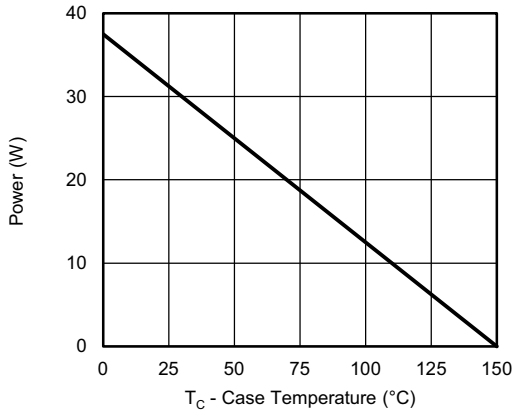
Safe Operating Area, Junction-to-Ambient

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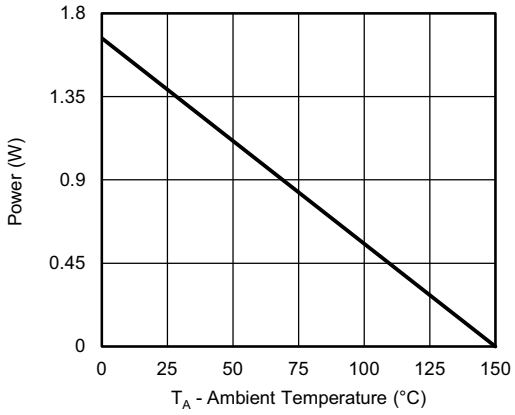
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case



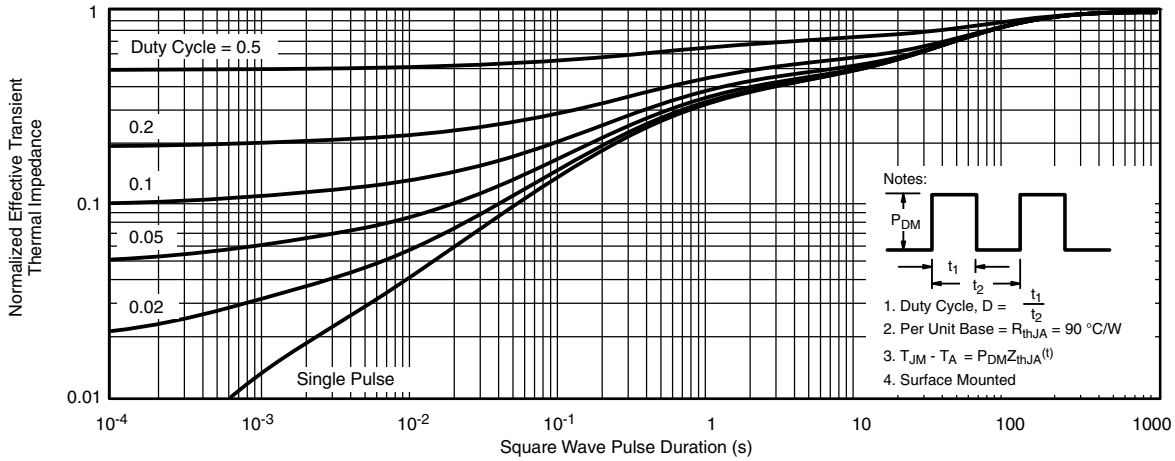
Power, Junction-to-Ambient

Note

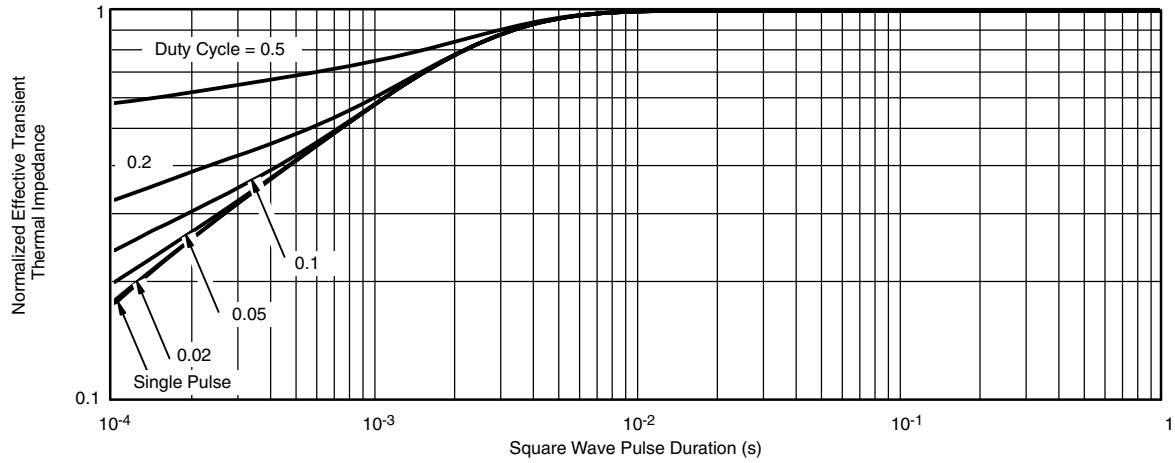
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

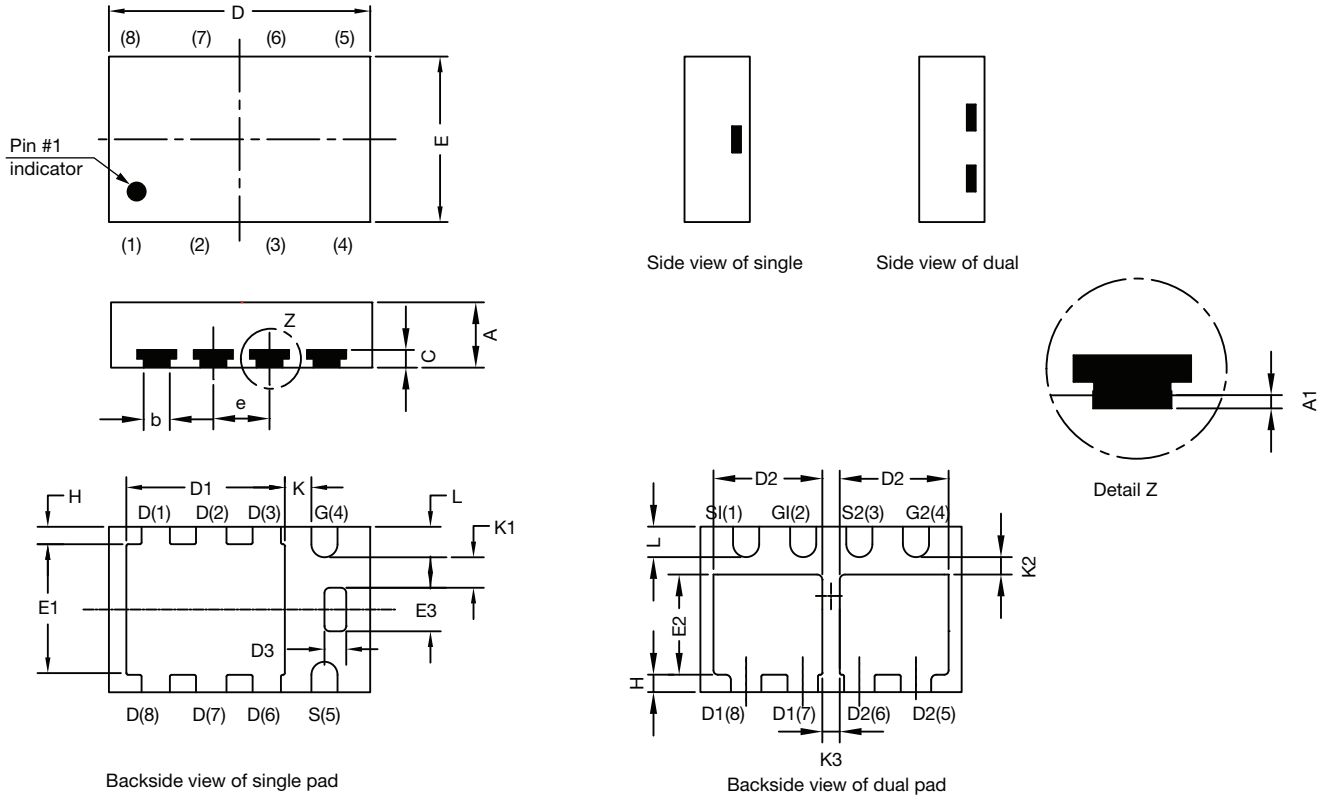


Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® ChipFET® Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14 DWG: 5940						

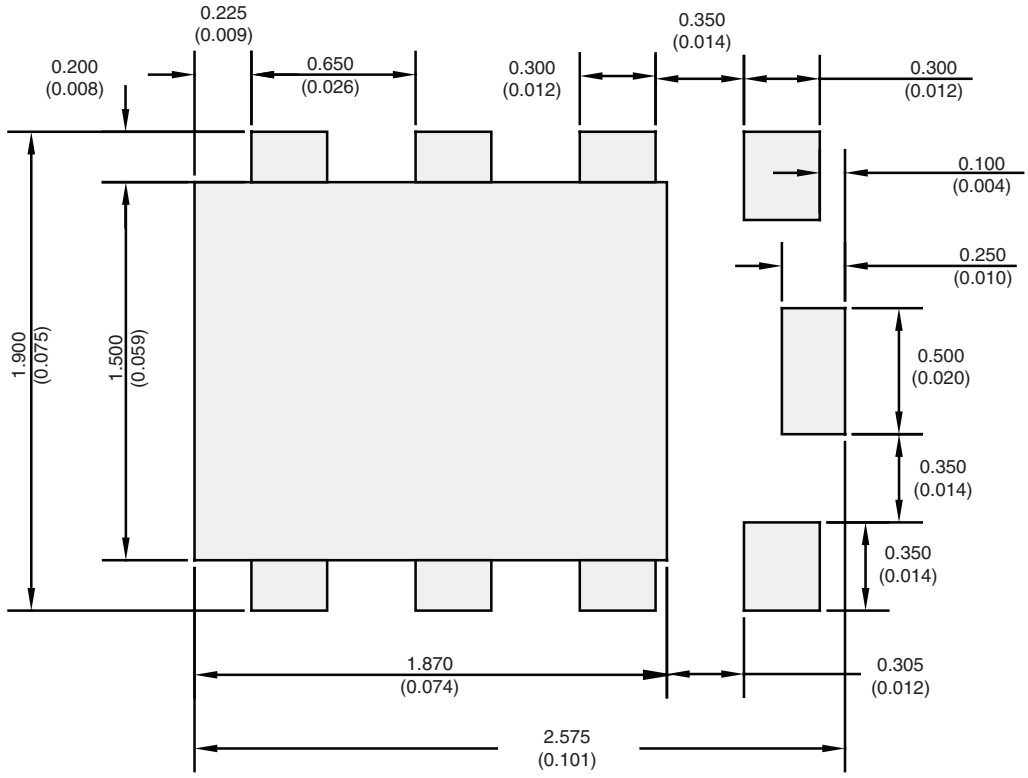
Note

- Millimeters will govern

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RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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