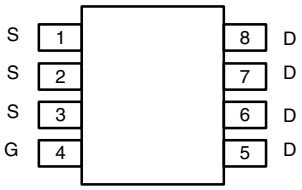
Si4101DY

Vishay Siliconix

P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)[d]	Q_g (Typ.)
- 30	0.0060 at V_{GS} = - 10 V	- 25.7	65 nC
	0.0080 at V_{GS} = - 4.5 V	- 22.3	

SO-8



Top View

Ordering Information:
Si4101DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

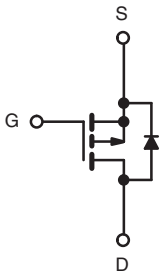
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Adaptor Switch, Load Switch
- Power Management
- Notebook Computers and Portable Battery Packs



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 25.7	A
	T_C = 70 °C		- 20.6	
	T_A = 25 °C		- 18[a, b]	
	T_A = 70 °C		- 14.4[a, b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	- 70	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 5	
	T_A = 25 °C		- 2.4[a, b]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 30	
Single-Pulse Avalanche Energy		E_{AS}	45	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	6	W
	T_C = 70 °C		3.8	
	T_A = 25 °C		2.9[a, b]	
	T_A = 70 °C		1.9[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a, c]	t ≤ 10 s	R_{thJA}	36	43	°C/W
Maximum Junction-to-Foot	Steady State	R_{thJF}	16	21	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. Maximum under steady state conditions is 84 °C/W.
d. Based on T_C = 25 °C.

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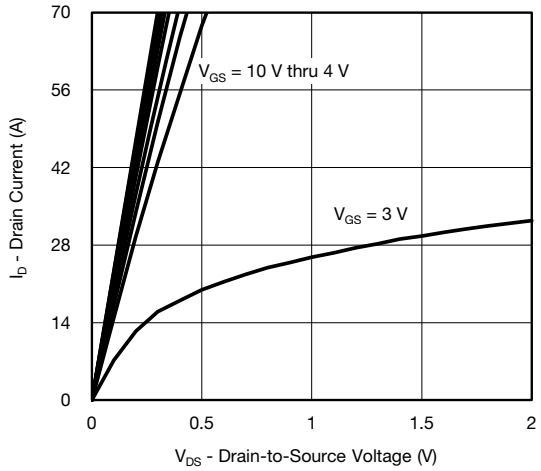
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 2.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ - 10 V, V_{GS} = - 10 V	- 30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 15 A		0.0050	0.0060	Ω
		V_{GS} = - 4.5 V, I_D = - 10 A		0.0066	0.0080	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 15 A		72		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		8190		pF
Output Capacitance	C_{oss}			772		
Reverse Transfer Capacitance	C_{rss}			715		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 18 A		135	203	nC
		V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_D = - 18 A		65	85	
Gate-Source Charge	Q_{gs}			22.5		
Gate-Drain Charge	Q_{gd}			17.6		
Gate Resistance	R_g	f = 1 MHz	0.4	2	4	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		20	30	ns
Rise Time	t_r			9	18	
Turn-Off DelayTime	$t_{d(off)}$			80	120	
Fall Time	t_f			11	20	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω $I_D \cong$ - 10 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		72	108	
Rise Time	t_r			60	90	
Turn-Off DelayTime	$t_{d(off)}$			60	90	
Fall Time	t_f			23	35	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I_S	T_C = 25 °C			- 5	A
Pulse Diode Forward Current	I_{SM}				- 70	
Body Diode Voltage	V_{SD}	I_S = - 3 A, V_{GS} = 0 V		- 0.78	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10 A, dI/dt = 100 A/µs, T_J = 25 °C		29	45	ns
Body Diode Reverse Recovery Charge	Q_{rr}			19	29	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			16		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

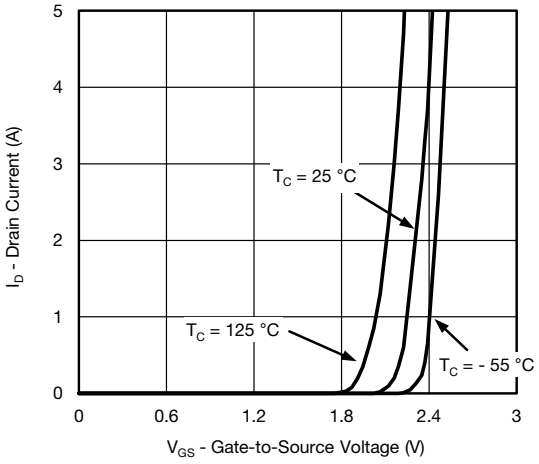
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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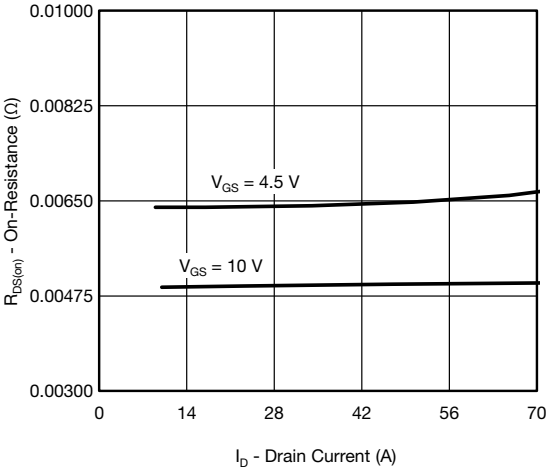
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



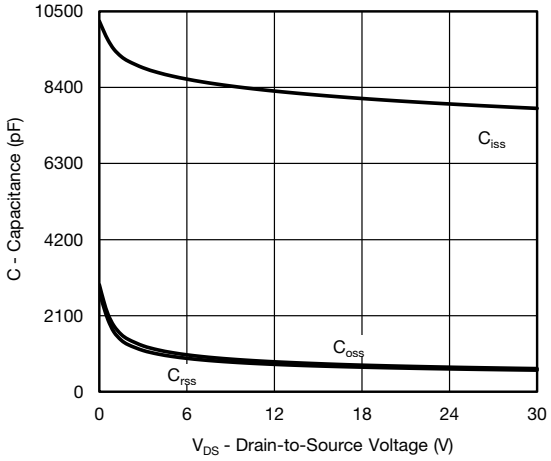
Output Characteristics



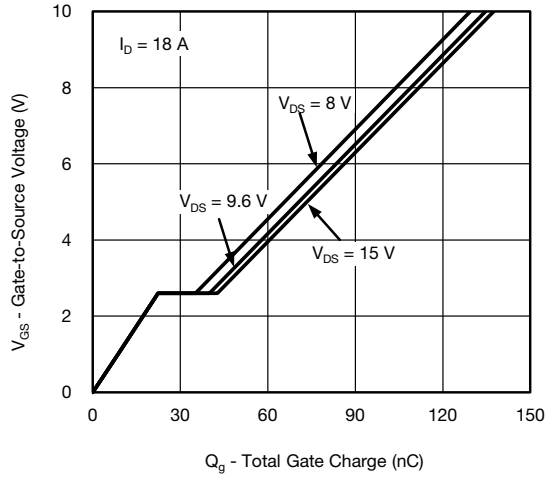
Transfer Characteristics



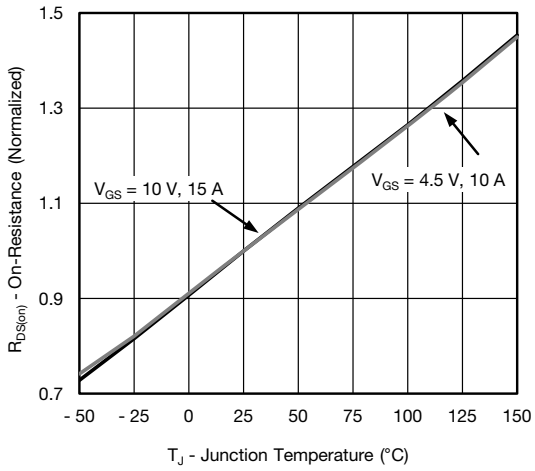
On-Resistance vs. Drain Current



Capacitance



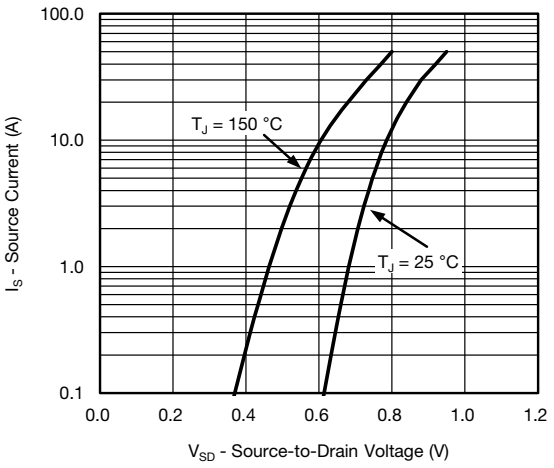
Gate Charge



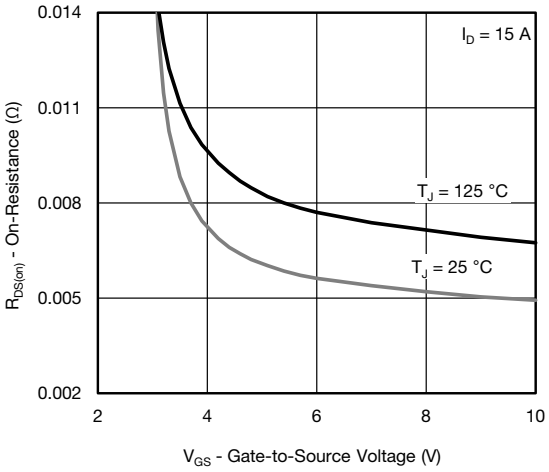
On-Resistance vs. Junction Temperature

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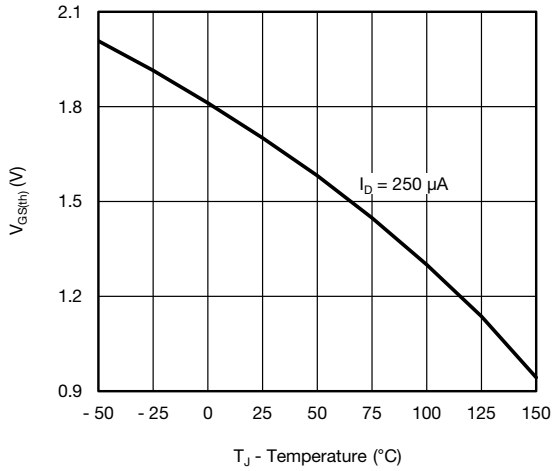
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



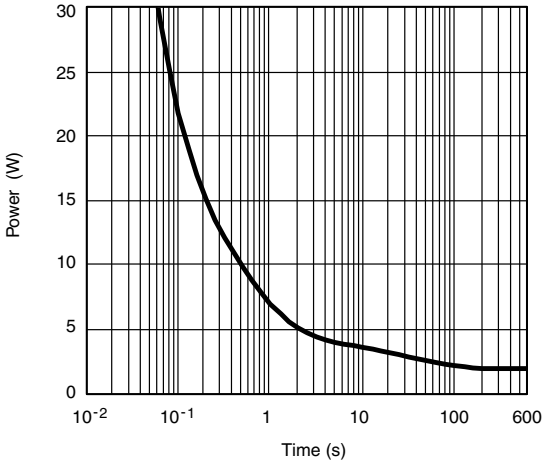
Source-Drain Diode Forward Voltage



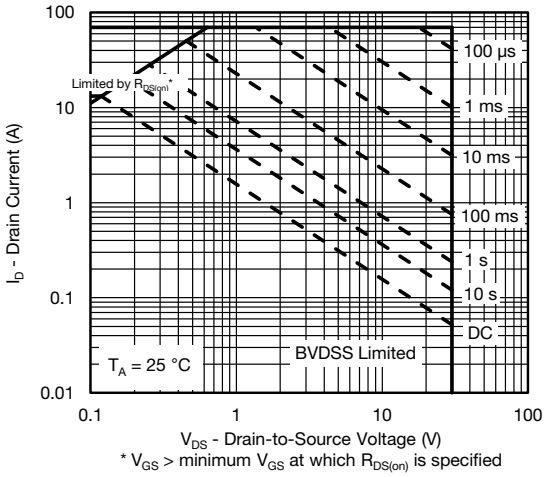
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



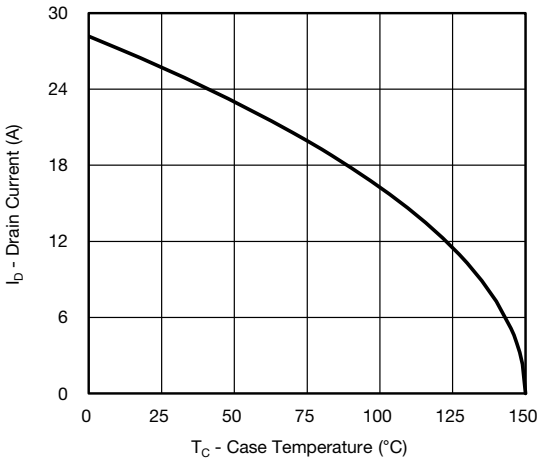
Single Pulse Power, Junction-to-Ambient



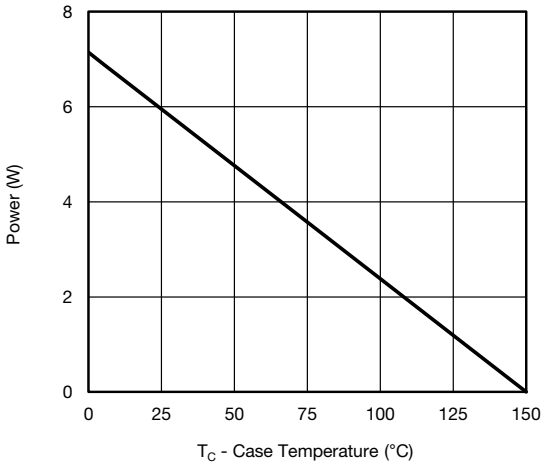
Safe Operating Area

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 62828
S13-0110-Rev. A, 21-Jan-13
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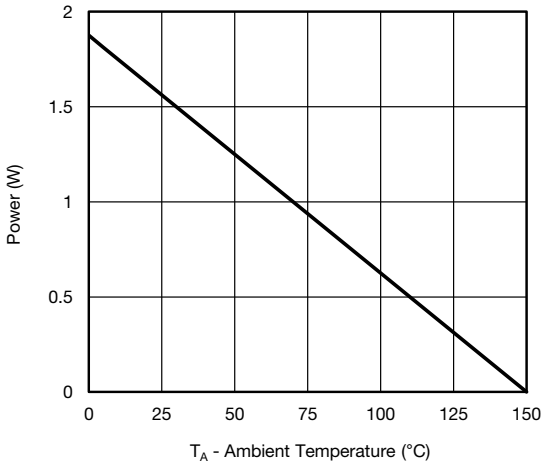
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Derating, Junction-to-Foot

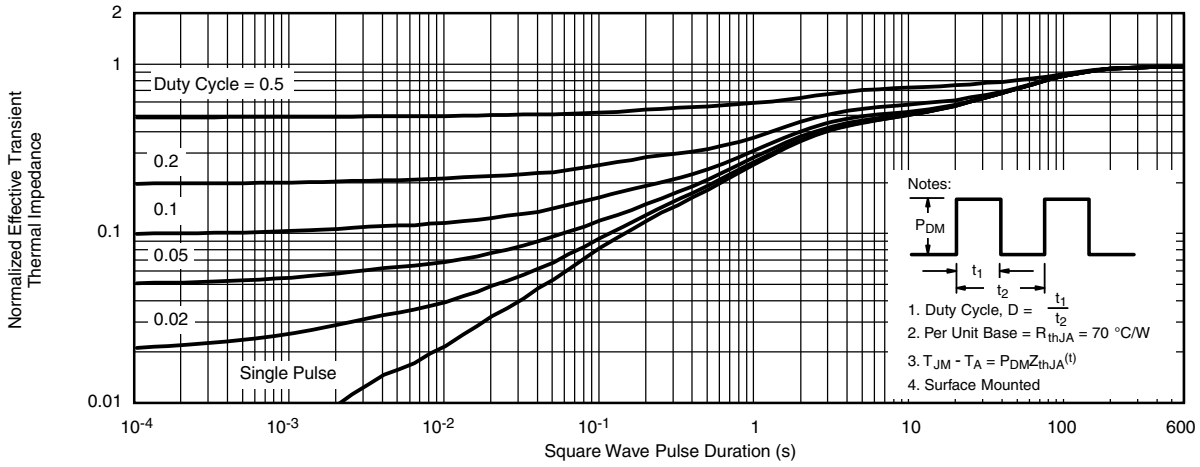


Power Derating, Junction-to-Ambient

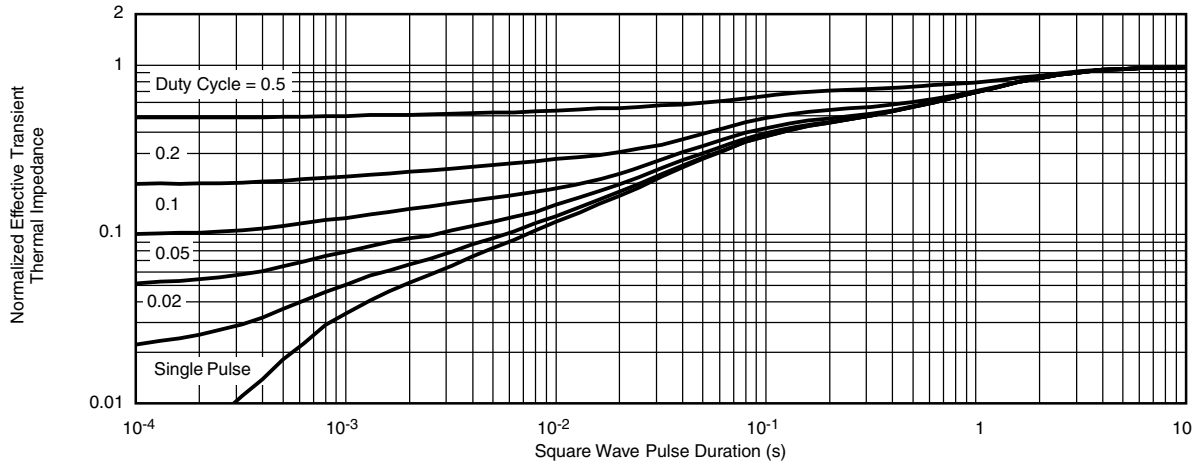
* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

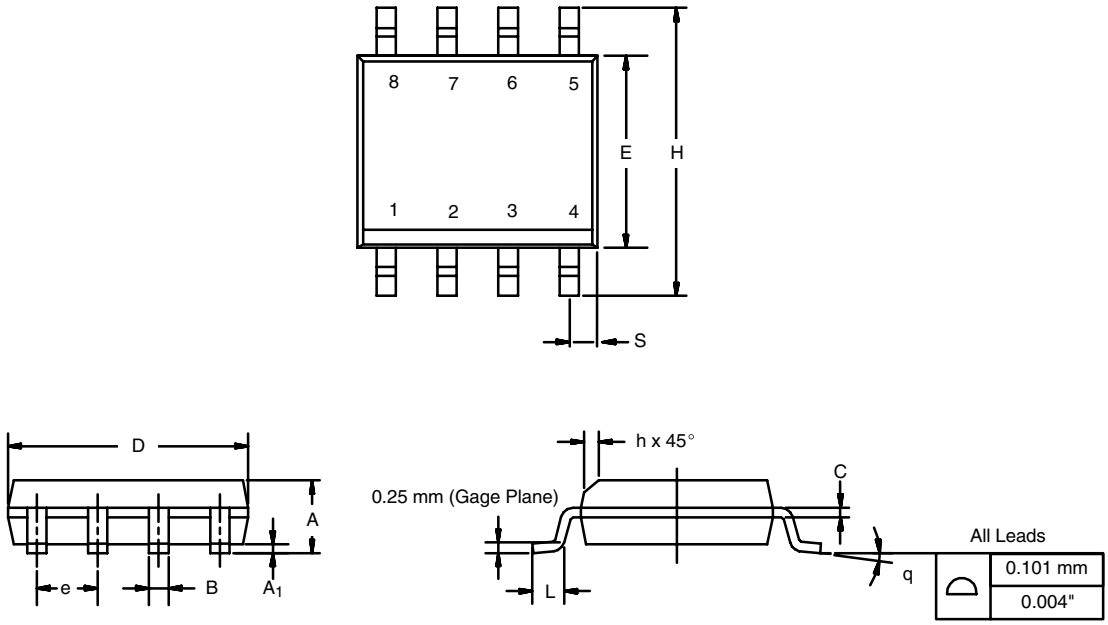


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62828.

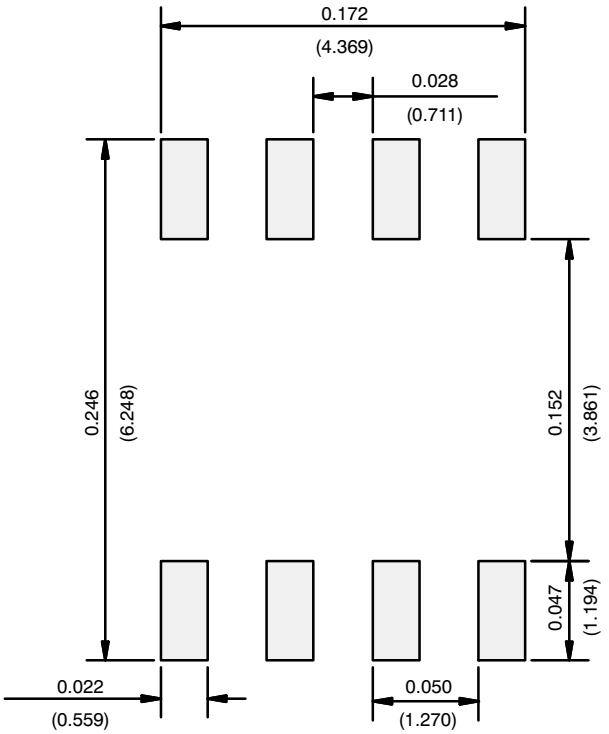
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SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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