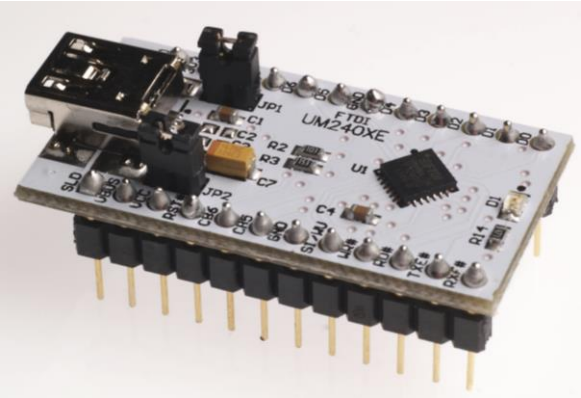
Future Technology Devices International

Datasheet

UMFT240XE USB to 8-bit 245 FIFO Development Module



UMFT240XE is a USB to 8-bit 245 FIFO DIP module with a 0.6" row pitch.

1 Introduction

The UMFT240XE is a development module for FTDI's FT240XQ, one of the devices from FTDI's range of USB to serial data interface integrated circuit devices. FT240X is a USB to 245 FIFO interface with a battery charging feature, which can allow batteries to be charged with a higher current from a dedicated charger port (without the FT240X being enumerated). In addition, asynchronous and synchronous bit bang interface modes are available. The internally generated clock (6MHz, 12MHz, 24MHz and 48MHz) can be brought out of the on one of the CBUS pin to be used to drive a microprocessor or external logic.

The UMFT240XE is a module which is designed to plug into a standard 0.6" wide 24 pin DIP socket. All components used, including the FT240XQ are Pb-free (RoHS compliant).

1.1 Features

The UMFT240XE is fitted with a FT240XQ, all the features of the FT240X can be utilized with the UMFT240XE. For a full list of the FT240X's features please see the FT240X datasheet which can be found by clicking here.

In addition to the features listed in the FT240X datasheet, the UMFT240XE has the following features:

Small PCB assembly module designed to fit a standard 15.24mm (0.6") wide 24 pin DIP socket. Pins are on a 2.54mm (0.1") pitch.

On board USB 'mini-B' socket allows module to be connected to a PC via a standard A to mini-B USB cable.

Functionally configurable using jumpers. The default jumper setup enables the module to function without peripheral wires or application board. Other configurations enable external power supply options and variation of logic reference levels.

2 Driver Support

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for:

- Windows 10 32, 64-bit
- Windows 8 / 8.1 32, 64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows XP Embedded
- Server XP / 2003 /2008 / 2016
- Windows CE 4.2-5.2, 6.0/7.0, 2013
- Mac OS-X
- Linux 3.2 and greater
- Android

Royalty-Free D2XX Direct Drivers (USB Drivers + DLL S/W Interface):

- Windows 10 32, 64-bit
- Windows 8 / 8.1 32, 64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows XP Embedded
- Server XP / 2003 /2008 / 2016
- Windows CE 4.2-5.2, 6.0/7.0, 2013
- Mac OS-X
- Linux 3.2 and greater
- Android

The drivers listed above are all available to download for free from www.ftdichip.com. Various 3rd Party Drivers are also available for various other operating systems - visit www.ftdichip.com for details.

3 Ordering Information

Module Code	Utilised IC Code	TID	Description
UMFT201XE-01	FT201XQ	40001460	USB to I^2C evaluation module. 0.6” row pitch, standard DIP headers.
UMFT221XE-01	FT221XQ	40001462	USB to 8-bit SPI/FT1248 evaluation module. 0.6” row pitch, standard DIP headers.
UMFT231XE-01	FT231XQ	40001464	USB to Full-Handshake UART evaluation module. 0.6” row pitch, standard DIP headers.
UMFT240XE-01	FT240XQ	40001466	USB to 8-bit 245 FIFO evaluation module. 0.6” row pitch, standard DIP headers.

TID is the test identification code for the IC. Note that this TID is for revision D silicon.

Table of Contents

4 UMFT240XE Signals and Configurations

4.1 UMFT240XE Pin Out

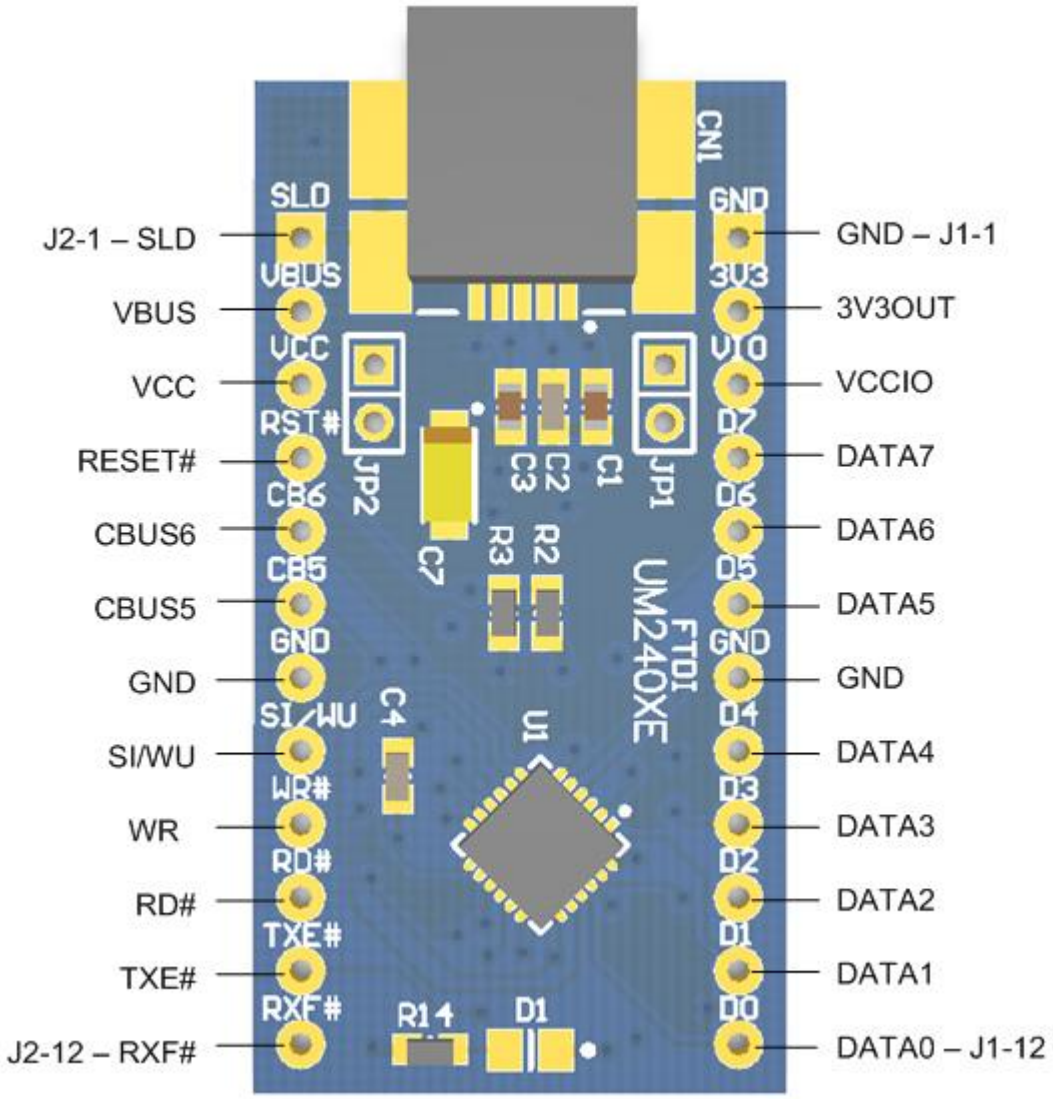


Figure 4.1 – Module Pin Out

Figure 4.1 illustrates the signals available on the DIP pins.

4.2 Signal Descriptions

Pin No.	Name	Type	Description
J1-1, J1-7, J2-5	GND	PWR	Module Ground Supply Pins
J1-2	3V3OUT	Power Input/ Output	3.3V output from integrated LDO regulator. This pin is decoupled with a 100nF capacitor to ground on the PCB module. The prime purpose of this pin is to provide the 3.3V supply that can be used internally. For power supply configuration details see section 5.
J1-3	VCCIO	Power Input	+1.8V to +3.3V supply to the UART Interface and CBUS I/O pins. For power supply configuration details see section 5.
J1-4	DATA7	I/O	245 FIFO Bi-Directional data bit 7.
J1-5	DATA6	I/O	245 FIFO Bi-Directional data bit 6.
J1-6	DATA5	I/O	245 FIFO Bi-Directional data bit 5.
J1-8	DATA4	I/O	245 FIFO Bi-Directional data bit 4.
J1-9	DATA3	I/O	245 FIFO Bi-Directional data bit 3.
J1-10	DATA2	I/O	245 FIFO Bi-Directional data bit 2.
J1-11	DATA1	I/O	245 FIFO Bi-Directional data bit 1.
J1-12	DATA0	I/O	245 FIFO Bi-Directional data bit 0.
J2-1	SLD	GND	USB Cable Shield. Connected to GND via a 0ohm resistor.
J2-2	VBUS	Power Output	5V Power output from the USB bus. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply and applied to the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design. Currents up to 1A can be sourced from a dedicated charger and applied to the USB bus.
J2-3	VCC	Power Input	5V power input for FT240X. For power supply configuration details see section 5.
J2-4	RESET#	Input	FT231X active low reset line. Configured with an on board pull-up and recommended filter capacitor. When no power is applied to the USB bus reset, will be held low, this prevents current from flowing to the host or hub when in self-powered mode.
J2-5	CBUS6	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal MTP ROM. Factory Default pin Function is Keep_Awake. See CBUS Signal Options, Table 4.2.
J2-6	CBUS5	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal MTP ROM. Factory Default pin Function is VBUS_Sense. See CBUS Signal Options, Table 4.2.
J2-8	SI/WU	Output	Send Immediate/Wake Up
J2-9	WR	Input	245 FIFO Write status line
J2-10	RD#	Input	245 FIFO Read status line
J2-11	TXE#	Output	245 FIFO Transmit control line
J2-12	RXF#	Output	245 FIFO Receive control line

Table 4.1 – Module Pin Out Description

4.3 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. These options are all configured in the internal MTP ROM using the utility software FT_PROG, which can be downloaded from the www.ftdichip.com. The default configuration is described in Section 9.

CBUS Signal Option	Available On CBUS Pin	Description
Tristate	CBUS5, CBUS6	IO Pad is tri-stated
DRIVE_1	CBUS5, CBUS6	Output a constant 1
DRIVE_0	CBUS5, CBUS6	Output a constant 0
PWREN#	CBUS5, CBUS6	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. **NOTE:** This function is driven by an open-drain to ground with no internal pull-up, this is specially designed to aid battery charging applications. UMFT240XE connects an on-board 47K pull-up on each CBUS and DBUS signal.
SLEEP#	CBUS5, CBUS6	Goes low during USB suspend mode. Typically used to power down an external logic to RS232 level converter IC in USB to RS232 converter designs. Deactivate SLEEP# option for when connected to a dedicated charger port, this can be selected when configuring the MTP ROM. When this option is enabled SLEEP# is driven high when FT240X is connected to a Dedicated Charger Port.
CLK24MHz	CBUS5, CBUS6	24 MHz Clock output.**
CLK12MHz	CBUS5, CBUS6	12 MHz Clock output.**
CLK6MHz	CBUS5, CBUS6	6 MHz Clock output.**
BCD_Charger	CBUS5, CBUS6	Battery Charge Detect indicates when the device is connected to a dedicated battery charger host. Active high output. NOTE: Requires a 10K pull-down to remove power up toggling.
BCD_Charger#	CBUS5, CBUS6	Active low BCD Charger, driven by an open drain to ground with no internal pull-up (4.7K on board pull-up present).
BitBang_WR#	CBUS5, CBUS6	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBang_RD#	CBUS5, CBUS6	Synchronous and asynchronous bit bang mode RD# strobe output.
VBUS Sense	CBUS5, CBUS6	Input to detect when VBUS is present.
Time Stamp	CBUS5, CBUS6	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS5, CBUS6	Active Low input, prevents the chip from going into suspend.

Table 4.2 – CBUS Signal Options

**When in USB suspend mode the outputs clocks are also suspended.

5 Module Configurations

5.1 Jumper Configuration Options

Jumper No.	Setting	Status	Description
JP1	Shorted	Default	Connects internal 3.3V regulator to VCCIO. This restricts signal drive to only 3.3V level signals.
JP1	Opened	Non-Default	Disconnects internal 3.3V regulator connection to VCCIO. This mode allows for the supply of 1.8V-3.3V power from an external power supply, thus allows the processing of signals with logic levels between 1.8V and 3.3V. VCCIO can be adjusted to match the interface requirements of external circuitry.

Table 5.1 – Jumper JP1 Pin Description

Jumper No.	Setting	Status	Description
JP2	Shorted	Default	Connects VBUS to VCC. This mode is known as "USB-Powered" mode.
JP2	Opened	Non-Default	Disconnects VBUS to VCC. This allows the supply of power from an external power supply. This mode is known as "Self-Powered" mode.

Table 5.2 – Jumper JP2 Pin Description

Note: There should never be more than one power output supplied to the same net. If JP2 is fitted when an external power supply is applied a direct short between two power supplies will be formed, this can result in damage to the UMFT240XE module and the target circuit.

5.2 BUS Powered Configuration

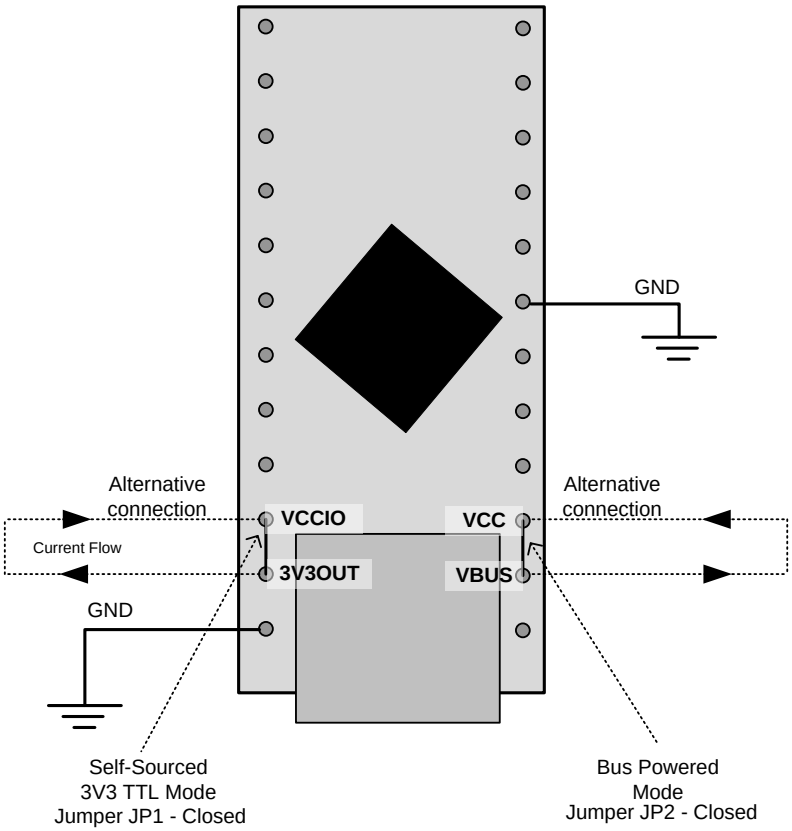


Figure 5.1 – Bus Powered Configuration

A bus powered configuration draws its power from the USB host/hub. The UMFT240XE is configured by default to be in bus powered mode.

Figure 5.1illustrates the UMFT240XE module in a typical USB bus powered design configuration. By default 3V3OUT is connected to VCCIO, and VBUS is connected to VCC.

For a bus power configuration power is supplied from the USB VBUS:

+5V VBUS power is sourced from the USB bus and is connected to the FT240X power input (VCC)

+3.3V power is sourced from the FT240X's voltage regulator output and is connected to the FT240X IO port's power input (VCCIO).

Interfacing the UMFT240XE module to a microcontroller (MCU), or other logic devices for bus powered configuration is done in exactly the same way as a self-powered configuration (see Section 3). Except that it is possible for the MCU or external device to take its power supply from the USB bus (either the 5V from the USB pin, or 3.3V from the 3V3OUT pin).

5.3 Self Powered Configuration

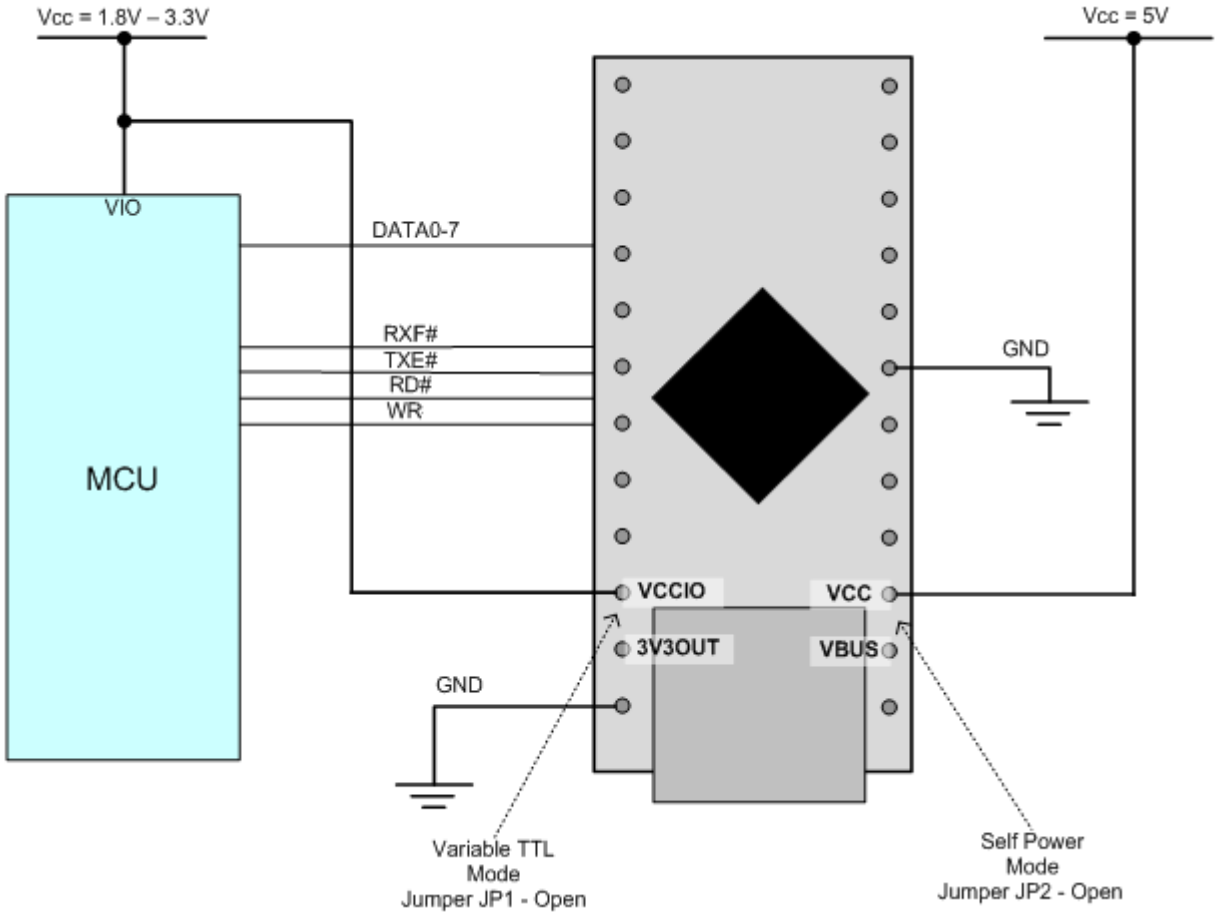


Figure 5.2 – Self-Powered Configuration

A self-powered configuration operates on the principle of drawing power from an external power supply, as oppose to drawing power from the USB host. In this configuration no current is drawn from the USB bus.

Figure 5.2 illustrates the UMFT240XE in a typical USB self-powered configuration. In this case the jumper connection of JP1 is removed, which allows 5V power to be supplied to the module VCC pins from an external source. VCCIO can to be powered from 3V3OUT or the VCC of an external source. (Note that Figure 5.2 is for illustration only and that the pins do not actually go all the way through the PCB)

For a self-powered configuration it is necessary to prevent current from flowing back to the USB data lines when the connected USB host or hub has powered down. To carry out this function the UMFT240XE uses an on-board voltage divider network connected to the USB power bus and RESET# pin. This operates on the principle that when no power is supplied to the VBUS line, the FT240X will automatically be held in reset by a weak pull-down, when power is applied the voltage divider will apply a weak 3.3V pull-up. Driving a level to the RESET# pin of the UMFT240XE will override the effect of this voltage divider. When the FT240X is in reset the USB DP signal pull-up resistor connected to the data lines is disconnected and no current can flow down the USB lines.

An example of interfacing the FT240X with a Microcontroller's UART interface is also illustrated in Figure 5.2. This example shows the wire configuration of the transfer and handshake lines. This example also illustrates that a voltage other than 3.3V can be supplied to the FT240X's IO port, this feature is described further and for bus powered mode in Section 5.5.

Alternatively both the FT240X's IO port and MCU can be powered from the 3V3OUT pin; this approach is described in Section 5.4.

5.4 USB Bus Powered with Power Switching Configuration

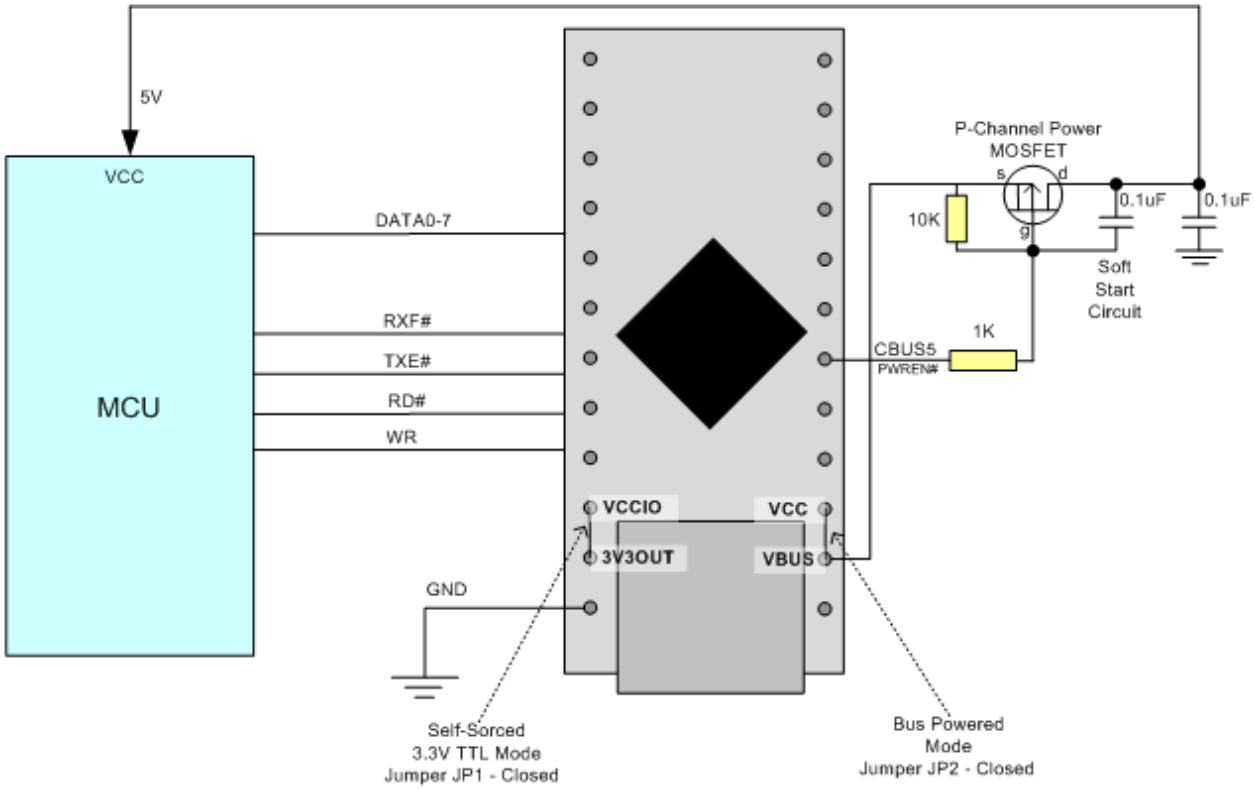


Figure 5.3 – Bus Powered with Power Switching Configuration

USB bus powered mode is introduced in Section 5.2. This section describes how to use bus-powered mode with a power switch.

USB bus powered circuits are required by USB compliance standards to consume less than 2.5mA (and less than 100mA when not enumerated and not suspended) when connected to a host or hub when in USB suspend mode. The PWREN# CBUS function can be used to remove power from external circuitry whenever the FT240X is not enumerated. (Note: It is impossible to be in suspended mode when enumerated.)(Note that Figure 5.3 is for illustration only and that the pins do not actually go all the way through the PCB)

To implement a power switch using PWREN#, configure a P-Channel Power MOSFET to have a soft start by fitting a 10K pull-up, a 1K series resistor and a 100nF cap as shown in Figure 5.3.

Connecting the source of the P-Channel MOSFET to 3V3OUT instead of VBUS can allow external logic to source 3.3V power from the FT240X without breaking USB compliancy. In this setup it is important that the VCCIO is not sourced from the drain of this MOSFET, this is because the power used to drive the gate of this transistor is sourced from VCCIO. VCCIO should be connected directly to 3V3OUT for this setup to function effectively. It is also important that the external logic must and IO core of the FT240X must not draw more that 50mA, this is because the current limit of the internal 3.3V regulator is 50mA.

5.5 Variable IO Voltage Supply

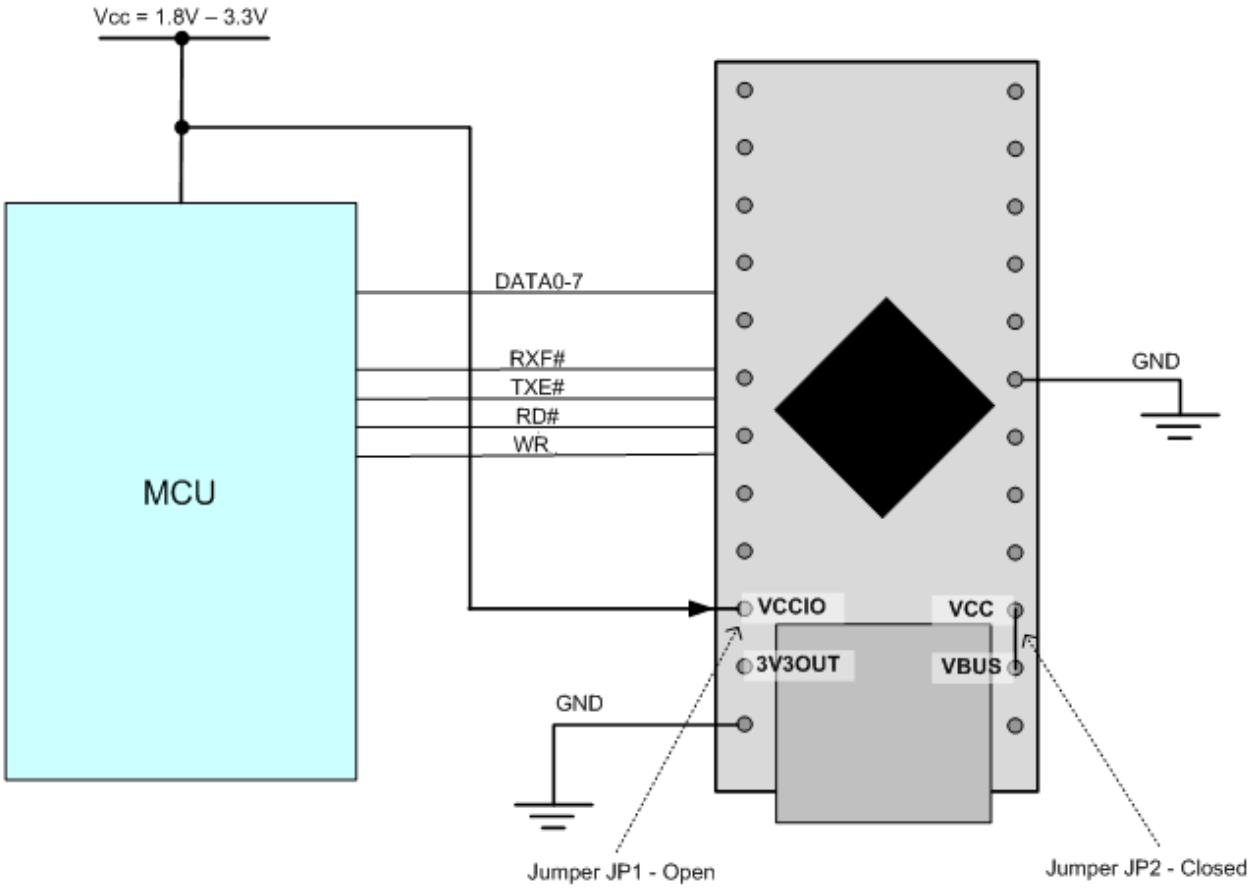


Figure 5.4 – USB Bus Powered 3.3V Logic Drive

The FT240X can process signals at CMOS/TTL logic levels in the range of 1.8V to 3.3V. This section describes how to utilise this feature.

Figure 5.4 shows a configuration where the FT240X is interfaced to a device with IOs operating in the range of 1.8V - 3.3V. The IO ports of this module need to be powered with a voltage level that is equal to the level of the signals it is processing. Since the FT240X's embedded voltage regulator only outputs 3V3 the IO ports will need to be powered from another power source when operating at voltage levels other than 3.3V.

By default, a short is present between 3V3OUT (embedded voltage regulator) and VCCIO (IO port's power input) with the connection made by JP1. If an external power supply is used to power the IO ports this jumper needs to be open.

The configuration described in this section can be implemented in either bus-powered mode or self-powered mode.

Note 1: The CBUS and DBUS pins are 5V tolerant; however, these signals cannot drive signals at 5V TTL/CMOS. VCCIO is not 5V tolerant; applying 5V to VCCIO will damage the chip.

Note 2: If power is applied to VCCIO and no power is applied to VCC all IOs will be at an unknown state, this however will not damage the chip. The FT240X also has protective circuitry to prevent the chip being damaged by a voltage discrepancy between VCCIO and the level of the signal being processed.

Note 3: When using VCCIO less than 3V3 on a chip from FTDI's X-chip range, it is recommended to uses pull up resistors (47K) to VCCIO on the data lines, all of the UMFT2xxXE devices include an on-board pull-up for these lines.

5.6 3.3V Voltage Supply

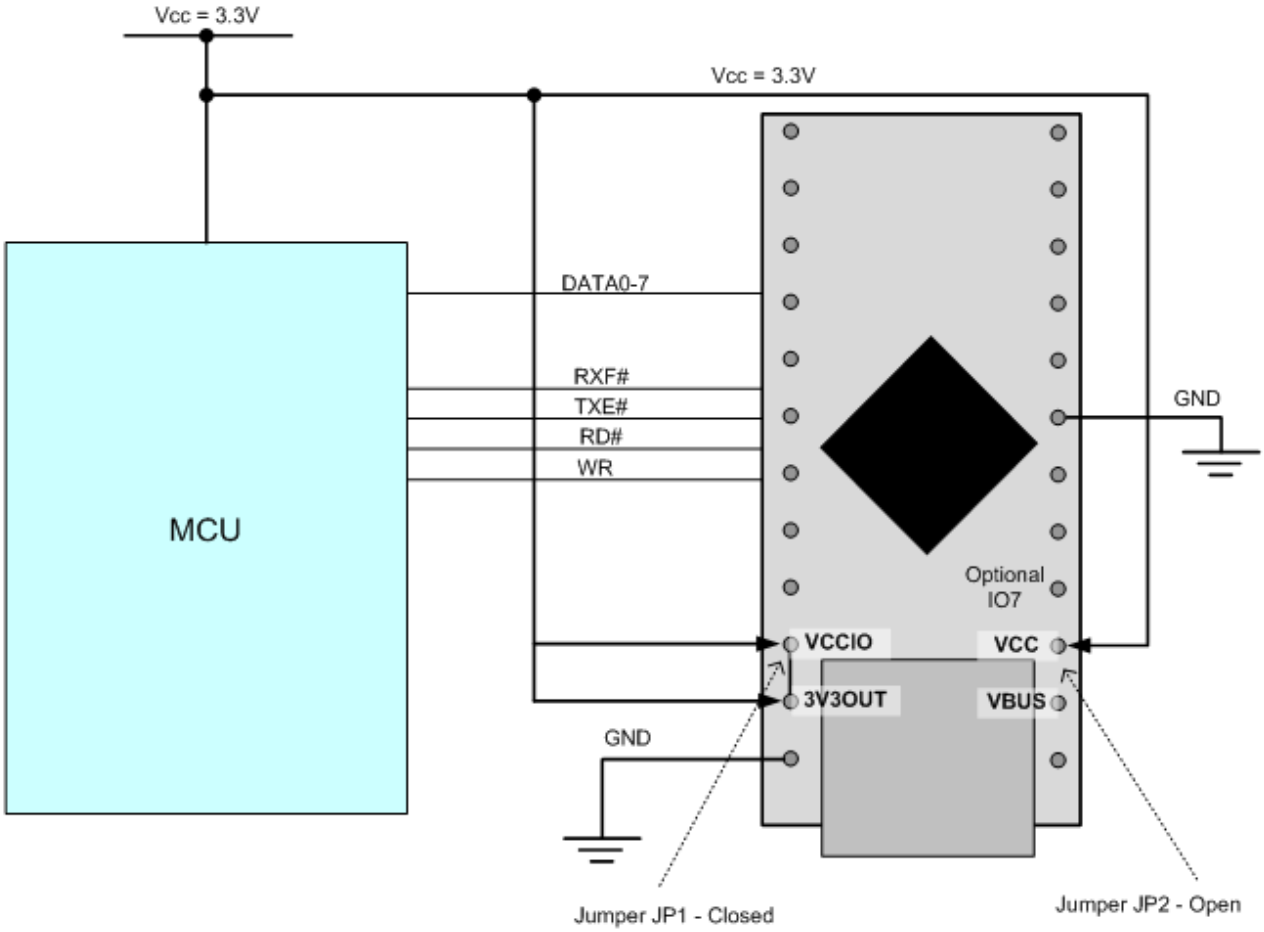


Figure 5.5 – USB Self-Powered 3.3V Logic Drive

The FT240X can be powered from a single 3.3V supply. This feature is an alternative to having the FT240X powered at 5V in standard self-powered configuration.

The 3.3V Self-Powered configuration is illustrated in Figure 5.5. Note that the 3.3V input is connected to VCC, VCCIO and 3V3OUT. (Note that Figure 5.5 is for illustration only and that the pins do not actually go all the way through the PCB).

5.7 Configuring the MTP ROM

The FT240X contains an embedded MTP ROM. This device can be used to specify the functions used by each CBUS pin, the current drive on each signal pin, current limit for the USB bus and the other descriptors of the device. For details on using the MTP ROM/EEPROM programming utility FT_PROG, please see the FT_PROG User Guide.

When programming the MTP ROM please note:

i) One of the CBUS Pins can be configured as PWREN# in the internal MTP ROM. This can be used to switch the power supply to the external circuitry.

ii) The Max Bus Power setting of the MTP ROM should specify the maximum current to be drawn from the USB host/hub when enumerated. For high-powered USB devices the current limit when enumerated is between 100mA and 500mA, for low-powered USB devices the current limit is 100mA.

6 Module Dimensions

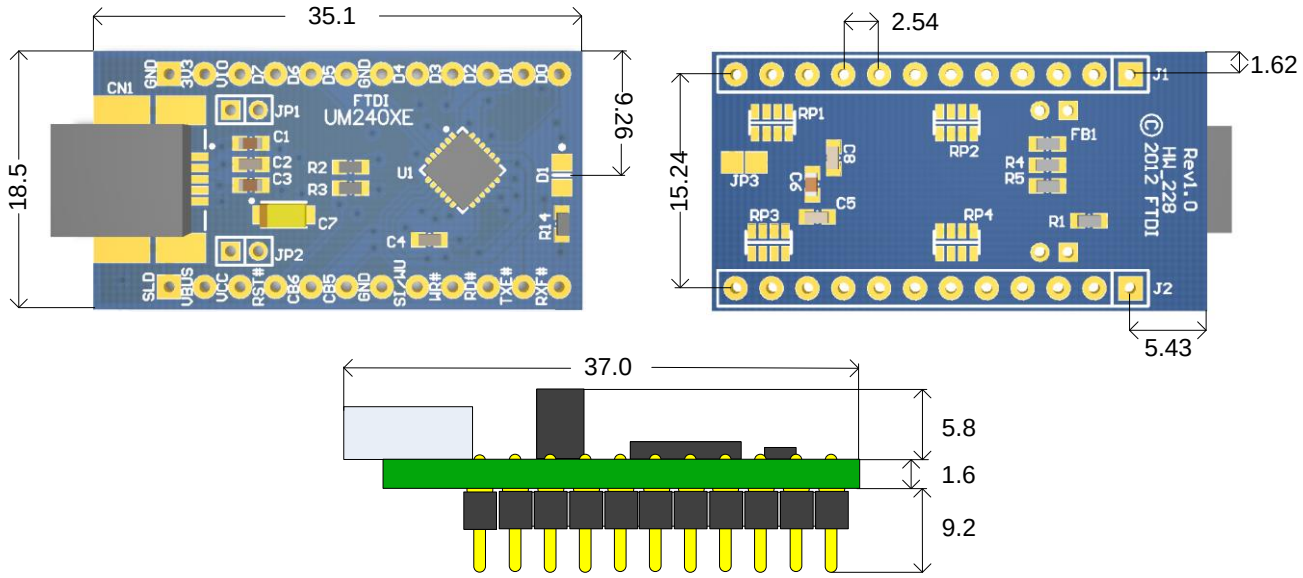
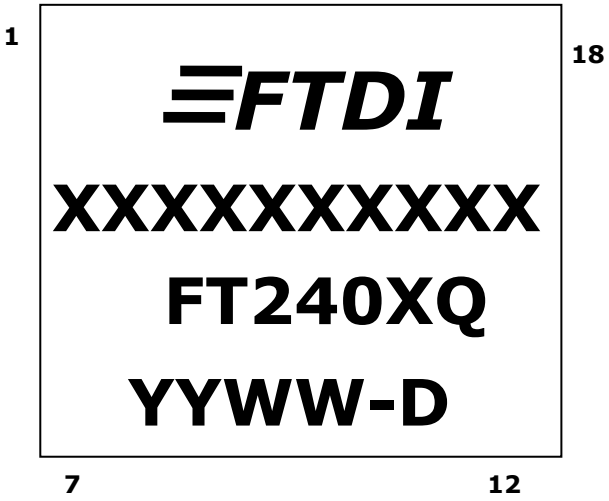


Figure 6.1 – UMFT240XE Module Dimensions

All dimensions are given in millimetres.

The UMFT240XE module exclusively uses lead free components, and is fully compliant with European Union directive 2002/95/EC.

7 IC Package Markings



The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number. This is followed by the revision letter.

The code **XXXXXXX** is the manufacturing LOT code.

8 UMFT240XE Module Circuit Schematic

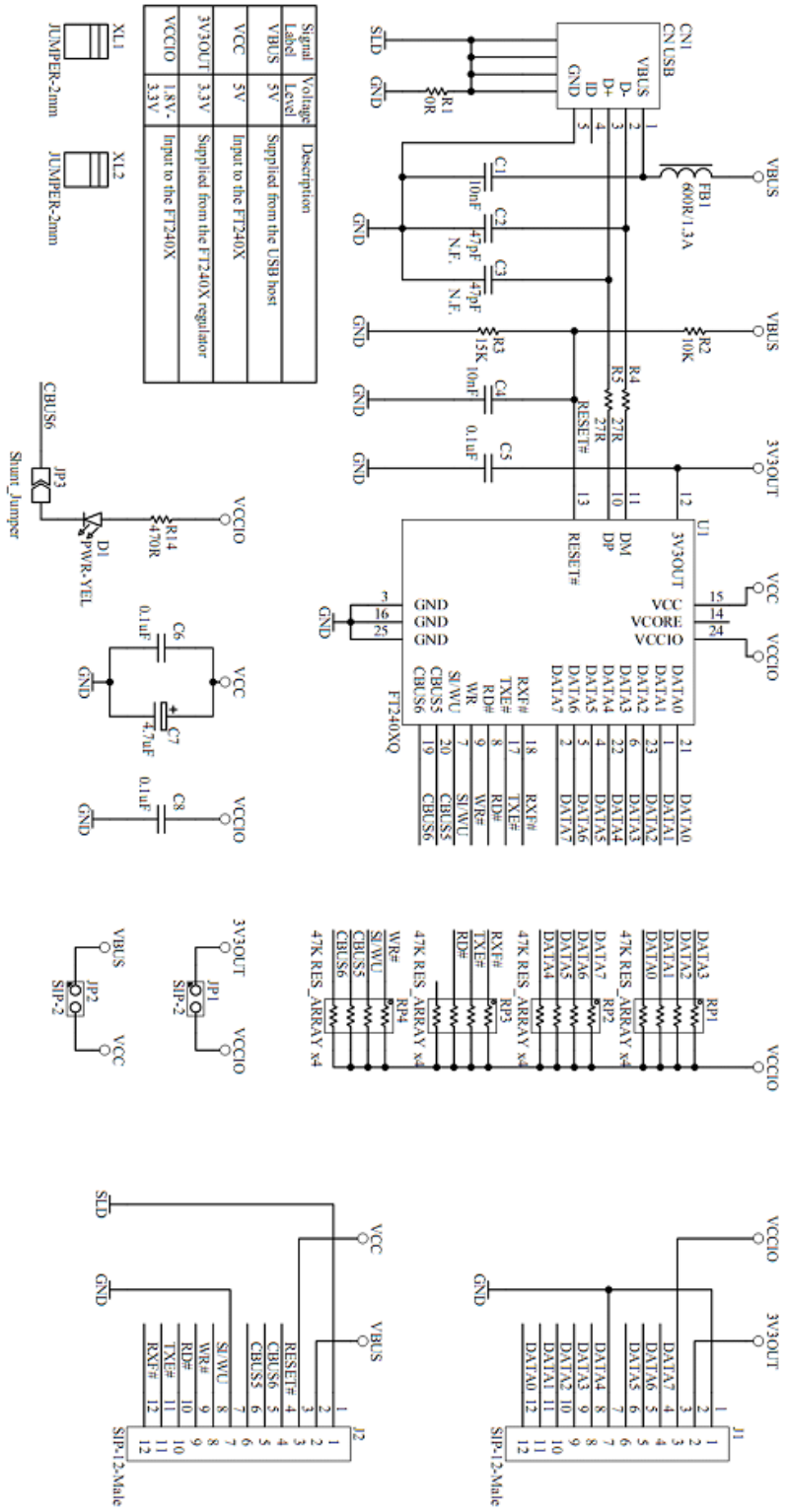


Figure 8.1 – Module Circuit Schematic

9 Internal MTP ROM Configuration

Following a power-on reset or a USB reset the FT240X will scan its internal MTP ROM and read the USB configuration descriptors stored there. The default values programmed into the internal MTP ROM in the FT240XQ used on the UMFT240XE are shown in Table 8.1.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6015h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the MTP ROM during final test of the UM232R module.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when the power is shut off (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	UMFT240XE	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT240X	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Enabled	Taking RI# low will wake up the USB host controller from suspend.
High Current I/Os	Disabled	Enables the high drive level on the data and CBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the CVP driver interface for the device.
CBUS5	Tristate	
CBUS6	Tristate	

Table 9.1 – Default Internal MTP ROM Configuration

The internal MTP ROM in the FT240X can be programmed over USB using the utility program FT_PROG. FT_PROG can be downloaded from the www.ftdichip.com. Users who do not have their own USB vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI Support (support1@ftdichip.com) for this service, also see TN_100 and TN_101.

10 Contact Information

Head Office – Glasgow, UK

Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Hillsboro, Oregon, USA

7130 SW Fir Loop
Tigard, OR 97223
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan

2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China

Room 1103, No. 666 West Huaihai Road,
Shanghai, 200052
China
Tel: +86 (0)21 6235 1596
Fax: +86 (0)21 6235 1595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A - References

Document References

FT201XQ

FT231XQ

FT240XQ

FT_PROG User Guide

TN_100

TN_101

Acronyms and Abbreviations

Terms	Description
DIP	Dual In-line Package
DLL	Dynamic Link Library
FIFO	First In First Out
EEPROM	Electrically Erasable Programmable Read Only Memory
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
VCP	Virtual COM Port

Appendix B - List of Figures and Tables

List of Figures

List of Tables

Appendix C – Revision History

Document Title: UMFT240XE Datasheet
Document Reference No.: FT_000653
Clearance No.: FTDI# 295
Product Page: http://www.ftdichip.com/FT-X.htm
Document Feedback: Send Feedback

Revision	Changes	Date
Version 1.0	Initial Datasheet Created	2012-06-12
Version 1.1	Added a section for package marking and changed TIDs. Edited figure 4.1, 5.2, 5.3, 5.4, 5.5 and 7.1 – WR# to WR	2013-01-29
Version 1.2	Removed TXLED/RXLED/TX&RXLED CBUS functionality. Document template changes made.	2019-02-26