NCN2612

6-Differential Channel 1:2 Switch for PCIe 2.0 and Display Port 1.1

The NCN2612 is a 6−Channel differential SPDT switch designed to route PCI Express Gen2 and/or DisplayPort 1.1a signals. Due to the ultra−low ON−state capacitance (4.1 pF typ) and resistance (7 Ω typ), these switches have a signal bit rate (BR) of 5 Gbps, ideal for high frequency data signals. This switch pinout is designed to be used in ATX form factor desktop PCs and is available in a space−saving WQFN package. The NCN2612 uses 80% less quiescent power than other comprable PCIe switches.

Features

- V_{DD} Power Supply from 3 V to 3.6 V
- Low Supply Current 250 μA typ
- 6 Differential Channels 2:1 MUX/DEMUX
- Compatible with Display Port 1.1a & PCIe 2.0
- Data Rate: Supports 5 Gbps
- Low Ron Resistance: 7 Ω typ
- Low Con Capacitance: 4.1 pF
- Space Saving Small WQFN−56 Package
- This is a Pb−Free Device

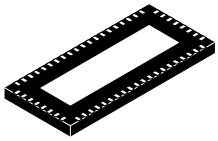
Typical Applications

- Notebook Computers
- Desktop Computers
- Server/Storage Networks

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MARKING DIAGRAM



WQFN56
CASE 510AK



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCN2612MTTWG	WQFN56 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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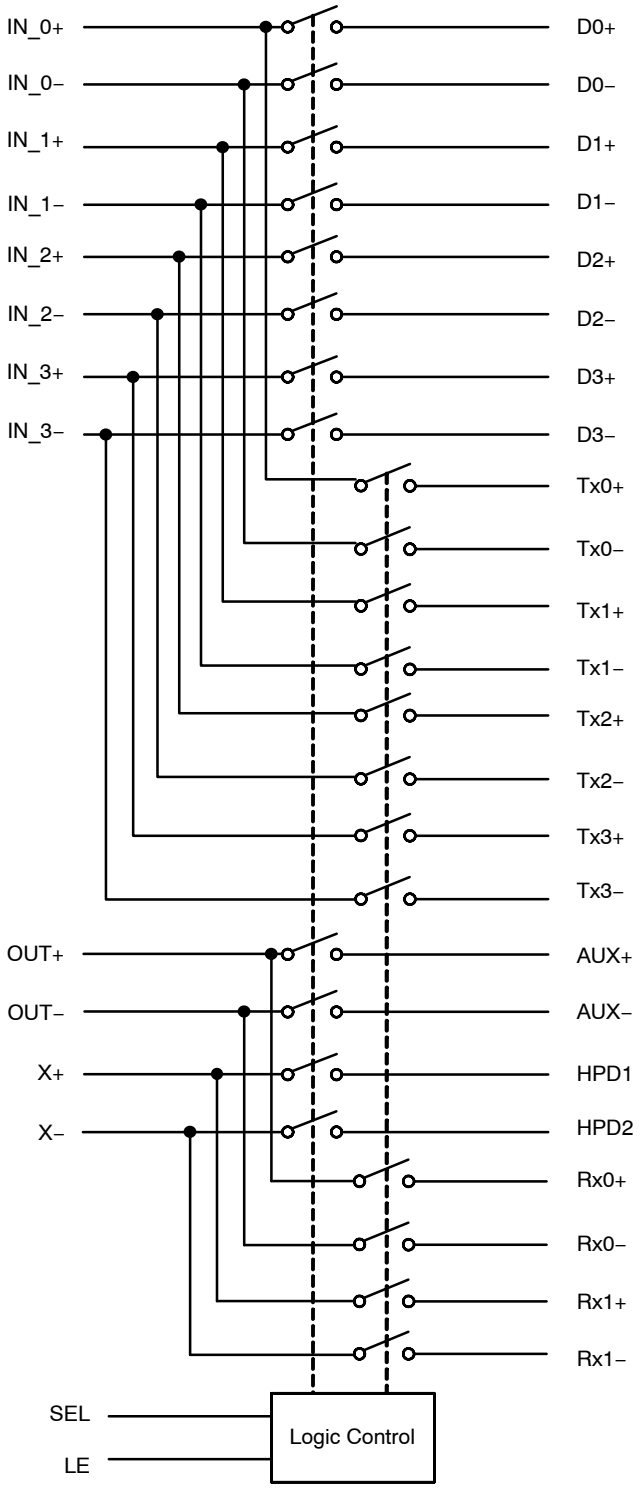


Figure 1. NCN2612 Block Diagram

TRUTH TABLE (SEL Control)

Function	SEL
PCI_Express Gen2 Path is Active (Tx, Rx)	L
Digital Video Port is Active (Dx, HPDx, AUX)	H

TRUTH TABLE (Latch Control)

LE	Internal Mux Select
0	Respond to Changes on SEL
1	Latched

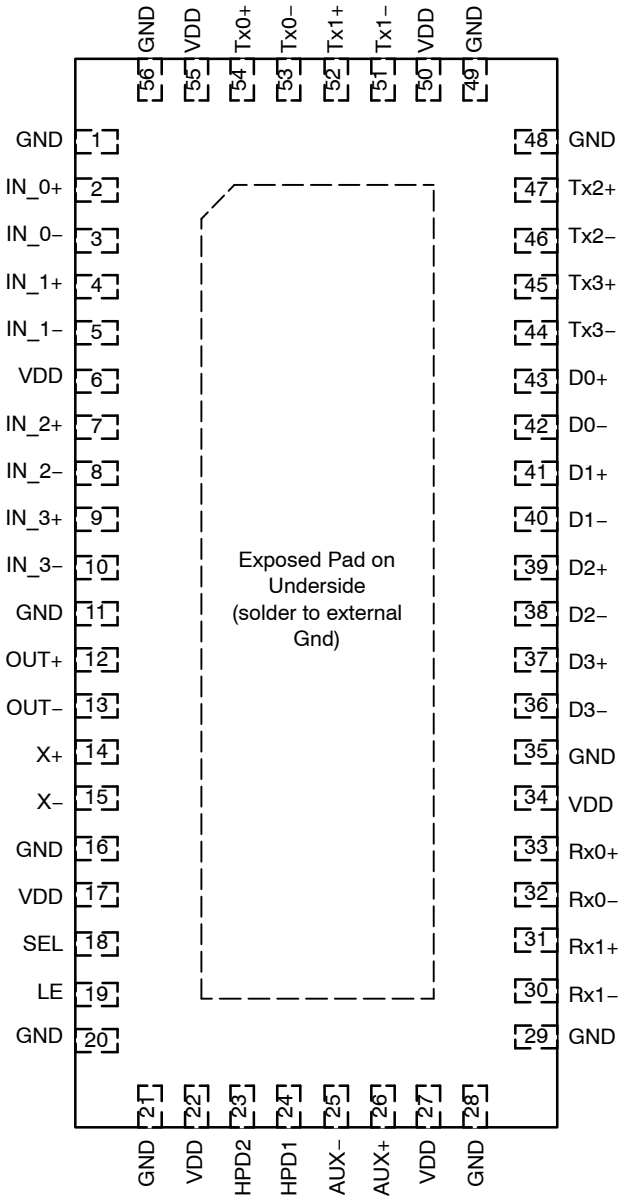


Figure 2. Pinout
(Top View)

PIN FUNCTION AND DESCRIPTION

Pin	Name	Description
6, 17, 22, 27, 34,50, 55	VDD	DC Supply, 3.3 V ±10%
1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	Power Ground.
Exposed Pad	–	The exposed pad on the backside of package is internally connected to Gnd. Externally the exposed pad should also be user−connected to GND.
2	IN_0+	Differential input from GMCH PCIE outputs. IN_0+ makes a differential pair with IN_0−.
3	IN_0−	Differential input from GMCH PCIE outputs. IN_0− makes a differential pair with IN_0+.
4	IN_1+	Differential input from GMCH PCIE outputs. IN_1+ makes a differential pair with IN_1−.
5	IN_1−	Differential input from GMCH PCIE outputs. IN_1− makes a differential pair with IN_1+.
7	IN_2+	Differential input from GMCH PCIE outputs. IN_2+ makes a differential pair with IN_2−.
8	IN_2−	Differential input from GMCH PCIE outputs. IN_2− makes a differential pair with IN_2+.
9	IN_3+	Differential input from GMCH PCIE outputs. IN_3+ makes a differential pair with IN_3−.
10	IN_3−	Differential input from GMCH PCIE outputs. IN_3− makes a differential pair with IN_3+.
12	OUT+	Pass−through output from AUX+ input when SEL = 1. Pass−through output from Rx0+ input when SEL = 0.
13	OUT−	Pass−through output from AUX− input when SEL = 1. Pass−through output from Rx0− input when SEL = 0.
14	X+	X+ is an analog pass−through output corresponding to Rx1+.
15	X−	X− is an analog pass−through output corresponding to the Rx1− input. The path from Rx1− to X− must be matched with the path from Rx1+ to X+. X+ and X− form a differential pair when the pass−through mux mode is selected.
18	SEL	SEL controls the mux through a flow−through latch. SEL = 0 for PCIE Mode; SEL = 1 for DP Mode
19	LE	The latch gate is controlled by LE.
43, 42	D0+, D0−	Analog pass−through output#1 corresponding to IN_0+ and IN_0−, when SEL = 1.
41, 40	D1+, D1−	Analog pass−through output#1 corresponding to IN_1+ and IN_1−, when SEL = 1.
39, 38	D2+, D2−	Analog pass−through output#1 corresponding to IN_2+ and IN_2−, when SEL = 1.
37, 36	D3+, D3−	Analog pass−through output#1 corresponding to IN_3+ and IN_3−, when SEL = 1.
54, 53	Tx0+, Tx0−	Analog pass−through output#2 corresponding to IN_0+ and IN_0− when SEL = 0.
52, 51	Tx1+, Tx1−	Analog pass−through output#2 corresponding to IN_1+ and IN_1− when SEL = 0.
47, 46	Tx2+, Tx2−	Analog pass−through output#2 corresponding to IN_2+ and IN_2− when SEL = 0.
45, 44	Tx3+, Tx3−	Analog pass−through output#2 corresponding to IN_3+ and IN_3− when SEL = 0.
26	AUX+	Differential input from HDMI/DP connector. AUX+ makes a differential pair with AUX−. AUX+ is passed through to the OUT+ pin when SEL = 1.
25	AUX−	Differential input from HDMI/DP connector. AUX− makes a differential pair with AUX+. AUX− is passed through to the OUT− pin when SEL = 1.
24	HPD1	Positive low frequency HPD input handshake protocol signal.
23	HPD2	Negative low frequency HPD input handshake protocol signal (normally not connected).
33	Rx0+	Differential input from PCIE connector or device. Rx0+ makes a differential pair with Rx0−. Rx0+ is passed through to the OUT+ pin when SEL = 0.
32	Rx0−	Differential input from PCIE connector or device. Rx0− makes a differential pair with Rx0+. Rx0− is passed through to the OUT− pin when SEL = 0.
31	Rx1+	Differential input from PCIE connector or device. Rx1+ makes a differential pair with Rx1−. Rx1+ is passed through to the X+ pin when SEL = 0.
30	Rx1−	Differential input from PCIE connector or device. Rx1− makes a differential pair with Rx1+. Rx1− is passed through to the X− pin on the path that matches the Rx1+ to X+ pin.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltages	V_{DD}	$-0.5 \le V_{DD} \le 5.3$	V
Input/Output Voltage Range of the Switch	V_I & V_O	$-0.7 \le V_I \le V_{DD} + 0.3$	V
Selection Pin Voltages	V_{SEL}	$-0.5 \le V_I \le V_{DD} + 0.3$	V
Continuous Current Through One Switch Channel	I_{IO}	± 120	mA
Maximum Junction Temperature (Note 1)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction−to−Air (Note 2)	$R_{\theta JA}$	37	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
2. This parameter is based on EIA/JEDEC 51−7 with a 4−layer PCB, 80mm x 80mm, two 1oz Cu material internal planes and top planes of 2oz Cu material.

ELECTRICAL CHARACTERISTICS (V_{DD} = +3.3V ±10%, T_A = −40°C to +85°C and T_J up to 125°C, unless otherwise noted. All Typical values are at V_{DD} = +3.3 V, T_A = +25°C, unless otherwise noted)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{DD}	Supply Voltage Range		3.0	3.3	3.6	V
I_{DD}	Power Supply Current	V_{DD} = 3.6 V, V_{IN} = GND or V_{DD}		250	500	μA
DATA SWITCH PERFORMANCE (for both PCIe and Display Port applications, unless otherwise noted)						
V_{IN}	Data Input/Output Voltage Range		−0.1		V_{DD}	V
R_{ON}	On Resistance (Tx, Rx)	V_{DD} = 3 V, 0 V ≤ V_{IN} ≤ V_{DD}, I_{IN} = 40 mA		7	13	Ω
R_{ON}	On Resistance (Dx,HP-Dx,AUX)	V_{DD} = 3 V, 0 V ≤ V_{IN} ≤ V_{DD}, I_{IN} = 40 mA		7.5	13	Ω
$R_{ON(flat)}$	On Resistance Flatness	V_{DD} = 3 V, 0 V ≤ VIN ≤ V_{DD}, I_{IN} = 40 mA		0.1	1.24	Ω
ΔR_{ON}	On Resistance Matching (Tx, Rx)	V_{DD} = 3 V, V_{IN} = 0 V, I_{IN} = 40 mA			0.35	Ω
ΔR_{ON}	On Resistance Matching (Dx,HPDx,AUX)	V_{DD} = 3 V, V_{IN} = 0 V, I_{IN} = 40 mA			0.35	Ω
C_{ON}	On Capacitance	f = 1 MHz, Switch On, Open Output		4.1		pF
C_{OFF}	Off Capacitance	f = 1 MHz, Switch Off		2.6		pF
I_{ON}	On Leakage Current (IN_/ X_/OUT_)	V_{DD} = +3.6 V, $V_{IN_}$ = $VX_$ = $V_{OUT_}$ = 0 V, +1.2 V; $V_{D_}$ or $V_{\overline{TX}_}$ or $V_{\overline{HPD}_}$ or $V_{\overline{RX}_}$ or $V_{\overline{AUX}_}$ = unconnected	−1		+1	μA
I_{OFF}	Off Leakage Current (D_/ TX_/ HPD_ / RX_/ AUX_)	V_{DD} = +3.6 V, $V_{IN_}$ = $V_{X_}$ = $V_{OUT_}$ = 0 V, +1.2 V; $V_{D_}$ or $V_{TX_}$; $V_{HPD_ / AUX_}$ or $V_{RX_}$ = 1.2 V, 0 V	−1		+1	μA
CONTROL LOGIC CHARACTERISTICS (SEL and LE pins)						
V_{IL}	Off voltage input		0		0.8	V
V_{IH}	High voltage input		2		V_{DD}	V
I_{IN}	Off voltage input	V_{IN} = 0 V or V_{DD}	−1		+1	μA
C_{IN}	High voltage input	f = 1 MHz		1		pF
DYNAMIC CHARACTERISTICS						
BR	Signal Data Rate	R_S = R_L = 100 Ω differential		5		Gbps
I_{LOSS}	Differential Insertion Loss	R_S = R_L = 50 Ω, F = 2.7 GHz		−4		dB
		R_S = R_L = 50 Ω, F = 5 GHz		−7		
		R_S = R_L = 50 Ω, F = 7.5 GHz		−13		
V_{ISO}	Differential Off Isolation	R_S = R_L = 50 Ω, F = 100 MHz		−41		dB
		R_S = R_L = 50 Ω, F = 1.35 GHz		−19		
		R_S = R_L = 50 Ω, F = 3 GHz		−16		
X_{talk}	Differential Crosstalk	R_S = R_L = 50 Ω, F = 2.5 GHz		−27		dB
		R_S = R_L = 50 Ω, F = 5 GHz		−20		
		R_S = R_L = 50 Ω, F = 7.5 GHz		−10		

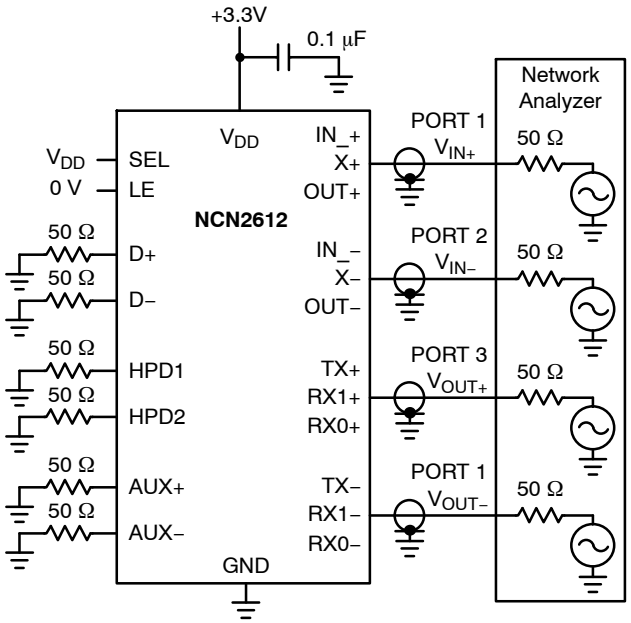
SWITCHING CHARACTERISTICS (V_{DD} = +3.3 V, T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
T_{SK1}	Bit−to−bit skew within same differential channel	R_S = 50 Ω, R_L = 200 Ω, C_L = 4 pF		7		ps
T_{SK2}	Channel−to−channel skew	R_S = 50 Ω, R_L = 200 Ω, C_L = 4 pF		55		ps

SELECTION PINS SWITCHING CHARACTERISTICS (V_{DD} = +3.3 V, T_A = 25°C, unless otherwise specified)

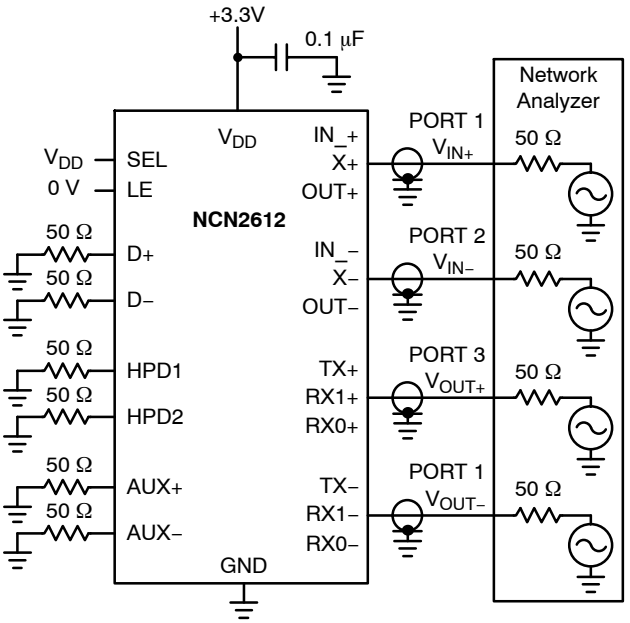
Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
T_{SELON}	SEL to Switch turn ON time	VDX_A or VDX_B = +1.0 V, R_L = 50 Ω, VHPD_X or VAUX_X = +1.0 V, R_L = 50 Ω, LE = V_{DD}, C_L = 100 pf		8	20	ns
T_{SELOFF}	SEL to Switch turn OFF time	VDX_A or VDX_B = +1.0 V, R_L = 50 Ω, VHPD_X or VAUX_X = +1.0 V, R_L = 50 Ω, LE = V_{DD}, C_L = 100pf		5	10	ns
T_{SET}	LE setup time SEL to LE	VDX_A or VDX_B = +1.0 V, R_L = 50 Ω, VHPD_X or VAUX_X = +1.0 V, R_L = 50 Ω, LE = V_{DD}, C_L = 100 pf		1		ns
T_{HOLD}	LE hold time LE to SEL	VDX_A or VDX_B = +1.0 V, R_L = 50 Ω, VHPD_X or VAUX_X = +1.0 V, R_L = 50 Ω, LE = V_{DD}, C_L = 100 pf		1		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.



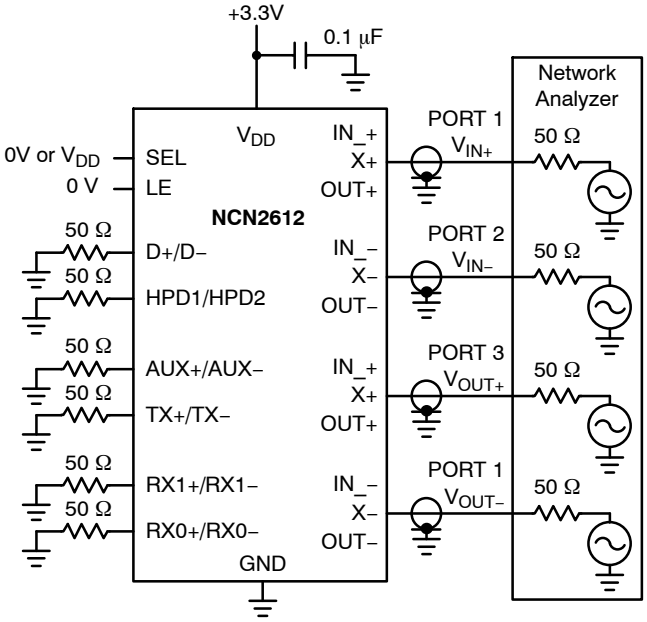
$$\text{Differential Insertion Loss} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

Figure 3. Differential Insertion Loss/Differential Return Loss



$$\text{Differential Off Isolation} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

Figure 4. Differential Off−Isolation



$$\text{Differential Crosstalk} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

Figure 5. Differential Crosstalk

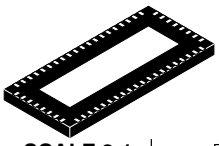
Measurements are standardized against shorts at IC terminals.
Differential OFF−Isolation is measured between IN_ and “OFF” D or TX, X and “OFF” HPD or RX1, OUT and “OFF” AUX or RX0 terminal on each switch under Figure 3.
Differential ON−Isolation is measured between IN_ and “ON” D or TX, X and “ON” HPD or RX1, OUT and “ON” AUX or RX0 terminal on each switch under Figure 4.
Differential Crosstalk is measured between any two pairs.

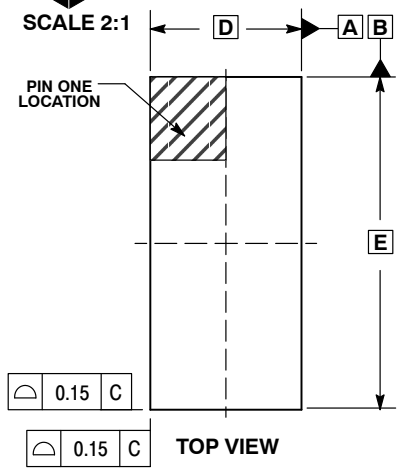
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PACKAGE DIMENSIONS

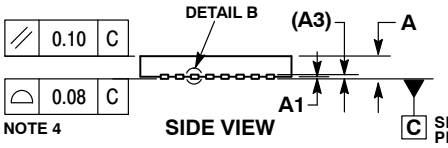
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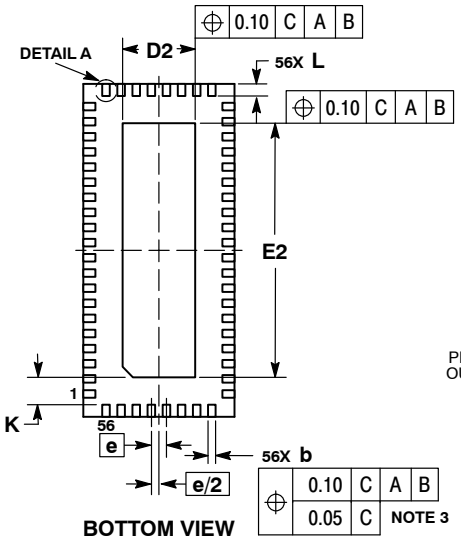
WQFN56 5x11, 0.5P
CASE 510AK−01
ISSUE A

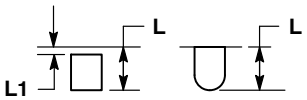
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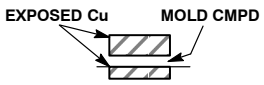








DETAIL A
ALTERNATE CONSTRUCTIONS

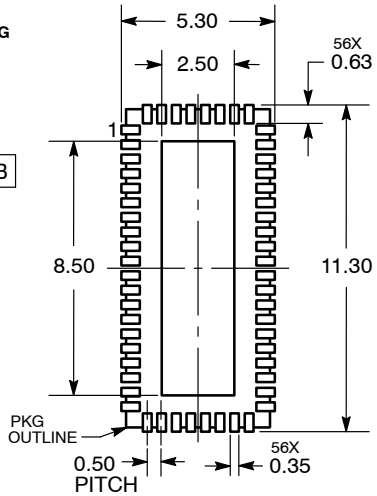


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

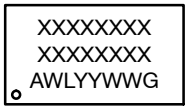
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	−−−	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	2.30	2.50
E	11.00 BSC	
E2	8.30	8.50
e	0.50 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	−−−	0.15

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**WQFN56 5x11, 0.5P**	**PAGE 1 OF 1**

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