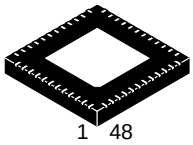
NB3N401S

3.3 V Quad Channel Half-Duplex M-LVDS Driver Receiver

ON Semiconductor®

www.onsemi.com



QFN48
CASE 485EP

Description

The NB3N401S is a 3.3 V supply Quad Multipoint Low Voltage Differential Signals (M−LVDS) line drivers and receivers. The device is TIA/EIA−899 compliant. The device offers the Type 1 receiver threshold at 0.0 V and the Type 2 receiver threshold at 0.1 V. The NB3N401S supports four independent Half Duplex bus configurations.

Each of the four sections has Pin (SEL) for selection of Type−1 and Type−2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common mode voltage range of −1 V to 3.4 V. The Type−1 receivers have near zero thresholds (±50 mV) and exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type−2 receivers include an offset threshold to provide a detectable voltage under open-circuit, idle-bus, and other faults conditions.

The NB3N401S is offered in a 48 Pin 7 mm × 7 mm × 0.9 mm QFN package.

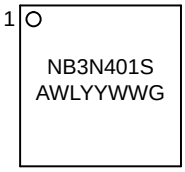
Features

- Low-Voltage Differential 30 to 55 Ω Line Drivers and Receivers for Signaling Rates Up to 250 Mbps
- Clock Frequencies up to 125 MHz
- Type−1 Receivers Incorporate 25 mV of Hysteresis
- Type−2 Receivers Provide an Offset (100 mV)
- Compatible with TIA/EIA−899 Standard for Multipoint Data Interchange
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- −1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With up to 2 V of Ground Noise
- Bus Pins High Impedance when Disabled or $V_{CC} \le 1.5$ V
- Independent Enable for each Driver and Receiver
- Independent Select for each Type1 and Type2 Receivers
- M−LVDS Bus Power Up/Down Glitch Free
- Power Down Pin for Device Power Down
- Operating Range: V_{CC} = 3.3 V ±0.3 V (3.0 to 3.6 V)
- Operation from –40°C to 85°C.
- Enhanced ESD Protection: 7 kV HBM on all the Pins
- These are Pb-Free Devices

Applications

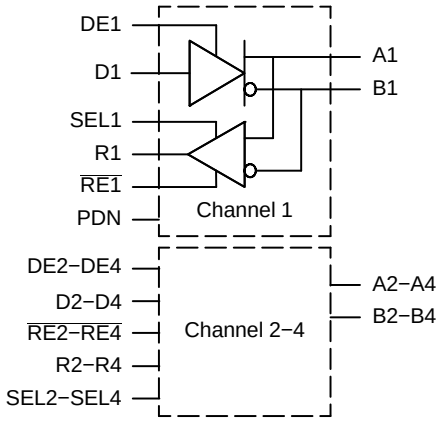
- Mobile Base Station Back Plane System
- Central Office Switches
- Network Switches

MARKING DIAGRAM



NB3N401S	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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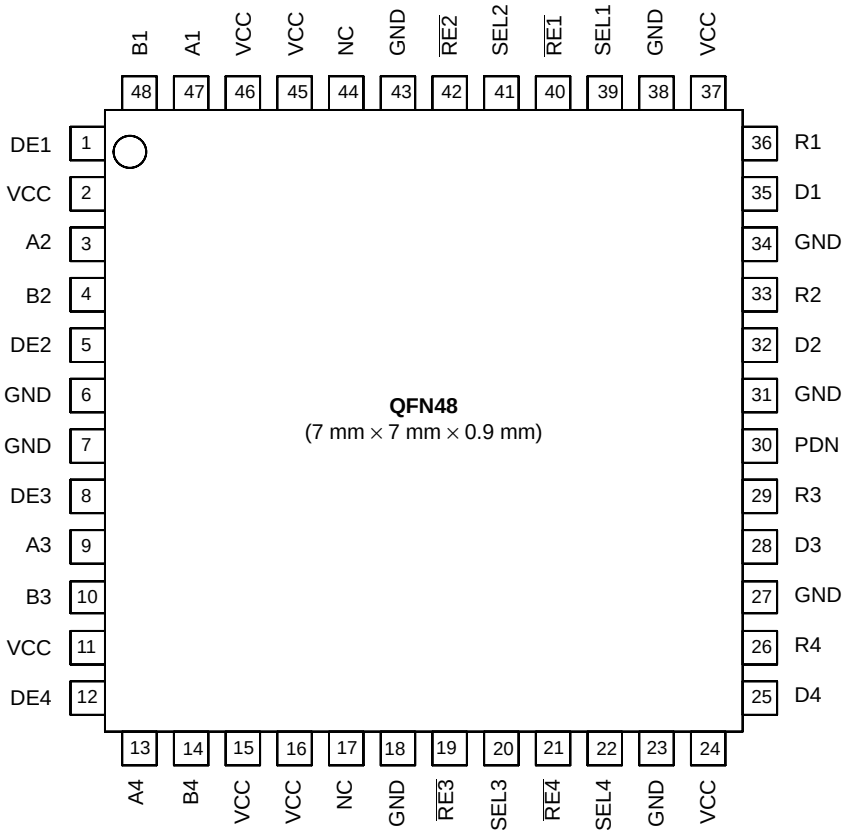


Figure 1. Pinout Diagram
(Top View)

Table 1. PIN DESCRIPTION

Number	Name	I/O Type	Description
1, 5, 8, 12	DE1−DE4	INPUT	Driver Enable Pins – Separate for each Driver, (HIGH = Active, LOW = High Z Output). This Pin will be pulled internally to Logic LOW when left open
2, 11, 15, 16, 24, 37, 45, 46	VCC		Power Supply Pins. Pins must be connected to power supply to guarantee proper operations
3, 9, 13, 47	A1−A4	M−LVDS Input/Output	Transceiver Input/Output Pins
4, 10, 14, 48	B1−B4	M−LVDS Input/Output	Transceiver Invert Input/Output Pins
6, 7, 18, 23, 27, 31, 34, 38, 43	GND		Ground Pins. All pins must be connected to Ground to guarantee proper operations
19, 21, 40, 42	$\overline{RE1}$−$\overline{RE4}$	INPUT	Receiver Enable Pins – Separate for each Receiver, (LOW = Active, HIGH = High Z Output). This Pin will be pulled internally to Logic HIGH when left open
20, 22, 39, 41	SEL1−SEL4	INPUT	Failsafe Enable Pins. Separate for each Receiver section. LOW = Type 1 Receiver Input, HIGH = Type 2 Receiver Input. This Pin will be pulled internally to Logic HIGH when left open
25, 28, 32, 35	D1−D4	LVCMOS INPUT	Driver Input Pins
26, 29, 33, 36	R1−R4	LVCMOS OUTPUT	Receiver Output Pins
30	PDN	INPUT	Power Down Pin. When pulled Low, Device powers down. (HIGH = Active, LOW = High Z Output). This Pin will be pulled internally to Logic LOW when left open.
GNDPAD			Exposed PAD − Must be connected to GND on the PCB for proper device operation
17, 44	NC		No Connect (Pins must be left open)

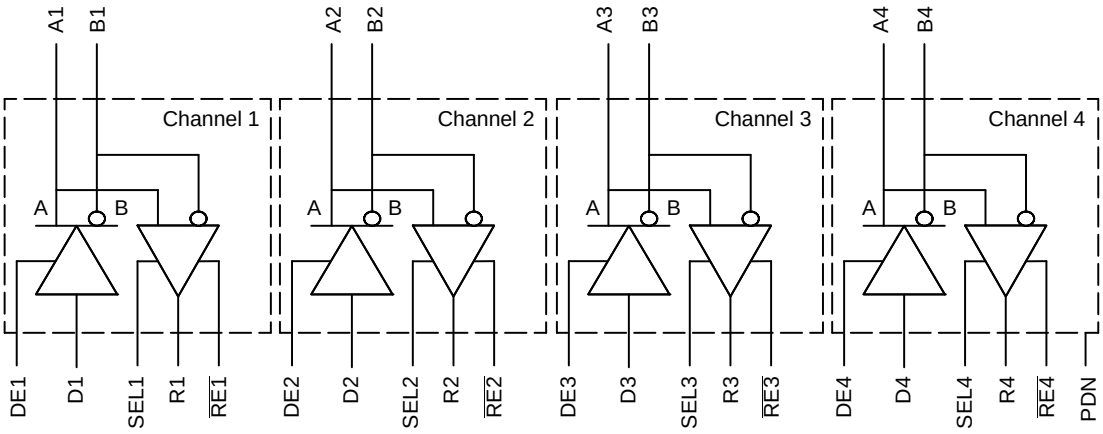


Figure 2. Block Diagram

Table 2. DEVICE FUNCTION TABLE

TYPE1 Receiver	**Inputs**				**Output**
	$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**SEL**	**PDN**	**R**
	V_{ID} > 35 mV	L	L	H	H
	−35 mV ≤ V_{ID} ≤ 35 mV	L	L	H	?
	V_{ID} < 35 mV	L	L	H	L
	Open	L	L	H	?
	X	Open	X	H	Z
	X	X	X	L	Z
	X	H	X	H	Z
TYPE2 Receiver	**Inputs**				**Output**
	$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**SEL**	**PDN**	**R**
	V_{ID} > 150 mV	L	H	H	H
	50 mV ≤ V_{ID} ≤ 150 mV	L	H	H	?
	V_{ID} < 50 mV	L	H	H	L
	Open	L	H	H	L
	X	Open	X	H	Z
	X	H	X	H	Z
	X	X	X	L	Z

Driver	**Inputs**	**Enable**	**Output**	
	D	**DE**	**A**	**B**
	L	H	L	H
	H	H	H	L
	OPEN	H	L	H
	X	OPEN	Z	Z
	X	L	Z	Z

*H = HIGH, L = LOW, Z = High Impedance, X Don't Care, ? = Indeterminate (Transition State)

Table 3. ATTRIBUTES (Note 1)

Characteristics			Value
ESD Protection	Human Body Model (JEDEC Standard JS−001−2014)	All Pins	±7 kV
	Charged Device Model (JEDEC Standard 22, Method C101−D)	All Pins	±1500 V
Moisture Sensitivity (Note 1)			Level 3
Flammability Rating Oxygen Index: 28 to 34			UL−94 Code V−0 A 1/8″ 28 to 34
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latch-Up Test			

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition	Rating	Unit
V_{CC}	Supply Voltage		$-0.5 \le V_{CC} \le 4.0$	V
V_{IN}	Input Voltage	D, DE, $\overline{RE}$, SEL A, B	$-0.5 \le V_{IN} \le 4.0$ $-1.8 \le V_{IN} \le 4.0$	V
V_{OUT}	Output Voltage	R A or B	$-0.3 \le V_{OUT} \le 4.0$ $-1.8 \le V_{OUT} \le 4.0$	V
T_A	Operating Temperature Range, Industrial		−40 to +85	°C
T_J	Maximum Junction Temperature		140	°C
T_{STG}	Storage Temperature Range		−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

Table 5. THERMAL CHARACTERISTICS

Symbol	Parameter	Condition	Rating	Unit
θ_{JP}	Thermal Resistance (Junction-to-Pad)	(Note 2)	1.5 (Typ)	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	16 (Typ)	°C/W
θ_{JB}	Thermal Resistance (Junction-to-Board)	(Note 2)	11 (Typ)	°C/W
P_D	Power Dissipation	$\overline{RE}$ = 0 V, DE = 0 V, CL = 15 pF, VID = 400 mV, 125 MHz, All Other Pins Open	382 (Max)	mW

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS (V_{CC} = 3.3 V ±0.3 V, GND = 0 V, T_A −40°C TO +85°C)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{CC}	Power Supply Current	Driver Only	Receiver Disabled, Driver Enabled, $\overline{RE}$ and DE at V_{CC}, R_L = 50 Ω, 125 MHz, All Others Open, PDN = High			76	mA
		Both Driver and Receiver Disabled	Driver and Receiver Disabled, $\overline{RE}$ at V_{CC}, DE at 0 V, R_L = No Load, 125 MHz, All Others Open, PDN = High			10	
		Both Driver and Receiver Enabled	Driver and Receiver Enabled, $\overline{RE}$ at 0 V, DE at V_{CC}, R_L = 50 Ω, C_L = 15 pF, 125 MHz, All Others Open, PDN = High			165	
		Receiver Only	Receiver Enabled, Driver Disabled, $\overline{RE}$ and DE at 0 V, R_L = 50 Ω, C_L = 15 pF, 125 MHz, All Others Open, PDN = High			100	
PDN	Power Down (PDN = L)			−	−	5	mA
V_{IH}	Input HIGH Voltage			2	−	VCC	V
V_{IL}	Input LOW Voltage			GND	−	0.8	V
V_{BUS}	Voltage at any Bus Terminal VA. VB			−1.4	−	3.8	V
|VID|	Magnitude of Differential Input Voltage			0.05	−	VCC	V

Table 7. ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ±0.3 V, GND = 0 V, T_A −40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BUS INPUT AND OUTPUT						
I_A	Receiver or Transceiver with Driver Disabled Input Current	V_A = 3.8 V, V_B = 1.2 V V_A = −1.4 V, V_B = 1.2 V	− −32	− −	32 −	μA
I_B	Receiver or Transceiver with Driver Disabled Input Current	V_B = 3.8 V, V_A = 1.2 V V_B = −1.4 V, V_A = 1.2 V	− −32	− −	32 −	μA
I_{AB}	Receiver or Transceiver with Driver Disabled Differential Input Current (I_A – I_B)	V_A = V_B, −1.4 V ≤ V_A ≤ 3.8 V	−4	−	4	μA
I_{AOFF}	Receiver or Transceiver Power-Off Input Current	V_A = 3.8 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V V_A = −1.4 V, V_B = 1.2V, 0 V ≤ V_{CC} ≤ 1.5 V	− −32	− −	32 −	μA
I_{BOFF}	Receiver or Transceiver Power-Off Input Current	V_B = 3.8 V, V_A = 1.2V, 0 V ≤ V_{CC} ≤ 1.5 V V_B = −1.4 V, V_A = 1.2V, 0 V ≤ V_{CC} ≤ 1.5 V	− −32	− −	32 −	μA
I_{ABOFF}	Receiver or Transceiver Power-Off Differential Input Current (I_{AOFF} – I_{BOFF})	V_A = V_B, 0 V ≤ V_{CC} ≤ 1.5 V, −1.4 V ≤ V_A ≤ 3.8 V	−4	−	4	μA
C_A	Transceiver with Driver Disabled Input Capacitance	V_A = 0.4 sin (30$e^{6\pi t}$) + 0.5 V, V_B = 1.2 V	−	5	−	pF
C_B	Transceiver with Driver Disabled Input Capacitance	V_B = 0.4 sin (30$e^{6\pi t}$) + 0.5 V, V_A = 1.2 V	−	5	−	pF
C_{AB}	Transceiver with Driver Disabled Differential Input Capacitance	V_{AB} = 0.4 sin (30$e^{6\pi t}$)	−	−	3	pF
$C_{A/B}$	Transceiver with Driver Disabled Input Capacitance Balance (C_A/C_B)		0.99	−	1.01	
DRIVER						
$\|V_{AB}\|$	Differential Output Voltage Amplitude (A, B)	(Figure 5)	480	−	650	mV
$\Delta\|V_{AB}\|$	Change in Differential Output Voltage Amplitude between Logic states (A, B)	(Figure 5)	−50	−	50	mV
$V_{OS(SS)}$	Steady State Common Mode Output Voltage (A, B)	(Figure 8)	0.7	−	1.1	V
$\Delta V_{OS(SS)}$	Change in Steady state Common Mode Output Voltage between Logic states (A, B)	(Figure 8)	−50	−	50	mV
$V_{OS(PP)}$	Peak to Peak Common Mode Output Voltage (A, B)	(Figure 8)	−	−	150	mV
V_{AOC}	Maximum Steady State Open Circuit Output Voltage (A, B)	(Figure 7)	0	−	2.4	V
V_{BOC}	Maximum Steady State Open Circuit Output Voltage (A, B)	(Figure 7)	0	−	2.4	V
$V_{P(H)}$	Voltage Overshoot Low to High Level Output (A, B)	(Figure 9)	−	−	1.2V_{SS}	V
$V_{P(L)}$	Voltage Overshoot High to Low Level Output (A, B)	(Figure 9)	−0.2V_{SS}	−	−	V
I_{IH}	High Level Input Current (D, DE)	V_{IH} = 2 V to V_{CC}	−	−	10	μA
I_{IL}	Low Level Input Current (D, DE)	V_{IL} = GND to 0.8 V	−	−	10	μA
$\|I_{OS}\|$	Differential Short Circuit Output Current Amplitude (A, B)	(Figure 6)	−	−	24	mA
C_I	Input Capacitance (D, DE)	V_I = 0.4 sin (30$e^{6\pi t}$) + 0.5 V	−	5	−	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
External DC Source when used for measurement to have low Ripple/Noise at board input.

Table 7. ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ±0.3 V, GND = 0 V, T_A −40°C to +85°C) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
RECEIVER						
V_{IT+}	+ve Going Differential Input Voltage Threshold (A,B)	Type 1 (Table 8) Type 2 (Table 9)	− −	− −	35 150	mV
V_{IT-}	−ve Going Differential Input Voltage Threshold (A,B)	Type 1 (Table 8) Type 2 (Table 9)	−35 50	− −	− −	mV
V_{HYS}	Differential Input Voltage Hysteresis [VIT+ − VIT−] (A,B)	Type 1 (Table 8) Type 2 (Table 9)	− −	25 0	− −	mV
V_{OH}	High Level Output Voltage (R)	I_{OH} = −8 mA	2.4	−	−	V
V_{OL}	Low Level Output Voltage (R)	I_{OL} = 8 mA	−	−	0.4	V
I_{IH}	High Level Input Current ($\overline{RE}$)	V_{IH} = 2 V to V_{CC}	−10	−	−	μA
I_{IL}	Low Level Input Current ($\overline{RE}$)	V_{IL} = GND to 0.8 V	−10	−	−	μA
I_{OZ}	High Impedance Output Current (R)	V_O = 0 V or V_{CC}	−10	−	15	μA
External DC Source when used for measurement to have low Ripple/Noise at board input.						
DRIVER SWITCHING						
t_{pLH}	Propagation Delay time, Low to High Level Output	(Figure 9)	1.3	1.9	2.4	ns
t_{pHL}	Propagation Delay time, High to Low Level Output	(Figure 9)	1.3	1.9	2.4	ns
t_r	Differential Output Signal Rise Time	(Figure 9)	0.9	−	2	ns
t_f	Differential Output Signal Fall Time	(Figure 9)	0.9	−	2.2	ns
$t_{SK(o)}$	Output Skew	(Figure 9)	−	−	200	ps
$t_{SK(pp)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	(Figure 9)	−	−	150	ps
$t_{SK(pp)}$	Device to Device Skew (Note 2)	(Figure 9)	−	−	300	ps
$T_{JIT(per)}$	Periodic Jitter RMS (1 Standard deviation) (Note 1)	125 MHz Clock Input, t_r = t_f = 0.5 ns (10% to 90%), Switching on All Channels (Figure 10)	−	−	2	ps
$T_{JIT(cc)}$	Cycle to Cycle Jitter RMS (Note 1)	125 MHz Clock Input, t_r = t_f = 0.5 ns (10% to 90%), Switching on All Channels (Figure 10)	−	−	9	ps
$T_{JIT(det)}$	Deterministic Jitter (Note 1)	Switching on All Channels, 250 Mbps 2^{15}−1 PRBS Input, t_r = t_f = 0.5 ns (10% to 90%) (Figure 10)	−	−	290	ps
$T_{JIT(r)}$	Random Jitter (Note 1)	Switching on All Channels, 250 Mbps 2^{15}−1 PRBS Input, t_r = t_f = 0.5 ns (10% to 90%) (Figure 10)	−	−	16	ps
t_{pZH}	Enable Time, High Impedance to High Level Output	(Figure 11)	−	−	7	ns
t_{pZL}	Enable Time, High Impedance to Low Level Output	(Figure 11)	−	−	7	ns
t_{pHZ}	Disable Time, High Level to High Impedance Output	(Figure 11)	−	−	7	ns
t_{pLZ}	Disable Time, Low Level to High Impedance Output	(Figure 11)	−	−	7	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Jitter is ensured by Design and characterization
2. $t_{SK(pp)}$ is the amplitude of the difference in propagation delay time between any specified terminals of two Devices that operates with same Power Supply Voltage, test circuits at same temperature and having identical packages.

Table 7. ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ±0.3 V, GND = 0 V, T_A −40°C to +85°C) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
RECEIVER SWITCHING						
t_{pLH}	Propagation Delay time, Low to High Level Output	C_L = 15 pF (Figure 12)	2.5	4.5	6.4	ns
t_{pHL}	Propagation Delay time, High to Low Level Output	C_L = 15 pF (Figure 12)	2.5	4.5	6.4	ns
t_r	Output Signal Rise Time	C_L = 15 pF (Figure 12)	1.4	−	2.65	ns
t_f	Output Signal Fall Time	C_L = 15 pF (Figure 12)	1.15	−	2.35	ns
$t_{SK(o)}$	Output Skew	C_L = 15 pF (Figure 12)	−	−	350	ps
$t_{SK(pp)}$	Pulse Skew ($\|t_{PHL} - t_{PLH}\|$) Type 1 Type 2	C_L = 15 pF (Figure 12)	 − −	 35 150	 210 700	ps
$t_{SK(pp)}$	Device to Device Skew (Note 2)	C_L = 15 pF (Figure 12)	−	−	800	ps
$T_{JIT(per)}$	Periodic Jitter RMS (1 Standard Deviation) (Note 1)	125 MHz Clock Input, $t_r = t_f$ = 0.5 ns (10% to 90%), Switching on All Channels (Figure 13)	−	−	6	ps
$T_{JIT(cc)}$	Cycle to Cycle Jitter RMS (Note 1)	125 MHz Clock Input, $t_r = t_f$ = 0.5 ns (10% to 90%), Switching on All Channels (Figure 13)	−	−	13	ps
$T_{JIT(det)}$	Deterministic Jitter (Note 1) Type 1 Type 2	Switching on All Channels, 250 Mbps $2^{15}-1$ PRBS Input, $t_r = t_f$ = 0.5 ns (10% to 90%) (Figure 13)	 − −	 − −	 800 945	ps
$T_{JIT(r)}$	Random Jitter (Note 1) Type 1 Type 2	Switching on All Channels, 250 Mbps $2^{15}-1$ PRBS Input, $t_r = t_f$ = 0.5 ns (10% to 90%) (Figure 13)	 − −	 − −	 90 65	ps
t_{pZH}	Enable Time, High Impedance to High Level Output	C_L = 15 pF (Figure 14)	−	−	15	ns
t_{pZL}	Enable Time, High Impedance to Low Level Output	C_L = 15 pF (Figure 14)	−	−	15	ns
t_{pHZ}	Disable Time, High Level to High Impedance Output	C_L = 15 pF (Figure 14)	−	−	10	ns
t_{pLZ}	Disable Time, Low Level to High Impedance Output	C_L = 15 pF (Figure 14)	−	−	10	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Jitter is ensured by Design and characterization
2. $t_{SK(pp)}$ is the amplitude of the difference in propagation delay time between any specified terminals of two Devices that operates with same Power Supply Voltage, test circuits at same temperature and having identical packages.

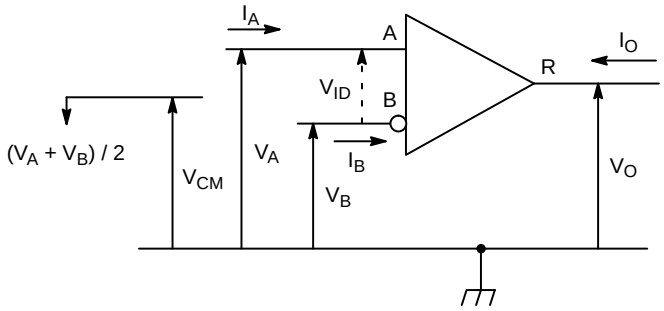


Figure 3. Receiver Voltage and Current Definitions

Table 8. TYPE 1 RECEIVER INPUT THRESHOLD TEST VOLTAGES

Applied Voltages		Resulting Differential Input Voltage	Resulting Common Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.365	0.035	3.3825	H
3.365	3.400	–0.035	3.3825	L
–0.965	–1.000	0.035	–0.9825	H
–1.000	–0.965	–0.035	–0.9825	L

*H = High Level, L = Low Level, Output State assumes Receiver is Enabled ($\overline{RE}$ = L)

Table 9. TYPE 2 RECEIVER INPUT THRESHOLD TEST VOLTAGES

Applied Voltages		Resulting Differential Input Voltage	Resulting Common Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.25	0.150	3.325	H
3.400	3.35	0.050	3.375	L
–0.850	–1.000	0.150	–0.925	H
–0.950	–1.000	0.050	–0.975	L

*H = High Level, L = Low Level, Output State assumes Receiver is Enabled ($\overline{RE}$ = L)

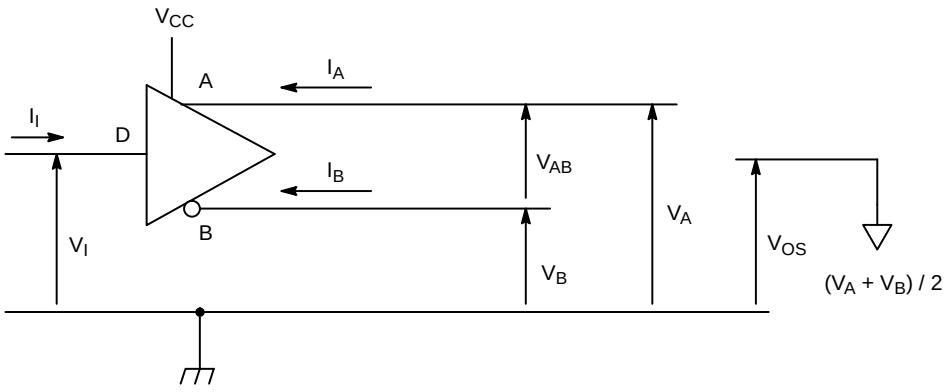


Figure 4. Driver Voltage and Current Definitions

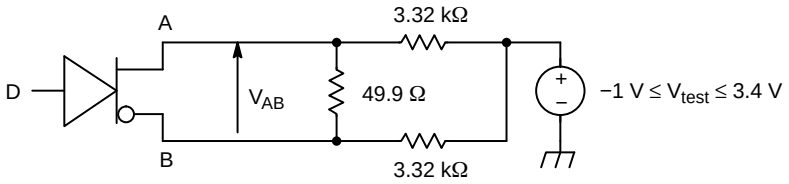


Figure 5. Differential Output Voltage Test Circuit

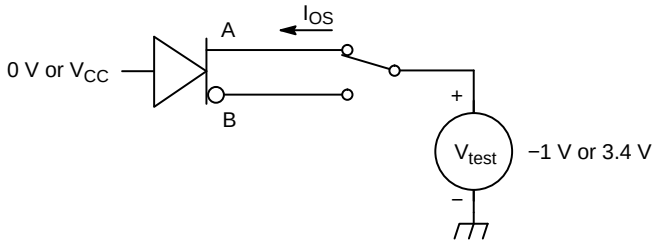


Figure 6. Driver Short-Circuit Test Circuit

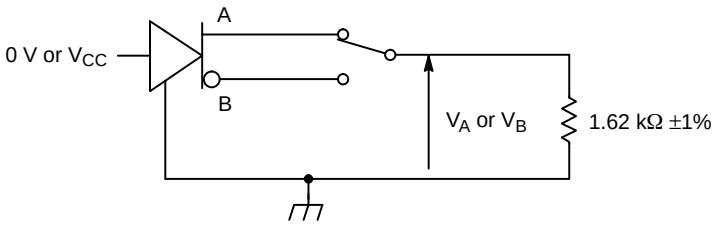
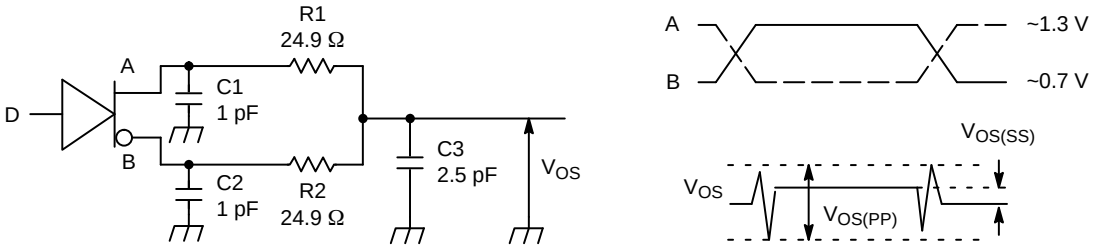
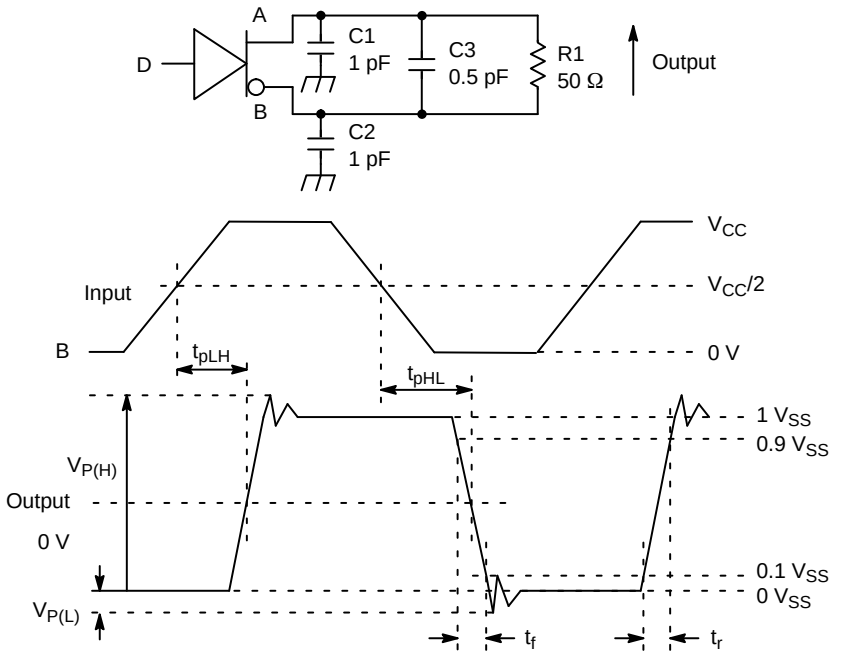


Figure 7. Maximum Steady State Output Voltage



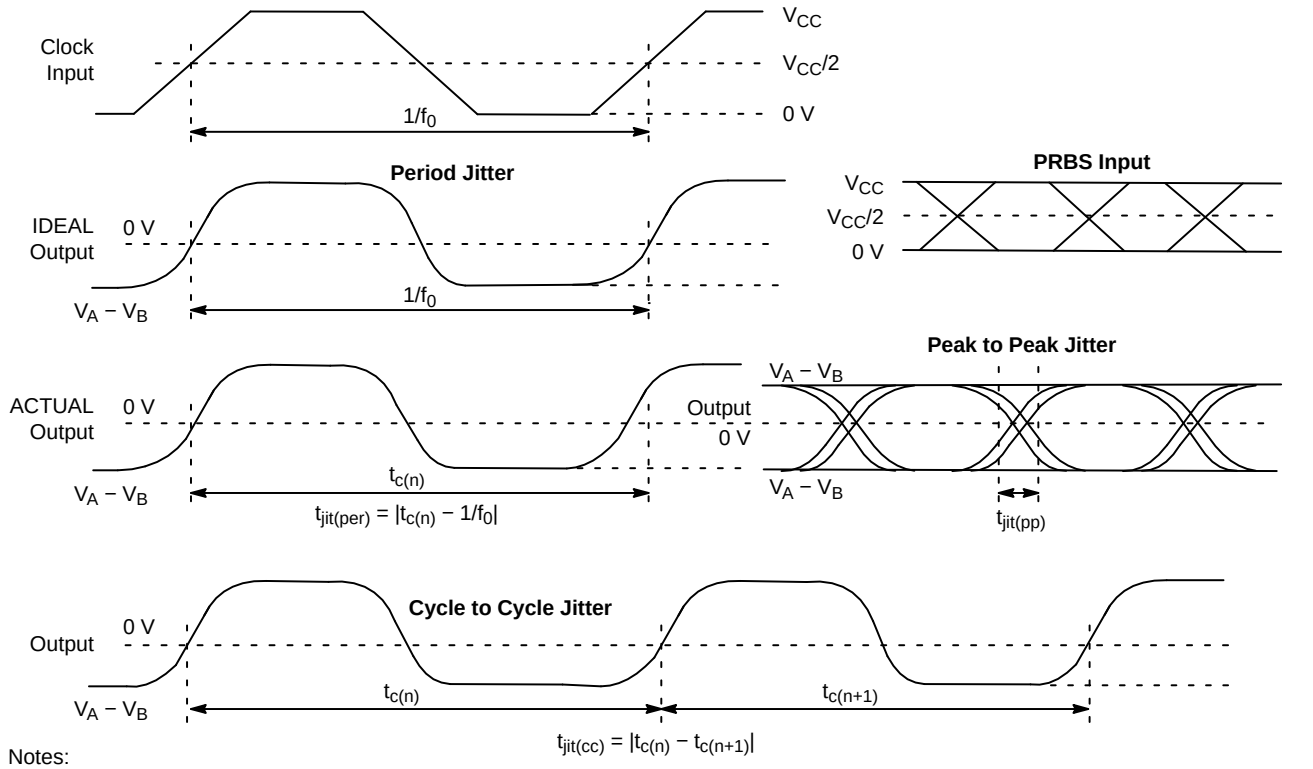
Notes:
1. All Input pulses are supplied by a Generator having characteristics as follows: t_r or $t_f \leq 1$ ns, pulse frequency = 1 MHz & Duty cycle = 50 ±5%.
2. Capacitor values indicated is inclusive of fixture and instrumentation Capacitance with 20 mm of the D.U.T. and are ±20%.
3. All Resistors are metal Film, Surface Mount, ±1% and located within 20 mm of the D.U.T.
4. The measurement of $V_{OS(pp)}$ is made on Test equipment with a –3 dB Bandwidth of at least 1 GHz.

Figure 8. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



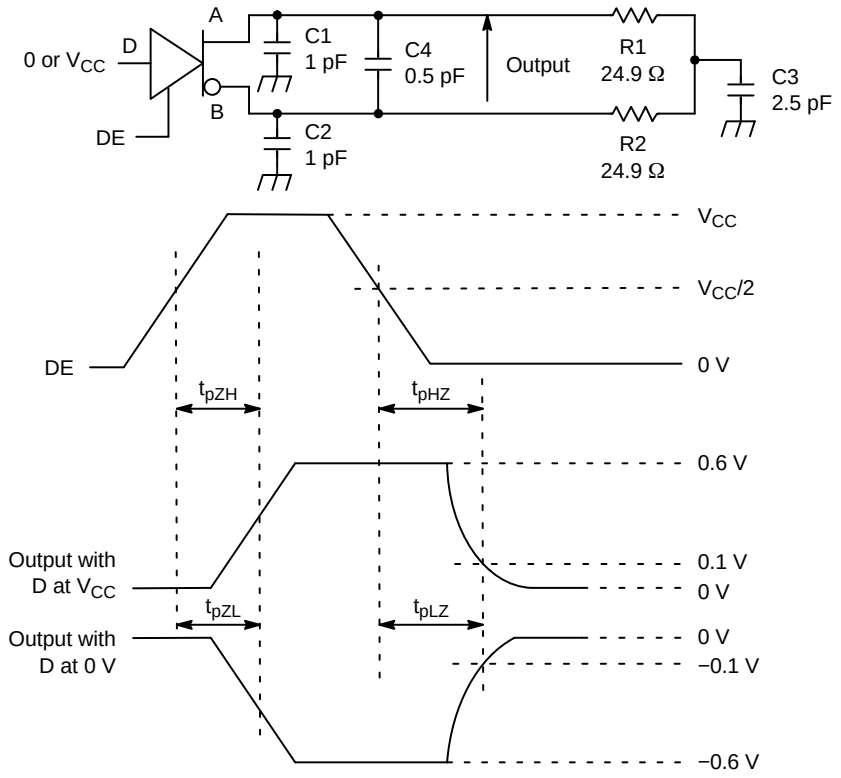
Notes:
1. All Input pulses are supplied by a Generator having characteristics as follows: t_r or $t_f \le 1$ ns, pulse frequency = 1 MHz & Duty cycle = 50 ±5%.
2. Capacitor values indicated is inclusive of fixture and instrumentation Capacitance with 20 mm of the D.U.T. and are ±20%.
3. All Resistors are metal Film, Surface Mount, ±1% and located within 20 mm of the D.U.T.
4. The measurement is made on Test equipment with a –3 dB Bandwidth of at least 1 GHz.

Figure 9. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



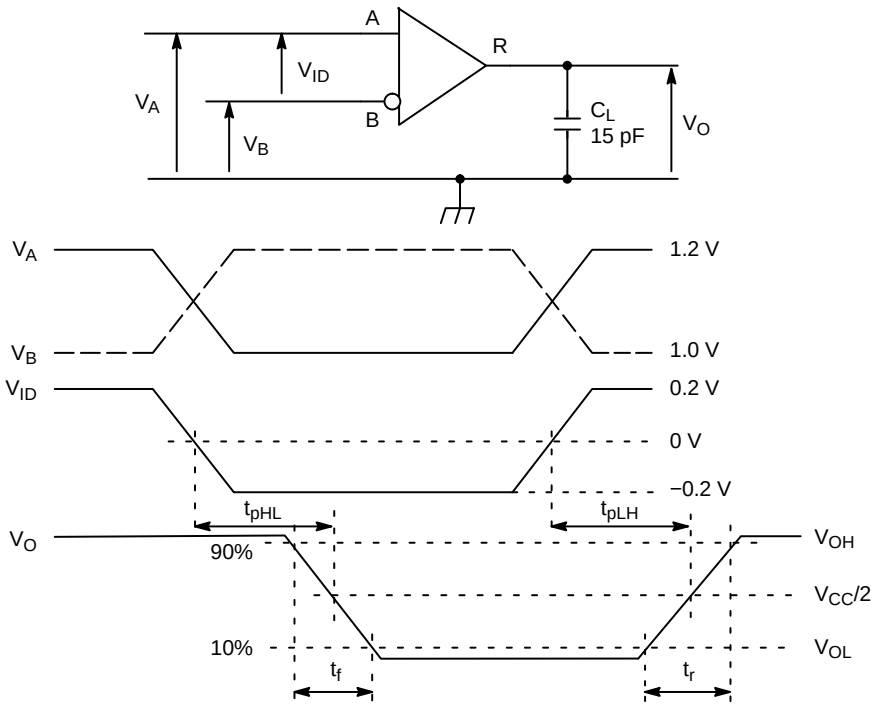
Notes:
1. Instrument used for generating Input Pulses and for Jitter measurement − Agilent 15433B BERT Stimulus, Tektronix DPO70804 running TDSJIT3 application software.
2. Period Jitter and Cycle to Cycle Jitter measured using a 125 MHz 50 ±1% Duty Cycle Clock Input over 75K samples.
3. Deterministic Jitter and Random Jitter are measured using 250 Mbps $2^{15} - 1$ PRBS Input, measured over BER = 10^{-12}

Figure 10. Driver Jitter Measurement Waveforms



Notes:
1. All Input pulses are supplied by a Generator having characteristics as follows: t_r or $t_f \le 1$ ns, pulse frequency = 1 MHz & Duty cycle = 50 ±5%.
2. Capacitor values indicated is inclusive of fixture and instrumentation Capacitance with 20 mm of the D.U.T. and are ±20%.
3. All Resistors are metal Film, Surface Mount, ±1% and located within 20 mm of the D.U.T.
4. The measurement is made on Test equipment with a –3 dB Bandwidth of at least 1 GHz.

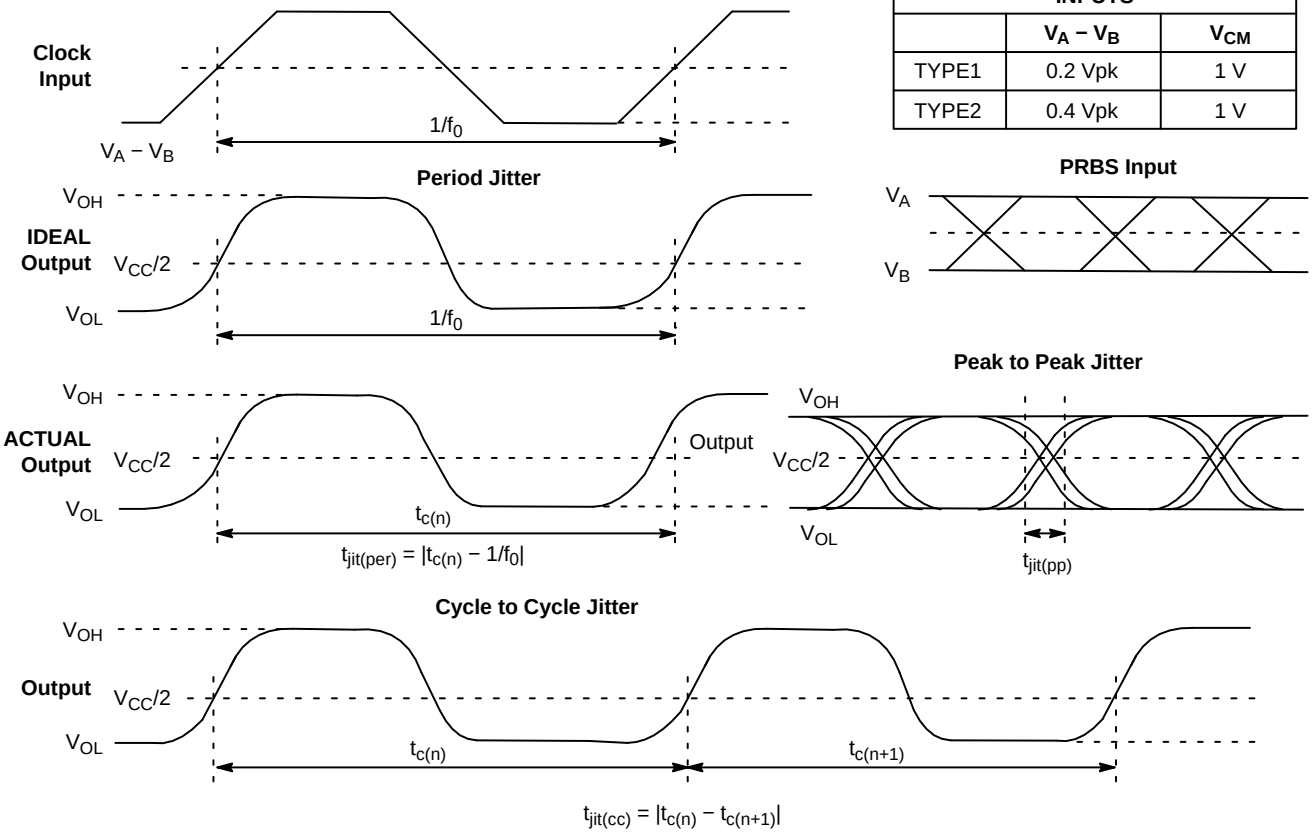
Figure 11. Driver Enable and Disable Time Circuit and Definitions



Notes:
1. All Input pulses are supplied by a Generator having characteristics as follows: t_r or $t_f \le 1$ ns, pulse frequency = 1 MHz & Duty cycle = 50 ±5%.
2. The measurement is made on Test equipment with a –3 dB Bandwidth of at least 1 GHz.

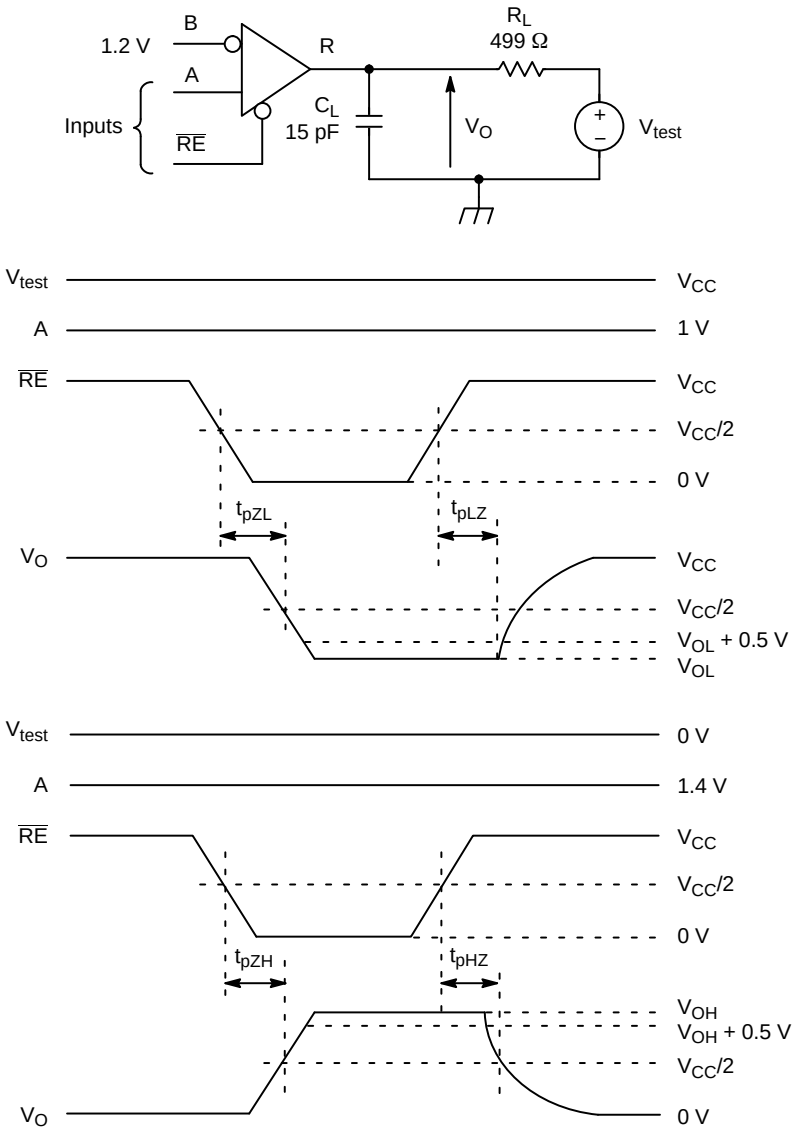
Figure 12. Receiver Timing Test Circuit Waveforms

INPUTS		
	$V_A - V_B$	V_{CM}
TYPE1	0.2 Vpk	1 V
TYPE2	0.4 Vpk	1 V



Notes:
1. Instrument used for generating Input Pulses and for Jitter measurement − Agilent 15433B BERT Stimulus, Tektronix DPO70804 running TDSJIT3 application software.
2. Period Jitter and Cycle to Cycle Jitter measured using a 125 MHz 50 ±1% Duty Cycle Clock Input over 75K samples.
3. Deterministic Jitter and Random Jitter are measured using 250 Mbps $2^{15} - 1$ PRBS Input, measured over BER = 10^{-12}

Figure 13. Receiver Jitter Measurement Waveforms



Notes:
1. All Input pulses are supplied by a Generator having characteristics as follows: t_r or $t_f \le 1$ ns, pulse frequency = 1 MHz & Duty cycle = 50 ±5%.
2. All Resistors are metal Film, Surface Mount, ±1% and located within 20 mm of the D.U.T.
3. C_L is combination of 20% tolerance low-loss Ceramic Surface Mount Capacitor and fixture Capacitance within 20 mm of the D.U.T.

Figure 14. Receiver Enable/Disable Time Test Circuit and Waveforms

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

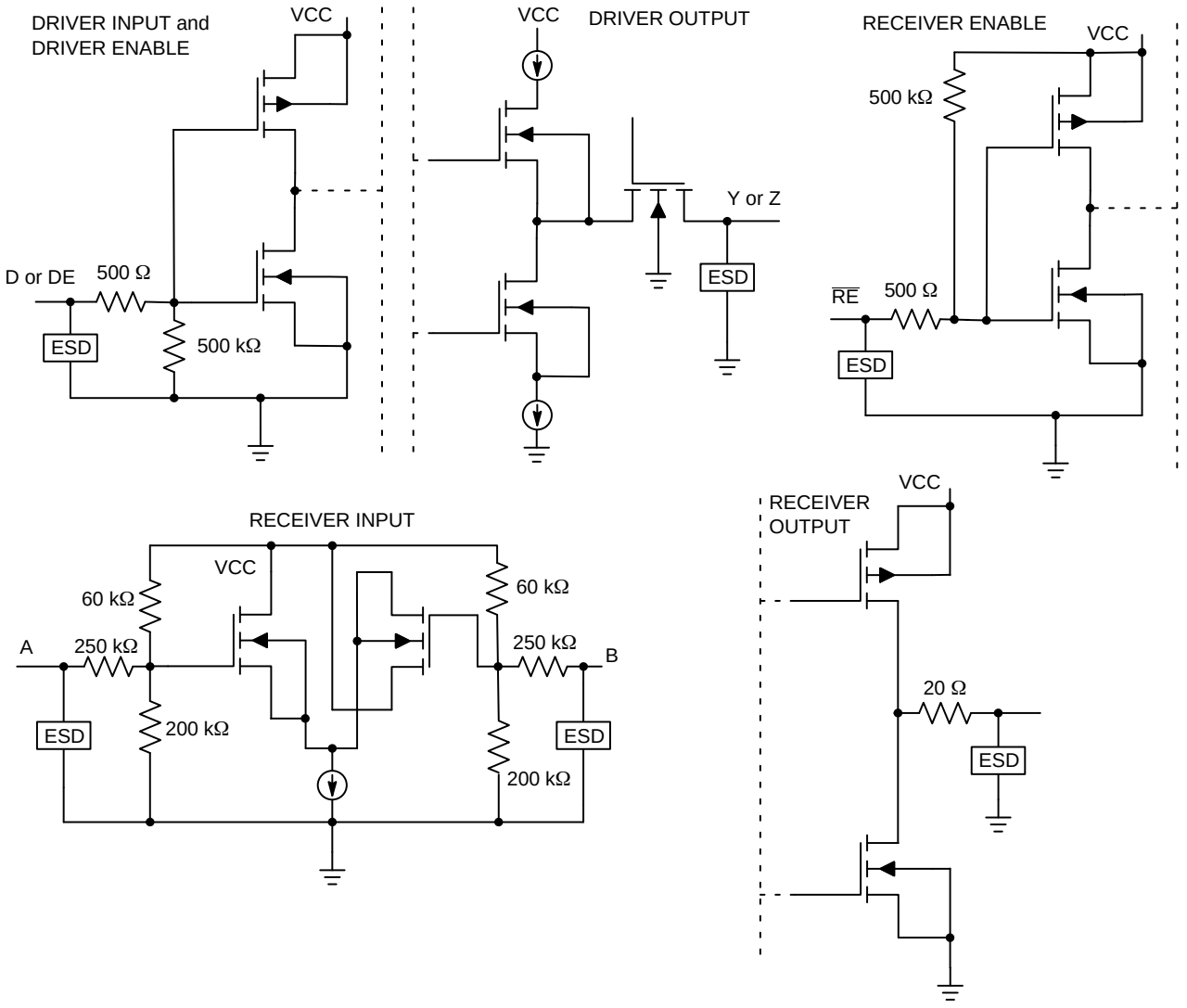


Figure 15. Input and Output Schematic Diagrams

ORDERING INFORMATION

Device	Package	Shipping†
NB3N401SMNTXG	QFN48 (Pb−Free)	2,500 / Tape & Reel

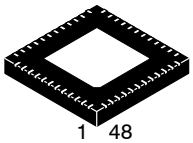
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

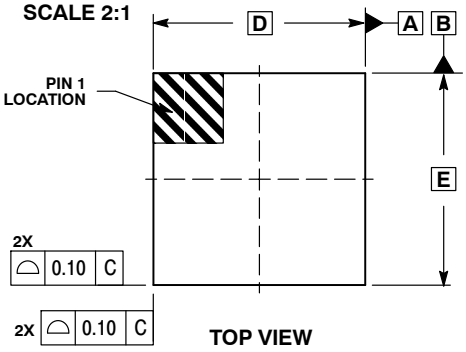
ON Semiconductor®

QFN48 7x7, 0.5P
CASE 485EP
ISSUE O

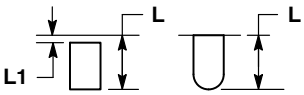
DATE 04 NOV 2015



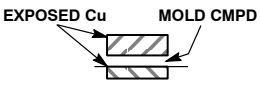
SCALE 2:1



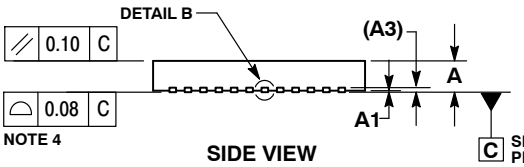
TOP VIEW



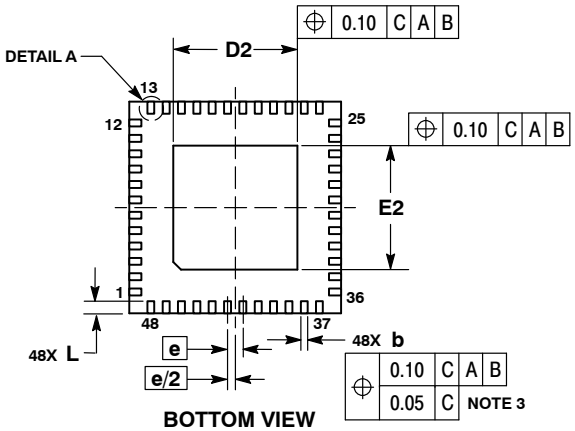
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

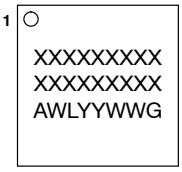


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	7.00 BSC	
D2	4.00	4.20
E	7.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
L1	0.00	0.15

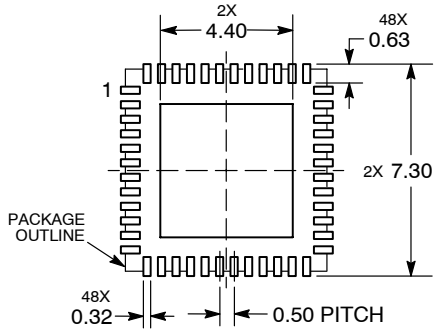
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**QFN48 7X7, 0.50P**	**PAGE 1 OF 1**

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