Preferred Devices

Power Management, Dual Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These are Pb-Free Devices

Rating

MAXIMUM RATINGS

	- ,				
$\mathbf{Q_1}$ (T _A = 25°C unless otherwise noted, common for Q ₁ and Q ₂)					
Collector-Base Voltage	V _{CBO}	50	Vdc		
Collector-Emitter Voltage	V _{CEO}	50	Vdc		
Collector Current	I _C	100	mAdc		
Electrostatic Discharge	ESD	HBM Class 1 MM Class B			

Symbol

Value

Unit

$Q_2 (T_A = 25^{\circ}C)$

Collector-Emitter Voltage	V_{CEO}	-12	Vdc
Collector-Base Voltage	V_{CBO}	-15	Vdc
Emitter-Base Voltage	V_{EBO}	-6.0	Vdc
Collector Current – Peak – Continuous	I _C	-1.0 (Note 1) -0.5	Adc
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^{\circ}C$ Derate above 25°C	P _D	357 (Note 2) 2.9 (Note 2)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	350 (Note 2)	°C/W
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^{\circ}C$	P _D	500 (Note 2) 4.0 (Note 2)	mW
Derate above 25°C		4.0 (Note 2)	mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA}	250 (Note 2)	°C/W

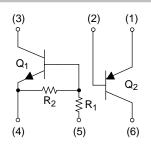
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. Single pulse 1.0 ms.
- 2. FR-4 @ Minimum Pad.



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SOT-563 CASE 463A PLASTIC

MARKING DIAGRAM



UY = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
EMF5XV6T5	SOT-563 (Pb-Free)	8000/Tape & Reel
EMF5XV6T5G	SOT-563 (Pb-Free)	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS ($T_A = 25$ °C unless otherwise noted, common for Q_1 and Q_2)

Characteristic			Min	Тур	Max	Unit
Q ₁ OFF CHARACTERISTICS						
Collector-Base Cutoff Current	$(V_{CB} = 50 \text{ V}, I_{E} = 0)$	I _{CBO}	_	-	100	nAdc
Collector-Emitter Cutoff Current	$(V_{CE} = 50 \text{ V}, I_{B} = 0)$	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current	$(V_{EB} = 6.0 \text{ V}, I_{C} = 0)$	I _{EBO}	-	-	0.1	mAdc
Collector-Base Breakdown Voltage	$(I_C = 10 \mu A, I_E = 0)$	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (N	ote 3) $(I_C = 2.0 \text{ mA}, I_B = 0)$	V _{(BR)CEO}	50	-	-	Vdc
ON CHARACTERISTICS (Note 3)						
DC Current Gain	$(V_{CE} = 10 \text{ V}, I_{C} = 5.0 \text{ mA})$	h _{FE}	80	140	-	
Collector-Emitter Saturation Voltage	$(I_C = 10 \text{ mA}, I_B = 0.3 \text{ mA})$	V _{CE(sat)}	-	-	0.25	Vdc
Output Voltage (on) $(V_{CC} = 5.0 \text{ V}, V_B = 3.5 \text{ V}, R_L = 1.0 \text{ k}\Omega)$		V _{OL}	-	-	0.2	Vdc
Output Voltage (off) $(V_{CC} = 5.0 \text{ V}, V_B = 0.5 \text{ V}, R_L = 1.0 \text{ k}\Omega)$		V _{OH}	4.9	-	-	Vdc
Input Resistor		R1	32.9	47	61.1	kΩ
Resistor Ratio		R1/R2	0.8	1.0	1.2	
Q ₂ OFF CHARACTERISTICS						
Collector - Emitter Breakdown Voltage	$(I_C = -10 \text{ mAdc}, I_B = 0)$	V _{(BR)CEO}	-12	-	-	Vdc
Collector - Base Breakdown Voltage	$(I_C = -0.1 \text{ mAdc}, I_E = 0)$	V _{(BR)CBO}	-15	-	-	Vdc
Emitter – Base Breakdown Voltage $(I_E = -0.1 \text{ mAdc}, I_C = 0)$		V _{(BR)EBO}	-6.0	-	-	Vdc
Collector Cutoff Current $(V_{CB} = -15 \text{ Vdc}, I_E = 0)$		I _{CBO}	-	-	-0.1	μAdc
Emitter Cutoff Current	$(V_{EB} = -6.0 \text{ Vdc})$	I _{EBO}	-	-	-0.1	μAdc
ON CHARACTERISTICS						
DC Current Gain (Note 4)	$(I_C = -10 \text{ mA}, V_{CE} = -2.0 \text{ V})$	h _{FE}	270	-	680	
Collector - Emitter Saturation Voltage (N	ote 4) $(I_C = -200 \text{ mA}, I_B = -10 \text{ mA})$	V _{CE(sat)}	_	-	-250	mV
Base-Emitter Saturation Voltage (Note	4) $(I_C = -150 \text{ mA}, I_B = -20 \text{ mA})$	V _{BE(sat)}	_	-0.81	-0.90	V
Base-Emitter Turn-on Voltage (Note 4)	$(I_C = -150 \text{ mA}, V_{CE} = -3.0 \text{ V})$	V _{BE(on)}	-	-0.81	-0.875	V
Input Capacitance	$(V_{EB} = 0 \text{ V, f} = 1.0 \text{ MHz})$	C _{ibo}	-	52	-	pF
Output Capacitance	$(V_{CB} = 0 \text{ V, f} = 1.0 \text{ MHz})$	C _{obo}	-	30	-	pF
Turn–On Time $(I_{BI} = -50 \text{ mA}, I_{C} = -500 \text{ mA}, R_{L} = 3.0 \Omega)$		t _{on}	_	50	-	ns
Turn-Off Time (I _{B1} = I	$B_2 = -50 \text{ mA}, I_C = -500 \text{ mA}, R_L = 3.0 \Omega$	t _{off}	-	80	-	ns

Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
 Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

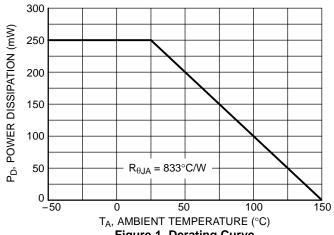


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS FOR Q1

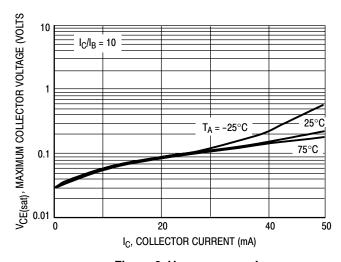


Figure 2. V_{CE(sat)} versus I_C

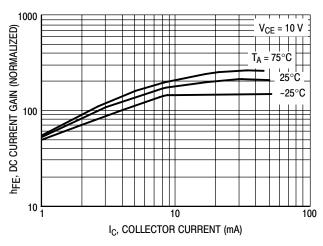


Figure 3. DC Current Gain

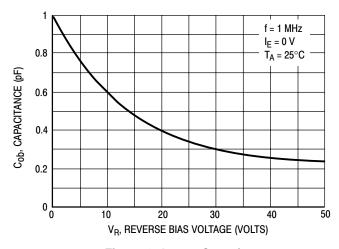


Figure 4. Output Capacitance

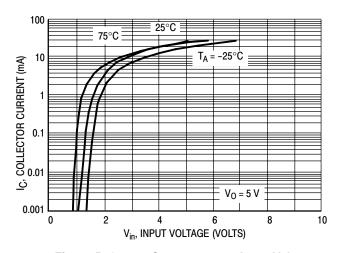


Figure 5. Output Current versus Input Voltage

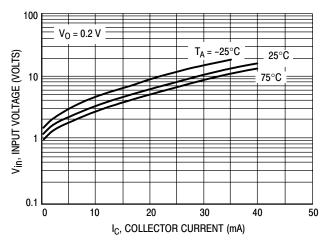


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS FOR Q2

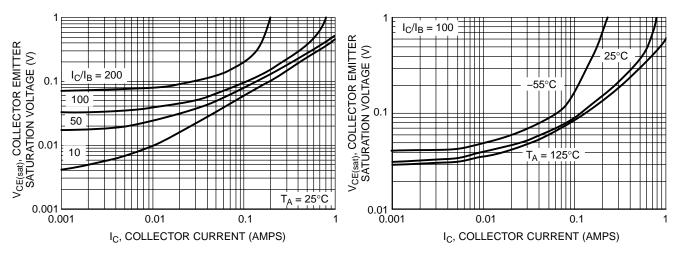


Figure 7. Collector Emitter Saturation Voltage vs. Collector Current

Figure 8. Collector Emitter Saturation Voltage vs. Collector Current

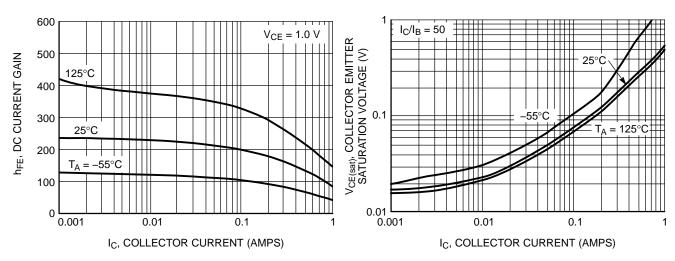


Figure 9. DC Current Gain

Figure 10. Collector Emitter Saturation Voltage vs. Collector Current

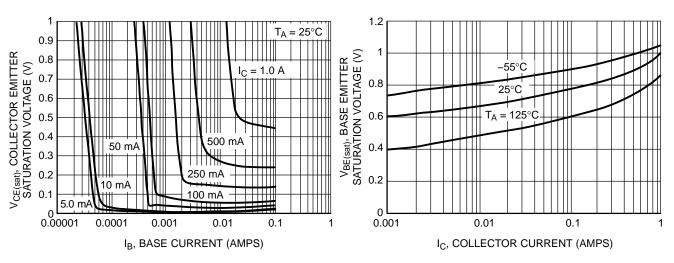


Figure 11. Collector Emitter Saturation Voltage vs Base Current

Figure 12. Base Emitter Saturation Voltage vs.
Collector Current

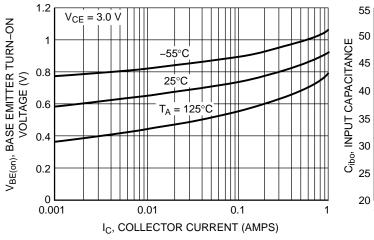


Figure 13. Base Emitter Turn-On Voltage vs.
Collector Current

Figure 14. Input Capacitance

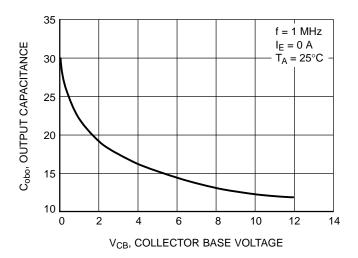


Figure 15. Output Capacitance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



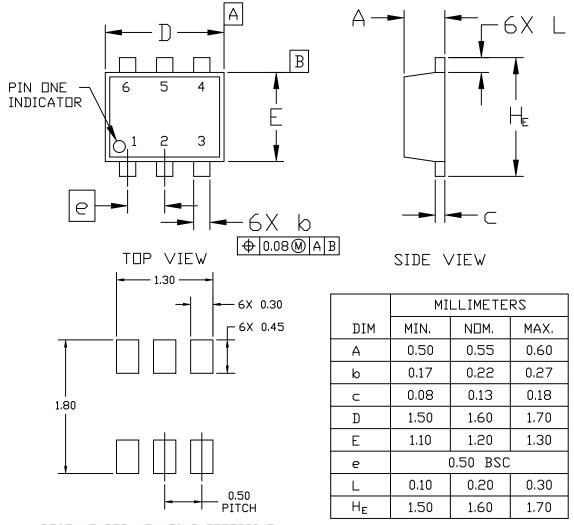


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DATE 26 JAN 2021

NOTES:

- I. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



RECOMMENDED MOUNTING FOOTPRINT*

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

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2

1

DATE 26 JAN 2021

STYLE 1: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1	STYLE 2: PIN 1. EMITTER 1 2. EMITTER 2 3. BASE 2 4. COLLECTOR 2 5. BASE 1 6. COLLECTOR 1	STYLE 3: PIN 1. CATHODE 1 2. CATHODE 1 3. ANODE/ANODE 4. CATHODE 2 5. CATHODE 2 6. ANODE/ANODE
STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 5: PIN 1. CATHODE 2. CATHODE 3. ANODE 4. ANODE 5. CATHODE 6. CATHODE	STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 7: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. ANODE 6. CATHODE	STYLE 8: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SDURCE 5. DRAIN 6. DRAIN	STYLE 9: PIN 1. SDURCE 1 2. GATE 1 3. DRAIN 2 4. SDURCE 2 5. GATE 2 6. DRAIN 1
STYLE 10: PIN 1. CATHODE 1 2. N/C 3. CATHODE 2 4. ANODE 2 5. N/C 6. ANODE 1	STYLE 11: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	

GENERIC MARKING DIAGRAM*



XX = Specific Device CodeM = Month Code= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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