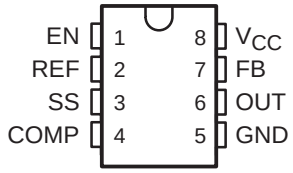
- **Pin-for-Pin Compatible With MAX734**
- **Programming Voltage for Flash Memory**
- **2.7-V to 11-V Input Operating Range**
- **Output Current of 120 mA or Greater From 3.75-V or Higher Input**
- **3-μA Maximum Supply Current in Shutdown**
- **Only 5 External Components Required**
- **High Efficiency . . . 85% Typical (5-V Input, 120-mA Output)**
- **8-Pin SOIC and DIP Packages**
- **–40°C to 85°C Free-Air Operating Temperature Range**

D OR P PACKAGE
(TOP VIEW)



description

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 3.75 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut down the converter and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use.

High efficiency at low supply voltages and low supply current in shutdown make the TPS6734 particularly attractive for flash memory programming supplies, PCMCIA cards, and operational amplifiers in battery-powered equipment. The TPS6734 is available in 8-pin DIP and SOIC packages and operates over a free-air temperature range of –40°C to 85°C.

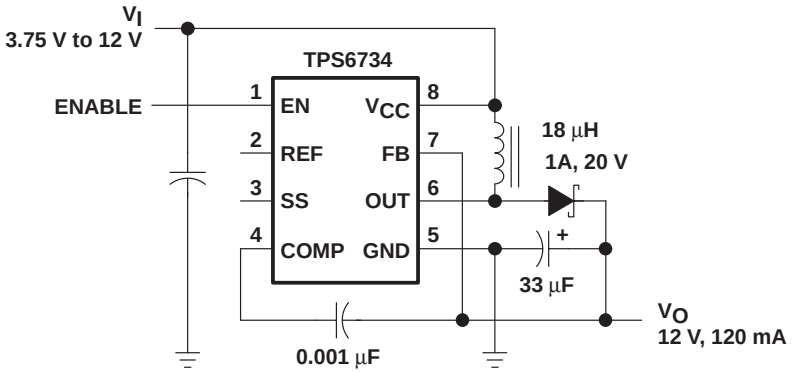


Figure 1. Typical Operating Circuit

AVAILABLE OPTIONS

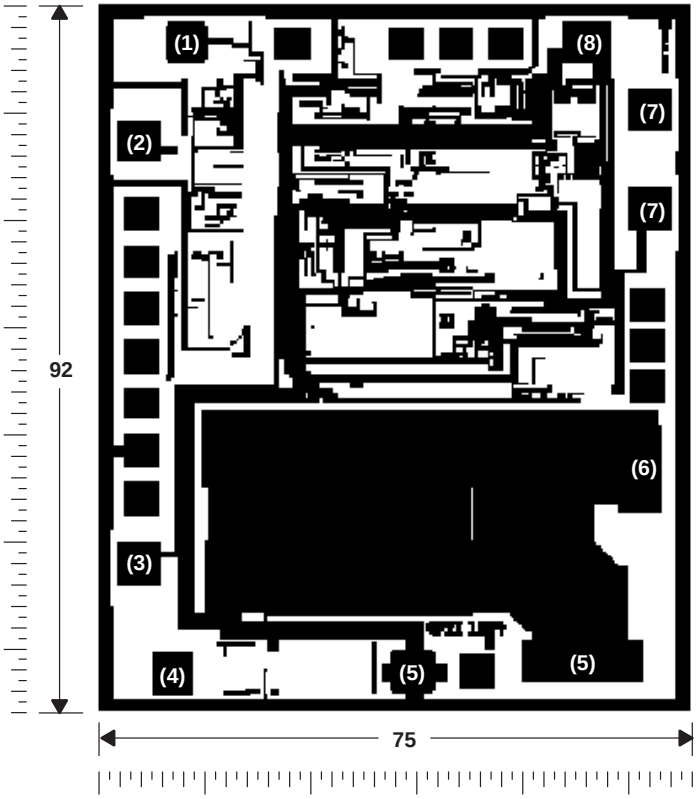
T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
–40°C to 85°C	TPS6734ID	TPS6734IP

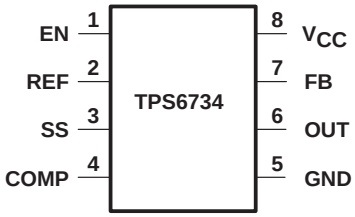
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TPS6734IDR).

TPS6734 chip information

Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pad. Chips can be mounted with conductive epoxy or a gold-silicon preform. Contact factory for die sales.

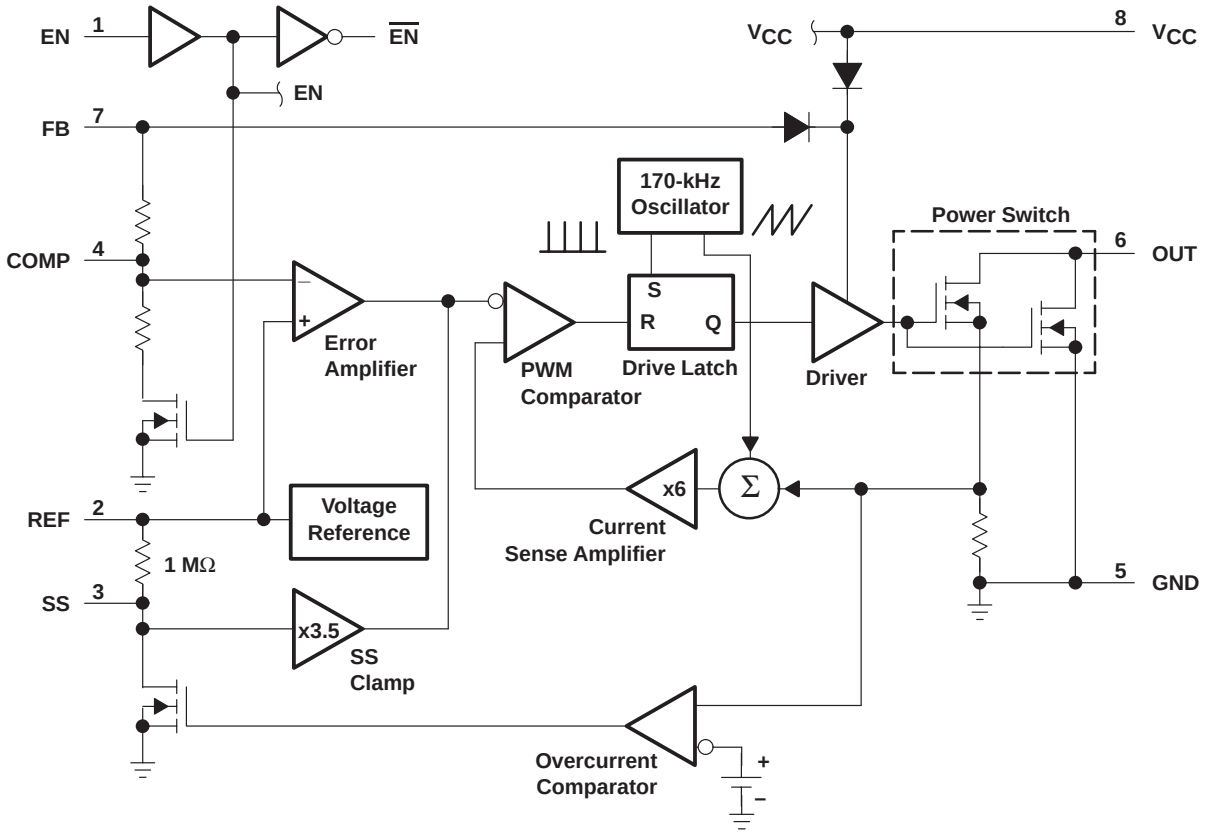
BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL
BONDING PADS: 4X4 MINIMUM
$T_J$max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
EN	1	Enable. EN ≥ 2 V turns on the TPS6734. EN ≤ 0.4 V turns it off and reduces the supply current to 3 μA max.
REF	2	1.22-V reference voltage output. REF can source 100 μA for external loads.
SS	3	Soft Start. A capacitor between SS and GND brings the output voltage up slowly at power-up.
COMP	4	Compensation connection. A 0.001-μF capacitor between COMP and FB stabilizes the feedback loop.
GND	5	Ground
OUT	6	N-channel MOSFET drain connection
FB	7	Feedback voltage. FB is connected to the converter output for the feedback loop.
V_{CC}	8	Supply voltage input

detailed description

The following descriptions refer to the functional block diagram.

reference

The internal 1.22-V reference is brought out on REF and can source 100 μA maximum to external loads. A 0.01-μF to 0.1-μF decoupling capacitor connected between REF and GND is recommended to minimize noise pickup.

oscillator and ramp generator

The oscillator circuit provides a 170-kHz clock, to set the converter operating frequency, and a timing ramp for slope compensation. The clock waveform is a pulse, a few hundred nanoseconds in duration, that is used to limit the maximum power-switch duty cycle to 95%. The timing ramp is summed with the current-sense signal at the input to the current-sense amplifier.

driver latch

The latch, which consists of a set/reset flip-flop and associated logic, is used to control the state of the power switch by turning the driver on and off. A high output from the latch turns the switch on; a low output from the latch turns it off. In normal operation, the flip-flop is set high during the clock pulse, but gating keeps the latch output low until the clock pulse is over. The latch is reset when the PWM comparator output goes high.

current-sense amplifier

The current-sense amplifier has a fixed gain of 6. It amplifies the slope-compensated current-sense voltage (a summation of the voltage on the current-sense resistor and the oscillator ramp) and feeds it to the PWM comparator.

error amplifier

The error amplifier is a high-gain differential amplifier used to regulate the converter output voltage. The amplifier generates an error signal, which is fed to the PWM comparator. The error signal is generated when a sample of the output voltage is compared to the internal reference and the difference is amplified. The output sample is obtained from a resistive divider connected between FB and GND. FB is externally connected to the converter output, and the divider output is connected to both the error amplifier input and COMP. A 0.001-μF capacitor connected between FB and COMP stabilizes the voltage control loop.

PWM comparator

The PWM comparator resets the drive latch and turns off the power switch whenever the slope-compensated current-sense signal from the current-sense amplifier exceeds the error signal.

power switch

The power switch is a 0.7-Ω n-channel MOSFET with current-sensing. The drain is connected to OUT and the current sense is connected to a resistor. The voltage across the resistor is proportional to the current in the power switch and is tied to the overcurrent comparator and the current-sense amplifier. In normal operation, the power switch is turned on at the start of each clock cycle and turned off when the PWM comparator resets the drive latch.

SS clamp

The SS (soft-start) clamp circuit limits the signal level on error-amplifier output during start-up. The voltage on SS is amplified and used to momentarily override the error-amplifier output until it rises above that output, at which point the error-amplifier takes over. This prevents the input to the PWM comparator from exceeding its common-mode range (the error-amplifier output too high to be reached by the current ramp) by limiting the maximum voltage on the error-amplifier output during start-up.

soft start

Soft start causes the output voltage to increase to the regulation point at a controlled rate of rise. The voltage on the charging soft-start capacitor gradually raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by increasing the current-limit threshold on a cycle-by-cycle basis. Even if SS has no capacitor installed, some distributed capacitance will always be present. A soft-start cycle is initiated when either the enable signal (EN) is switched high, or an overcurrent fault condition triggers the discharge of the soft-start capacitor.

overcurrent comparator

The overcurrent comparator monitors the current in the power switch. The comparator trips and initiates a soft-start cycle if the power-switch current exceeds 1.5-A peak. On each clock cycle, the power switch turns on and attempts to deliver current until the overcurrent limits are exceeded.

enable (EN)

A logic low on EN puts the TPS6734 in shutdown mode. In shutdown, the output power switch, voltage reference, and other functions are shut off, the supply current is reduced to 3 μA maximum, and the soft-start capacitor is discharged through a 1-MΩ resistance. The output voltage falls to a diode drop below the input voltage because of the current path from input to output through the inductor and diode.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Pin voltages: V_{CC}, OUT (see Note 1) . . . . . –0.3 V to 15 V
SS, COMP, EN (see Note 1) . . . . . –0.3 V to V_{CC}+ 0.3 V
Peak switch current . . . . . 1.5 A
Reference current . . . . . 2.5 mA
Continuous power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 s . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network terminal ground.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage	2.7	5	12	V
Compensation capacitor		0.001		µF
Output current at REF	0		100	µA
Reference capacitor		0.01		µF
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, $I_{O(LOAD)}$ = 0 mA, EN = 5 V, typical values are at T_A = 25°C (unless otherwise noted) (refer to circuit shown in Figure 13)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current	Operating	Entire circuit		1.2	2.5	mA
	Standby	EN = 0.4 V, entire circuit			3	µA
		EN = 0.4 V, into V_{CC}			3	µA
High-level input threshold voltage at EN			2			V
Low-level input threshold voltage at EN					0.4	V
Shutdown input leakage current at EN			–1		1	µA
On resistance at OUT		Current at OUT = 500 mA		0.7		Ω
Leakage current at OUT		V_{DS} = 12 V		1		µA
Reference voltage				1.22		V
Reference drift		T_A = –40°C to 85°C		6.7		ppm/°C
Oscillator frequency				170		kHz
Compensation pin impedance				7500		Ω

performance characteristics over recommended operating free-air temperature range, typical circuit connected as shown in Figure 13, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output voltage	V_{CC} = 4.75 V,	0 mA < $I_{O(LOAD)}$ < 120 mA	11.64	12.12	12.6	V
Load current	V_{CC} = 3.75 V		120	150		mA
	V_{CC} = 3.0 V,	Figure 11		150		
Line regulation	V_{CC} = 5 V to 12 V,	$I_{O(LOAD)}$ = 50 mA		0.20%		
Load regulation	$I_{O(LOAD)}$ = 0 mA to 120 mA			0.0042%		
Efficiency	V_{CC} = 5 V,	$I_{O(LOAD)}$ = 120 mA		86%		

TYPICAL CHARACTERISTICS

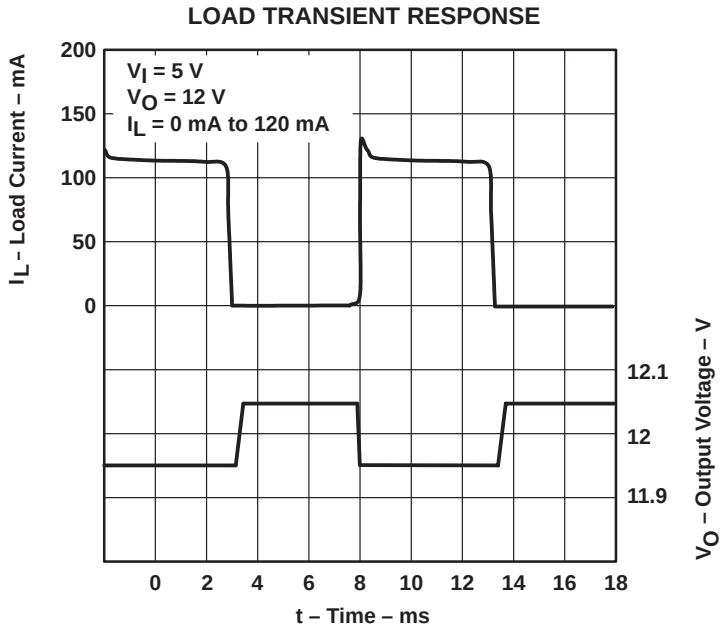


Figure 2

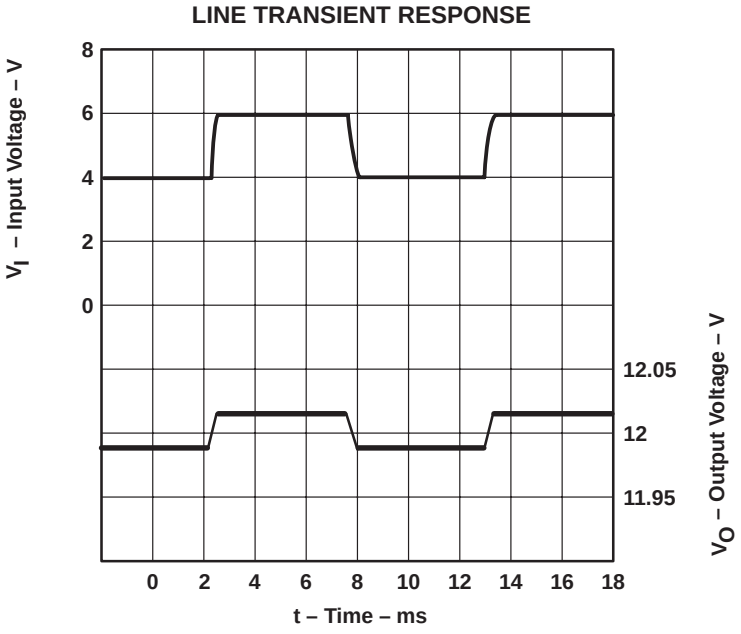


Figure 3

TYPICAL CHARACTERISTICS

EN RESPONSE TIME

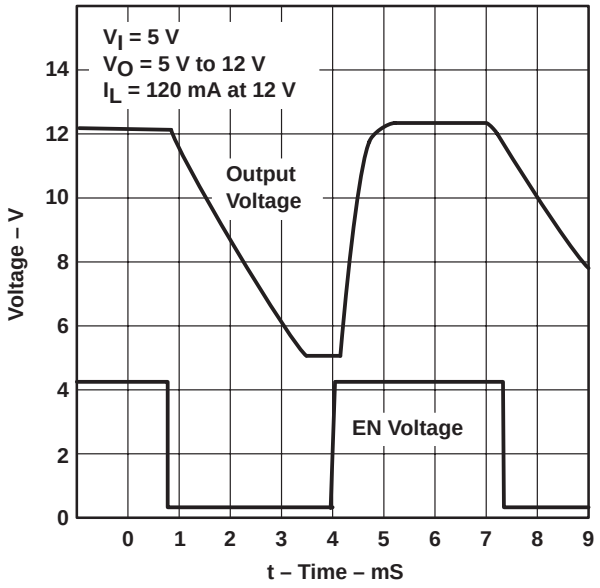


Figure 4

OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

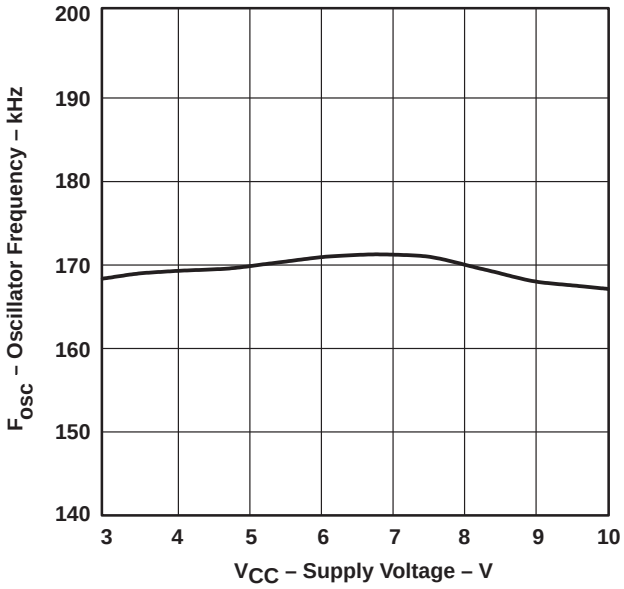


Figure 5

INPUT SUPPLY CURRENT vs SUPPLY VOLTAGE

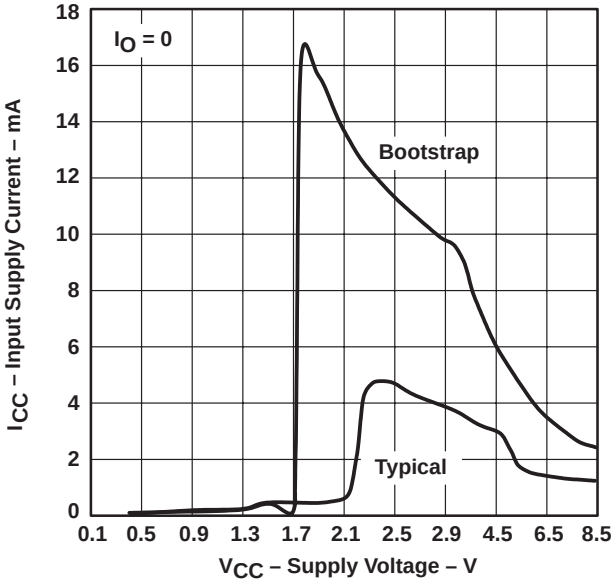


Figure 6

MAXIMUM OUTPUT CURRENT vs SUPPLY VOLTAGE

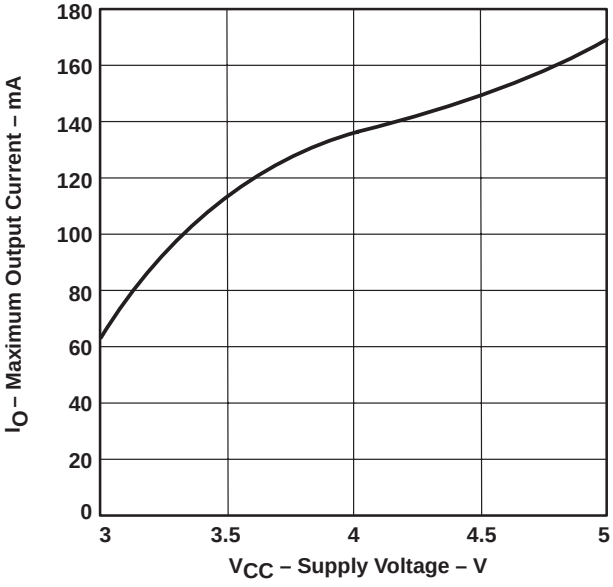


Figure 7

APPLICATION INFORMATION

The TPS6734 operates in a boost circuit as shown in Figures 1 and 11. Figure 1 shows the typical application circuit, which generates 12 V from a nominal 5-V source. The circuit is ideal for processor interface for energy management, because EN can be controlled by logic signals to place the 12-V source into the shutdown mode (3-μA current drain) when 12 V is not needed. An example of such an application is a flash memory device that requires 12 V for the erase cycle.

discontinuous mode

The circuit shown in Figure 1 operates in discontinuous mode over most of the range of input voltage and output current. In discontinuous mode, current through the inductor begins at zero, rises to a peak value, then ramps down to zero each cycle as shown by the voltage and current waveforms in Figure 8. The ringing in the voltage waveform on OUT results from a resonance between the inductor and the power switch capacitance and is normal for discontinuous operation.

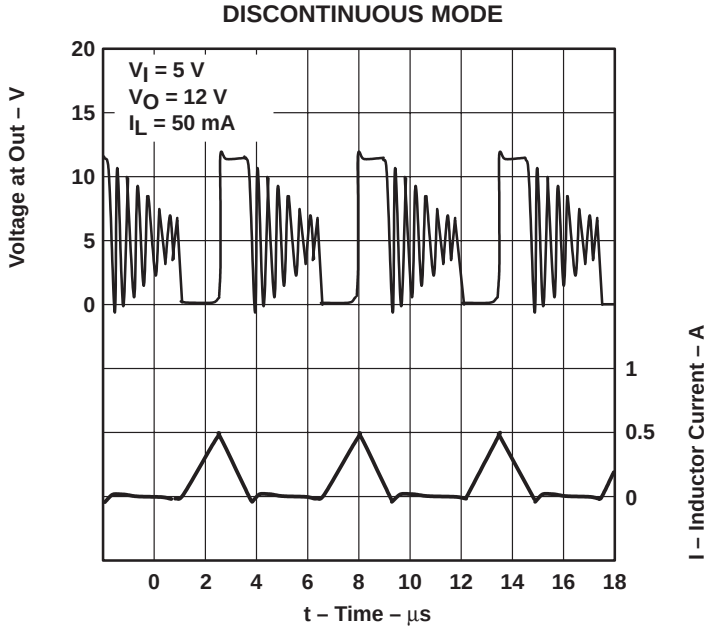


Figure 8

APPLICATION INFORMATION

continuous mode

When the converter is delivering heavy loads from low voltage sources, it operates in continuous mode. As shown in Figure 9, the inductor current does not drop to zero and the ringing is gone from the OUT voltage waveform.

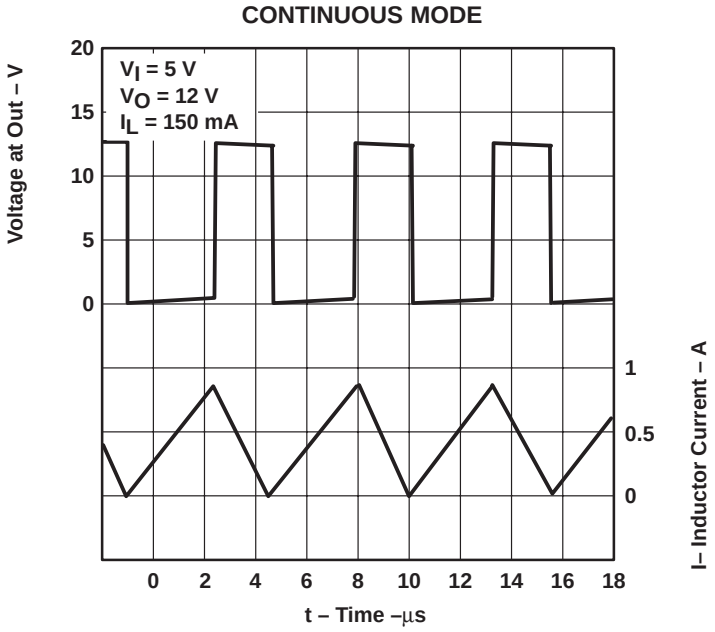


Figure 9

pulse-skipping mode

At very light load currents, the TPS6734 cannot generate drive pulses sufficiently narrow to maintain regulation and operate at 170 kHz. Under these circumstances, the converter operates in a pulse-skipping mode, in which cycles are skipped. In pulse-skipping mode, the waveforms are irregular and the output ripple contains a low-frequency component that may exceed 50 mV peak-to-peak.

APPLICATION INFORMATION

efficiency

Typical efficiency for the converter circuit shown in Figure 13 is plotted in Figure 10. The efficiency falls off rapidly at very light currents because the supply current is a significant percentage of the load.

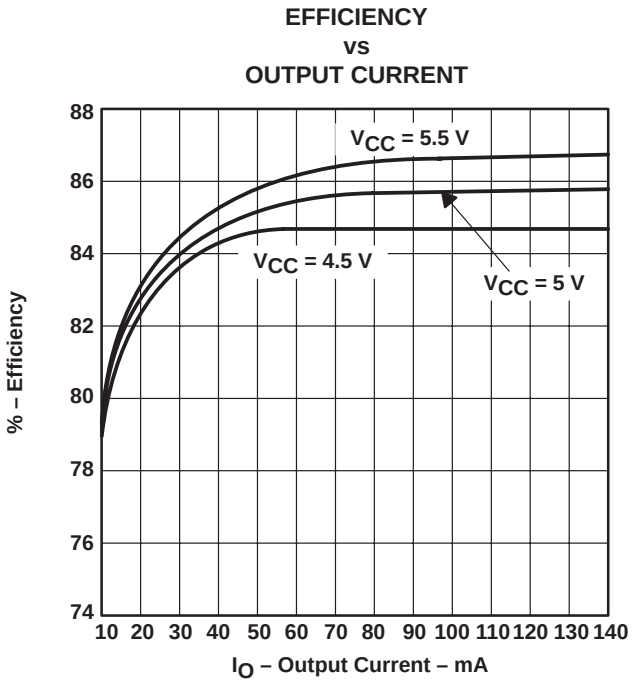


Figure 10

inductor selection

Inductance value is directly proportional to the input voltage and inversely proportional to the output power. The 18 μH shown in the typical circuit is the proper value for operation from 5-V sources up to 2-W loads. A lower inductance value should be used when operating from 3-V sources. Operation from 7 V and higher sources may require inductance values greater than 18 μH. The inductor's saturation current rating should be greater than three times the dc load current for 5-V inputs and five times the dc load for 3-V inputs.

output filter capacitor selection

The output filter capacitor should be selected for minimum ESR (equivalent series resistance). Capacitor ESR $\times$ ΔI_L (change in inductor current) determines the amplitude of the high-frequency ripple on the output voltage. The ESR of the capacitor should be less than 0.25 Ω to keep the output ripple less than 50 mV peak-to-peak over the entire current range (using 18-μH inductor).

diode

A Schottky diode or a high-speed silicon rectifier should be used. The continuous current rating of the diode should be at least 300 mA for full load (120 mA) operation.

APPLICATION INFORMATION

soft-start capacitor

Soft-start timing is controlled by the value of the SS capacitor. Table 1 lists soft-start time intervals for selected capacitor values and circuit conditions. If the circuit starts up with no load (e.g. in flash-memory programming supplies), no soft start is needed. Omitting the soft-start capacitor provides a minimum output-voltage rise time from the shutdown state, improving the output start-up time.

Table 1. Typical Soft-Start Times

SUPPLY VOLTAGE (V)	SOFT-START TIME† (ms) VERSUS CAPACITANCE (μF)				
	NO. CAP	0.047	0.1	0.47	1.0
5	0.70	22	42	220	400
7	0.46	15	37	185	225
9	0.38	10	17	88	155

† Soft-start times are ±35%

printed-circuit layout

Printed-circuit-board (PCB) layout is critical to quiet operation. A ground plane is recommended. Special attention should be given to minimizing the lengths of the switching loops. The first loop is formed by OUT, the diode, the output capacitor, and GND, the length of which can be minimized by connecting the anode of the diode close to OUT. The output capacitor should be connected directly between the diode cathode and GND with the shortest possible path. The second loop is formed by OUT, the inductor, the input capacitor, and GND. This loop is less critical than the first; however, the connection of OUT, the inductor and the anode of the diode must be minimized. Bypass capacitors should be located as close to the device as possible to prevent instability and noise pickup. If a large V_{CC}-to-GND bypass capacitor cannot be placed adjacent to the IC pins, the pins should be bypassed directly with a small ceramic capacitor (e.g., 0.1 μF). The recommended layout, shown in Figures 14 through 17, can provide guidance for PCB configuration (the ground plane beneath the TPS6734 and the short loops should be noted).

Plastic plug-in-type proto boards, or any construction scheme that allows long leads and the possibility of noise pickup, should not be used when assembling a breadboard or prototype application circuit implementing the TPS6734.

APPLICATION INFORMATION

bootstrapped output circuit

For operation below 2.7 V, the TPS6734 may be connected in a bootstrap configuration as shown in Figure 11. The bootstrap configuration is less efficient (requires more supply current and suffers a loss in efficiency at voltages below 5 V; see Figure 12) and is not recommended except for very low voltage operating conditions. Because the output-driver stage, which benefits most from higher voltages, is diode-coupled to the output voltage (see Figure 2), the bootstrapped configuration provides no benefit except at very low voltages. In the shutdown mode (EN = low), no-load quiescent current is unchanged (3 μA max) whether in the bootstrap or the typical configuration.

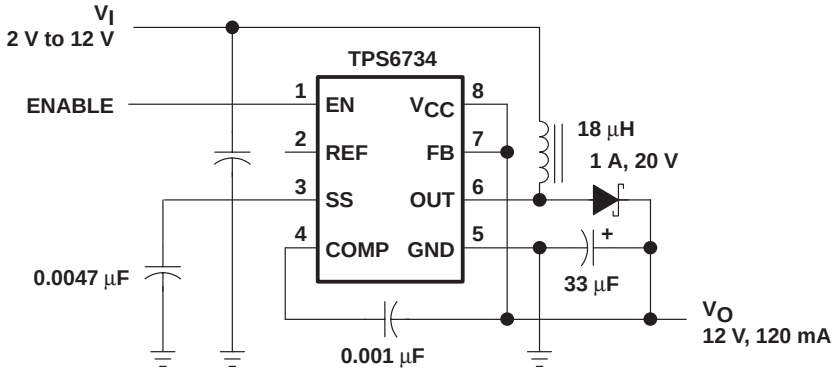


Figure 11. TPS6734 Bootstrap Configuration

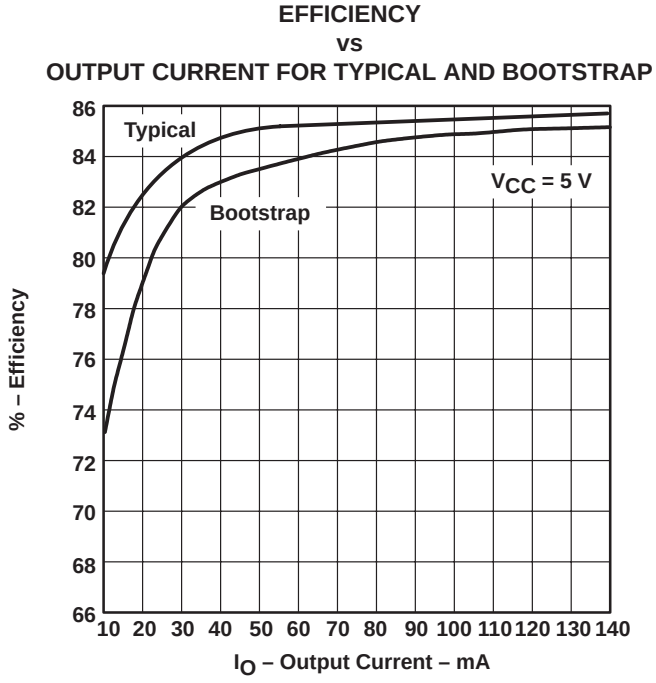
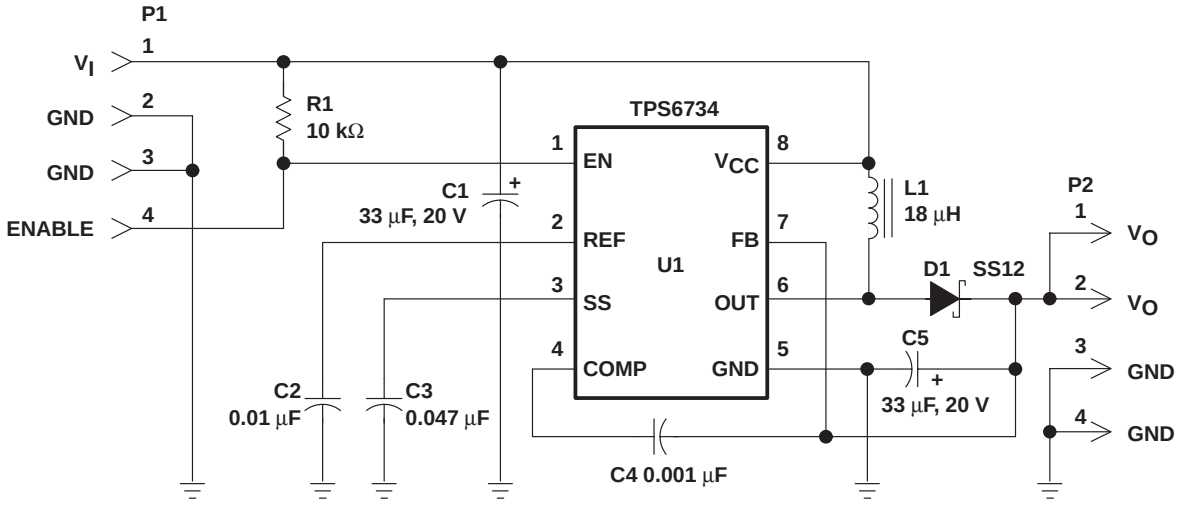


Figure 12

APPLICATION INFORMATION

TPS6734 converter design with recommended layout

The following schematic (Figure 13) and a required-components table are provided for a 12-V-output boost converter. The converter is capable of delivering 120 mA of output current over an input voltage range of 3.75 V to 12 V. Recommended layout and detailed artwork for a PCB are provided in Figures 14 through 17.



NOTE A: A jumper between pins P1-3 and P1-4 shuts off the TPS7634. Remove the jumper to resume normal operation.

Figure 13. Schematic for Printed Circuit Board (shown in Figures 14 through 17)

Required Components

QTY.	DESCRIPTION	REF DES	MANUFACTURER'S PART NO.	MANUFACTURER
1	IC, power supply, 12 V for flash memory	U1	TPS6734ID	Texas Instruments
1	Diode, Schottky	D1	SS12	General Instruments
1	Inductor, 18 μH, 150 mΩ, 1.23 A(DC)	L1	CD54180MC	Sumida
2	Capacitor, 33 μF, 20 V, tantalum	C1,5	TAPSD336M020R0200	AVX
1	Capacitor, 0.01 μF, 50 V, ceramic, 0805	C2		
1	Capacitor, 0.047 μF, 50 V, ceramic, 1206	C3		
1	Capacitor, 0.001 μF, 50 V, ceramic, 0805	C4		
2	Connector, header, 4-pin	P1,2		Molex
1	PCB, TPS6734			

APPLICATION INFORMATION

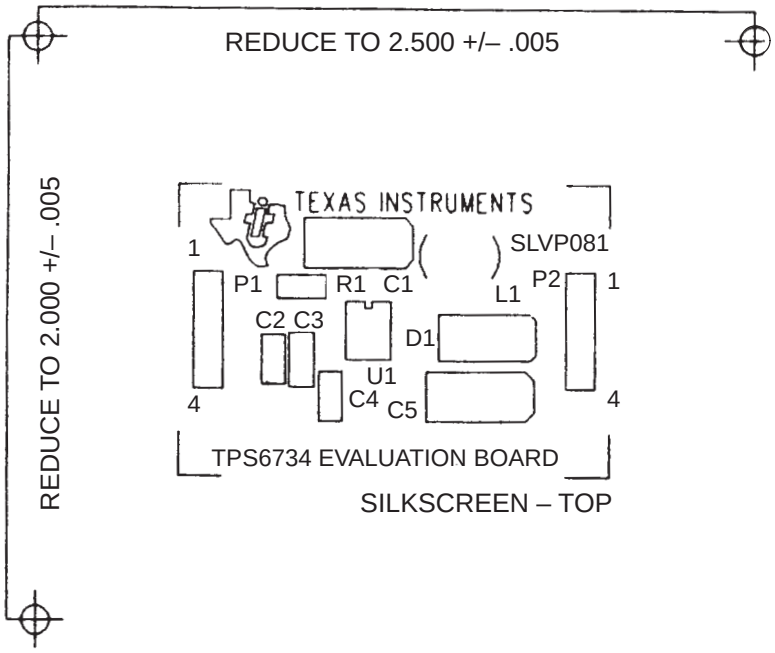


Figure 14. Component Placement

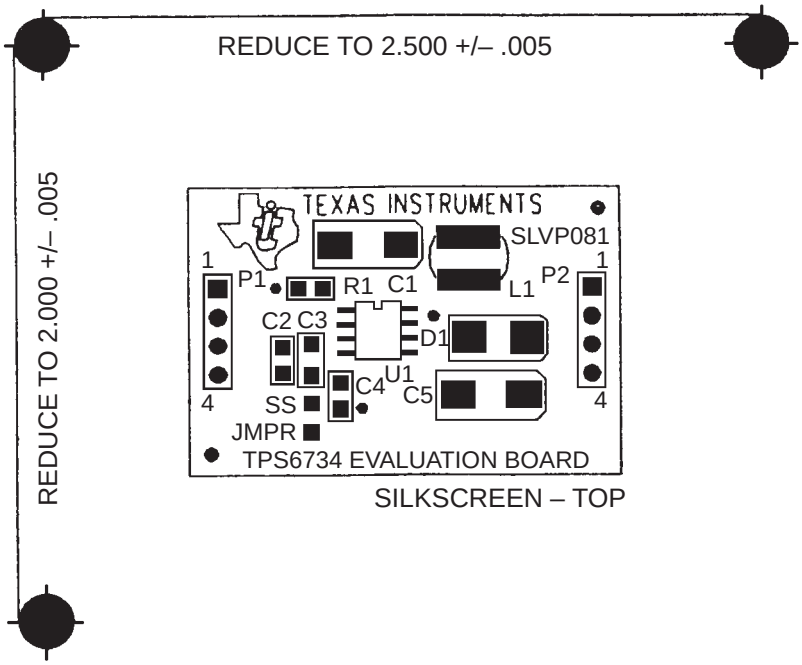


Figure 15. Solder Paste Mask

APPLICATION INFORMATION

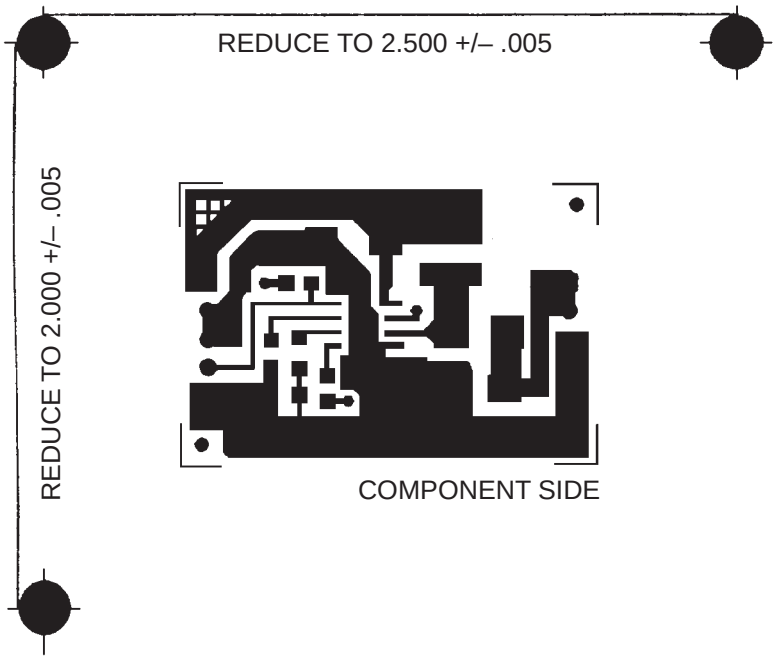


Figure 16. Printed Circuit, Component Side

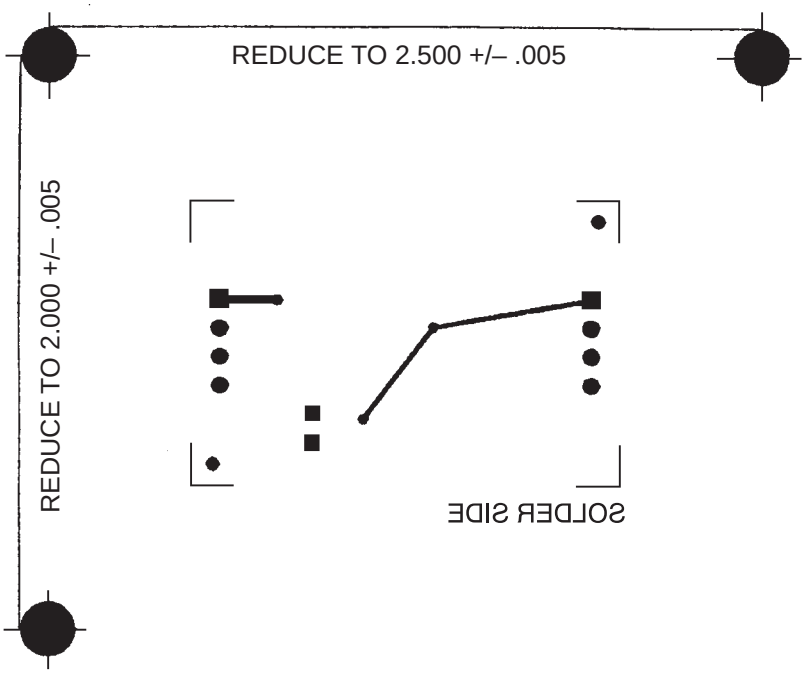
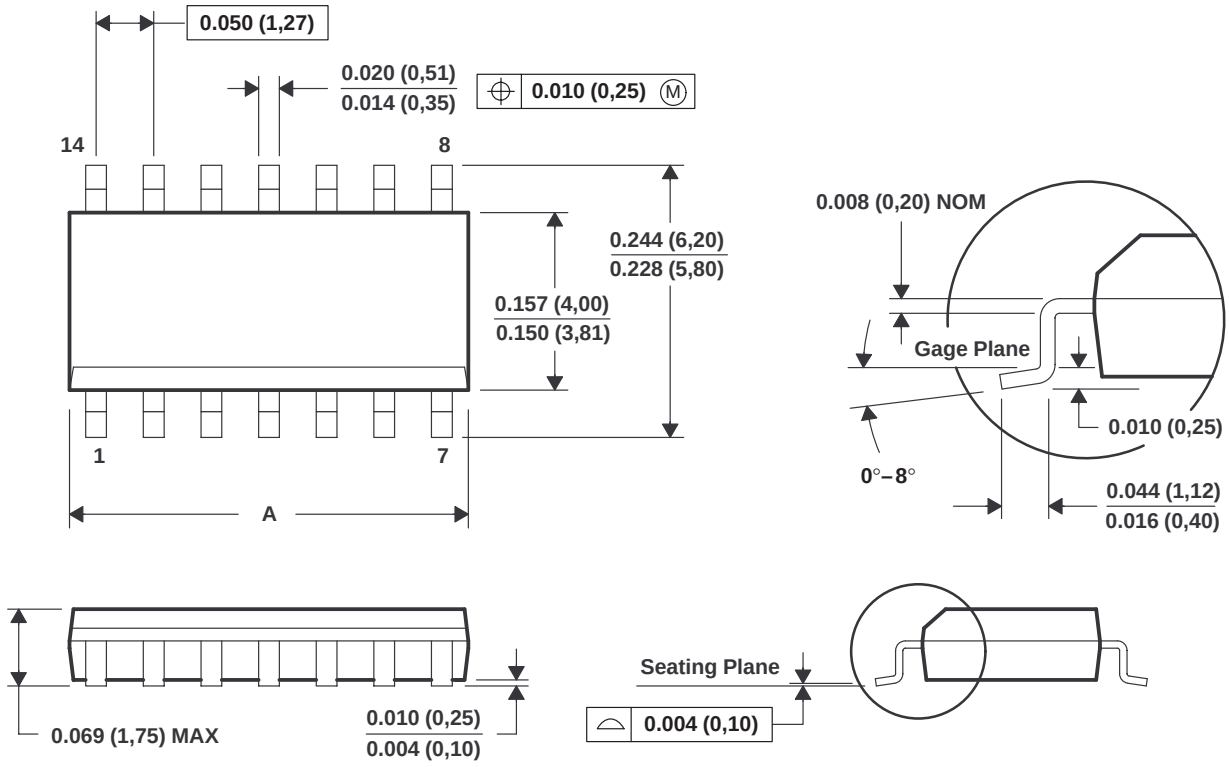


**Figure 17. Printed Circuit, Wiring Side
(Viewed from Component Side)**

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



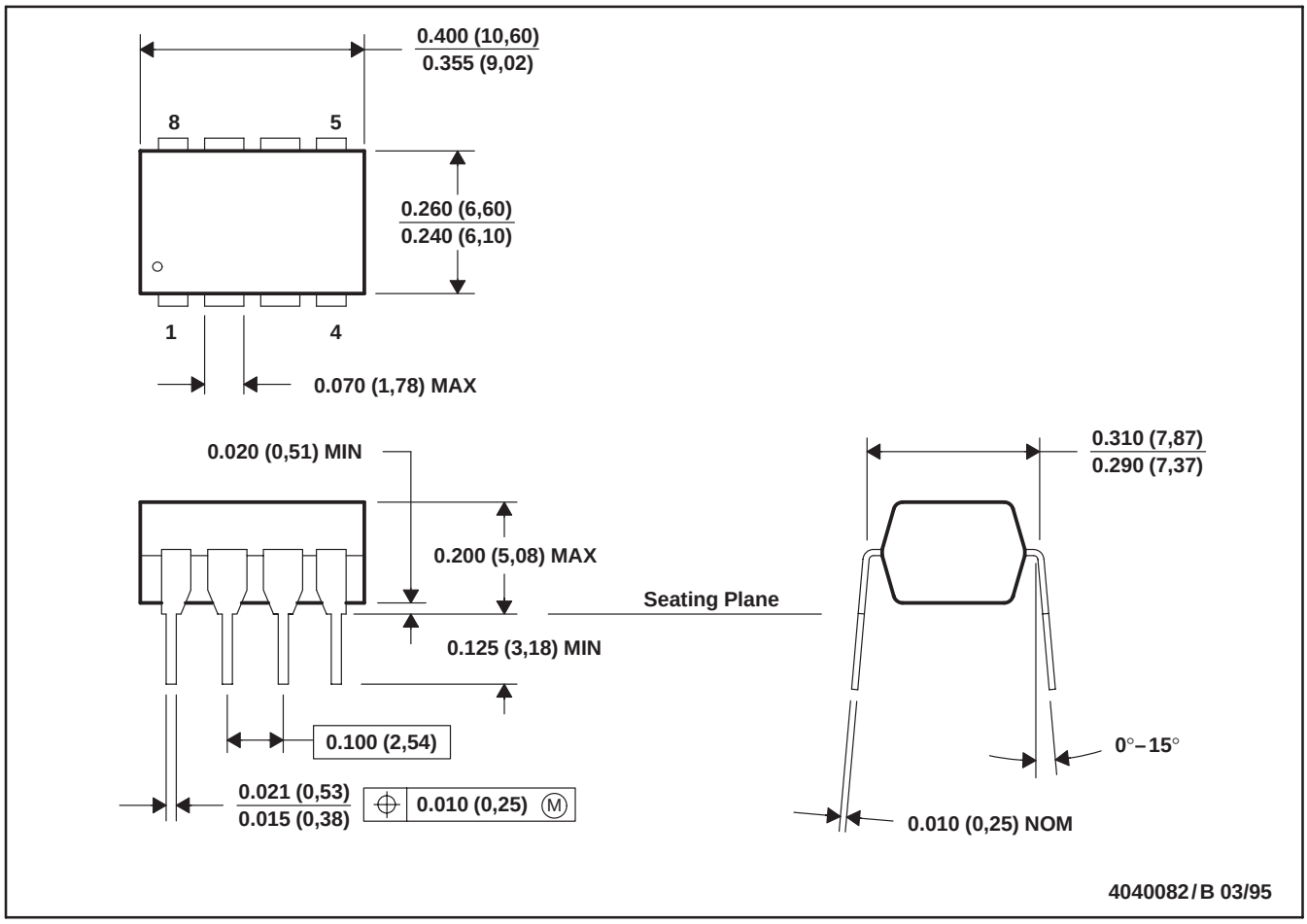
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6734ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6734I	Samples
TPS6734IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6734I	Samples
TPS6734IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6734I	Samples
TPS6734IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6734I	Samples
TPS6734IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS6734IP	Samples
TPS6734IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS6734IP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

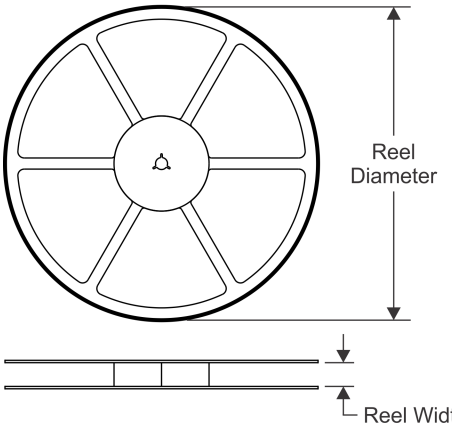
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

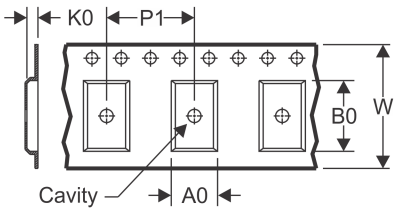
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

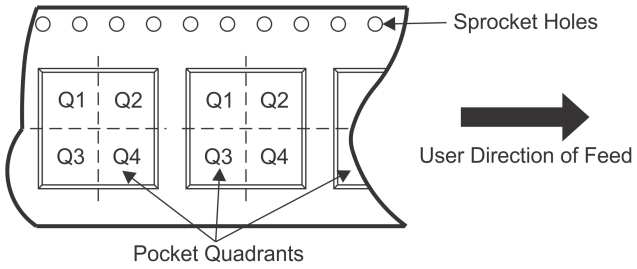


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

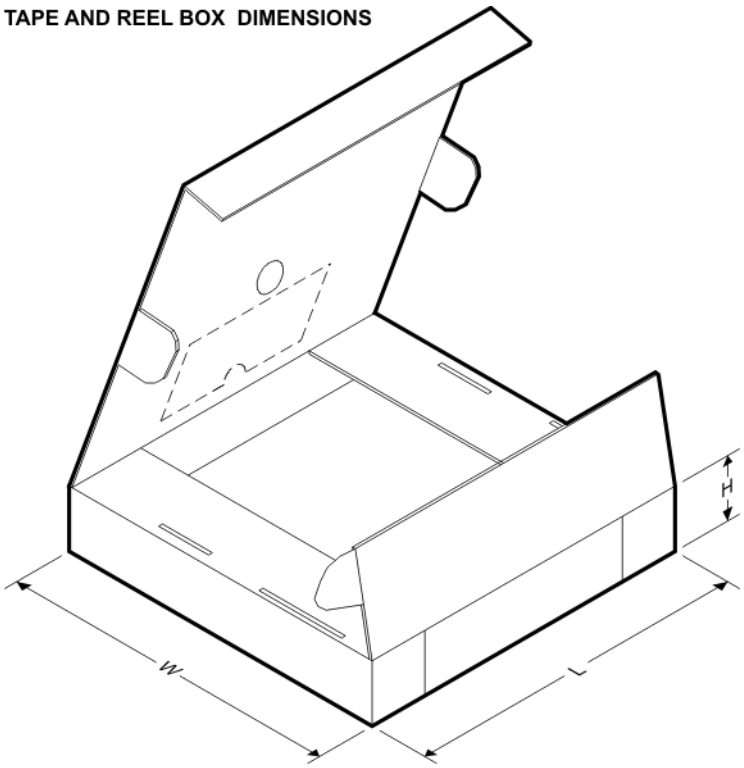
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6734IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

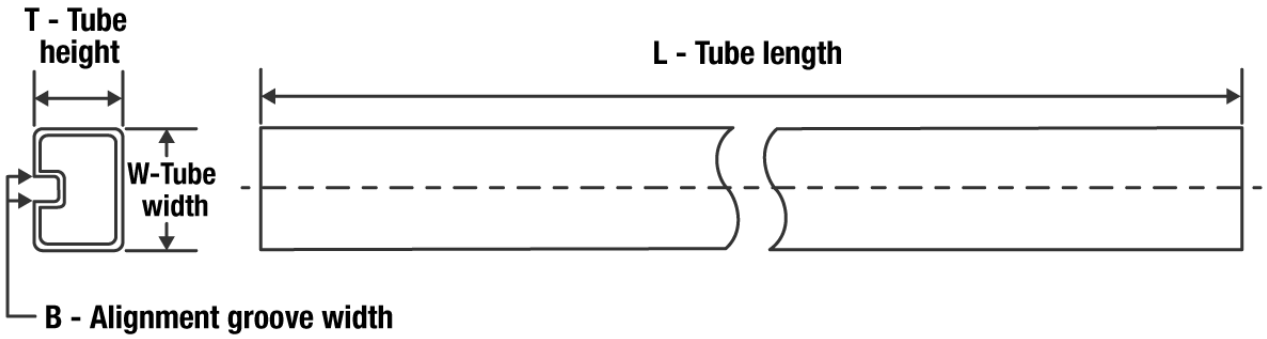
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6734IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS6734ID	D	SOIC	8	75	505.46	6.76	3810	4
TPS6734IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS6734IP	P	PDIP	8	50	506	13.97	11230	4.32
TPS6734IPE4	P	PDIP	8	50	506	13.97	11230	4.32

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