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NTD3817N

Power MOSFET
16 V, 34.5 A, Single N−Channel, DPAK/IPAK

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Three Package Variations for Design Flexibility
- These are Pb−Free Devices

Applications
- DC−DC Converters
- High Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	16	V
Gate−to−Source Voltage			V_{GS}	±16	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	10.8	A
		T_A = 85°C		8.4	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.5	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	7.6	A
		T_A = 85°C		5.9	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	1.2	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	34.5	A
		T_C = 85°C		26.8	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	25.9	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	78	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	22	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)			I_S	21.6	A
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 10 A_{pk}, L = 0.3 mH, R_G = 25 Ω)			EAS	15	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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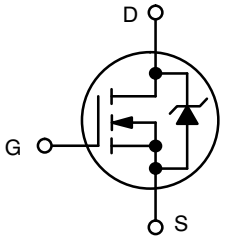
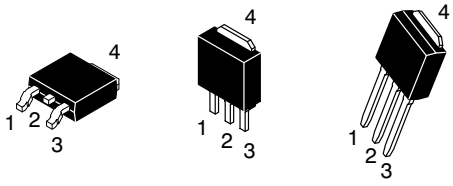
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
16 V	13.9 mΩ @ 10 V	34.5 A
	29 mΩ @ 4.5 V	

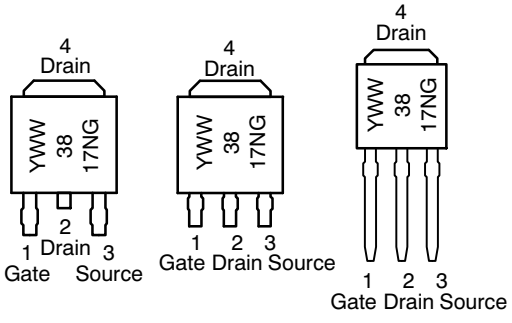


N−CHANNEL MOSFET



CASE 369AA DPAK (Bent Lead) STYLE 2 | **CASE 369AC 3 IPAK (Straight Lead)** | **CASE 369D IPAK (Straight Lead DPAK)**

MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
WW = Work Week
3817N = Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	5.8	°C/W
Junction−to−TAB (Drain)	$R_{\theta JC-TAB}$	4.5	
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	59	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	121	

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		16			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				15.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.1		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 15 A		12.8	13.9	mΩ
		V_{GS} = 4.5 V	I_D = 15 A		19.2	29	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			28		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			702		pF
Output Capacitance	C_{OSS}				257		
Reverse Transfer Capacitance	C_{RSS}				168		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 12 V, I_D = 15 A			7.0	10.5	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.6		
Gate−to−Source Charge	Q_{GS}				2.5		
Gate−to−Drain Charge	Q_{GD}				3.5		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 12 V, I_D = 15 A			13.5		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 12 V, I_D = 15 A, R_G = 3.0 Ω			12		ns
Rise Time	t_r				50		
Turn−Off Delay Time	$t_{d(OFF)}$				12		
Fall Time	t_f				4.6		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 12 V, I_D = 15 A, R_G = 3.0 Ω			8.0		ns
Rise Time	t_r				47		
Turn−Off Delay Time	$t_{d(OFF)}$				20		
Fall Time	t_f				10		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
5. Assume standoff of 110 mm

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 15 A	T_J = 25°C		0.96	1.1	V
			T_J = 125°C		0.86		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 15 A			11		ns
Charge Time	t_a				5.4		
Discharge Time	t_b				5.6		
Reverse Recovery Charge	Q_{RR}				2.8		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			2.49		nH
Drain Inductance, DPAK	L_D				0.0164		
Drain Inductance, IPAK (Note 5)	L_D				1.88		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				1.0		Ω

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
5. Assume standoff of 110 mm

TYPICAL PERFORMANCE CURVES

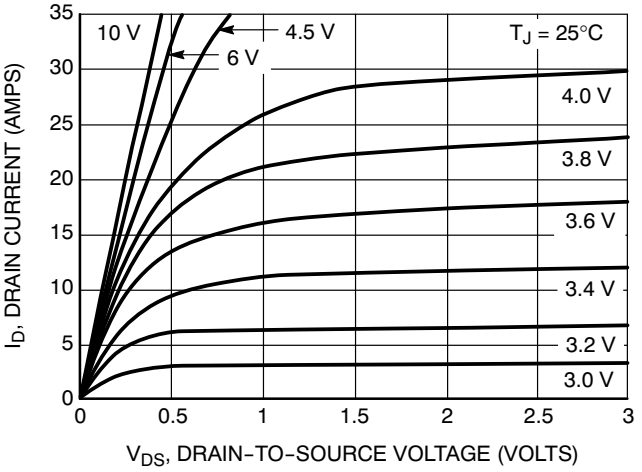


Figure 1. On−Region Characteristics

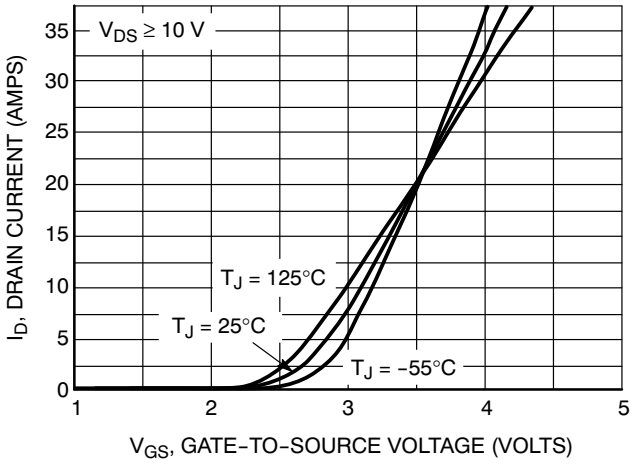


Figure 2. Transfer Characteristics

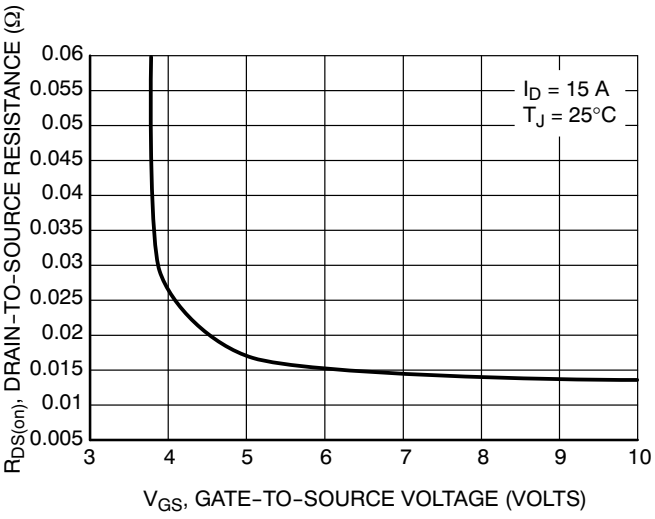


Figure 3. On−Resistance vs. Gate−to−Source Voltage

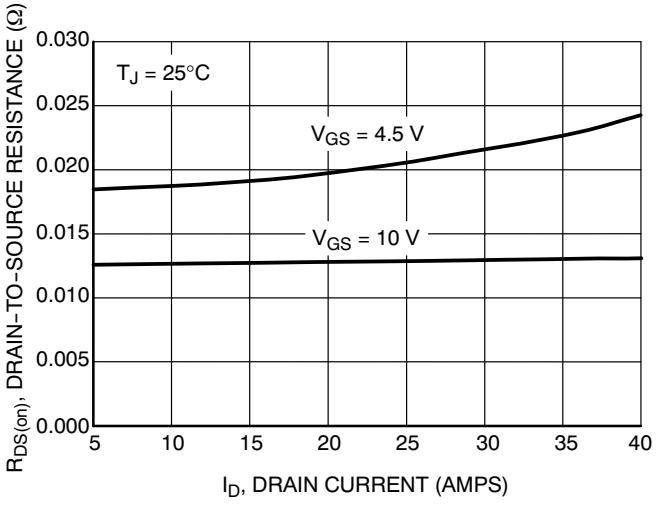


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

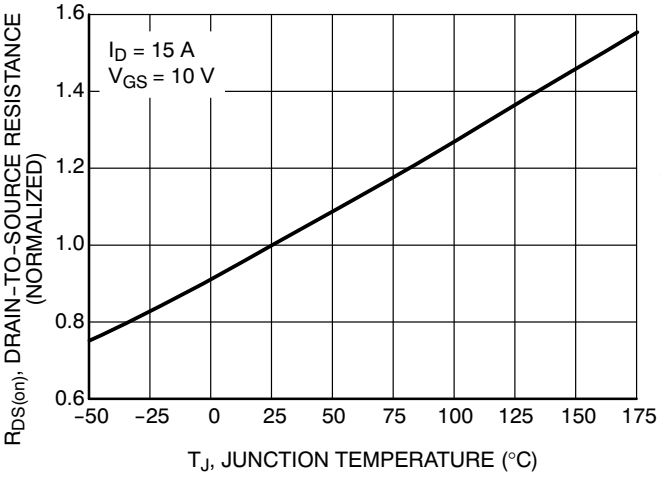


Figure 5. On−Resistance Variation with Temperature

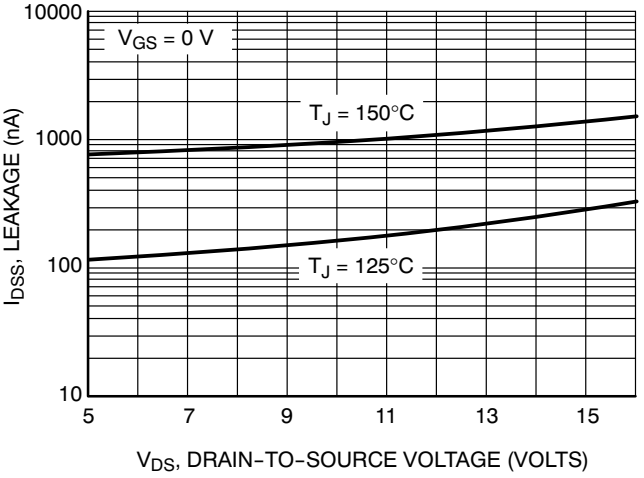


Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

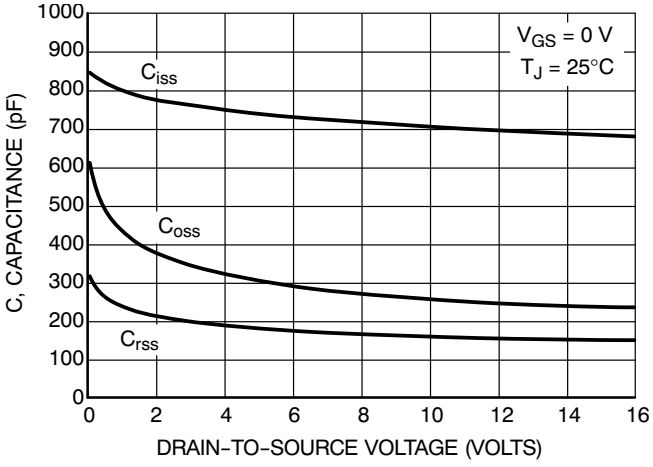


Figure 7. Capacitance Variation

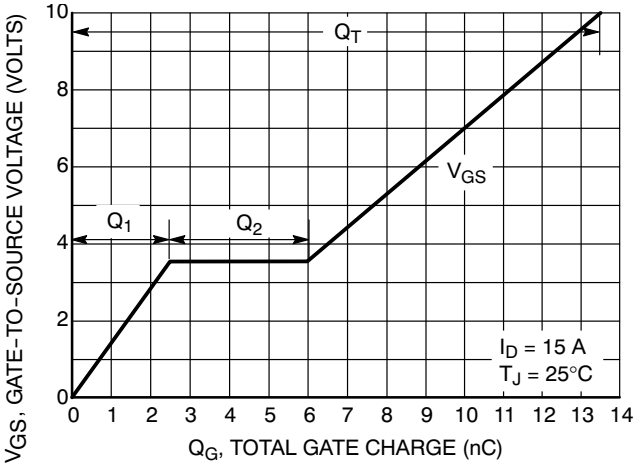


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

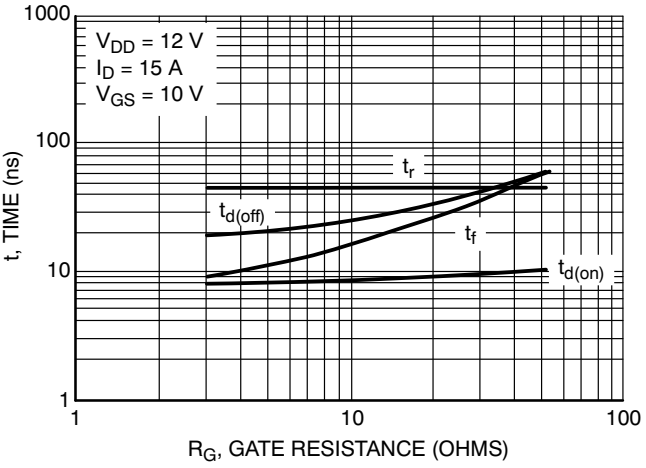


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

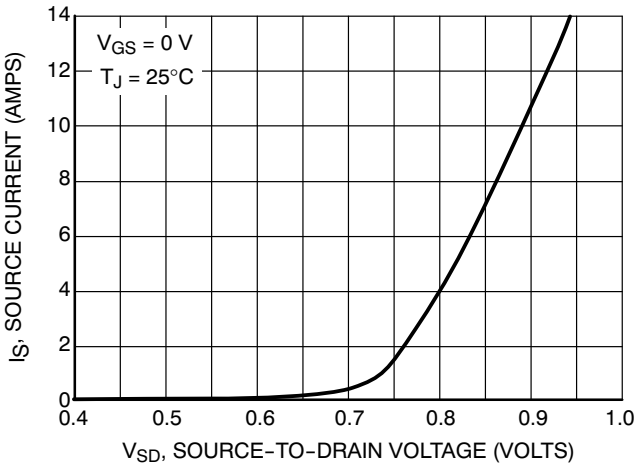


Figure 10. Diode Forward Voltage vs. Current

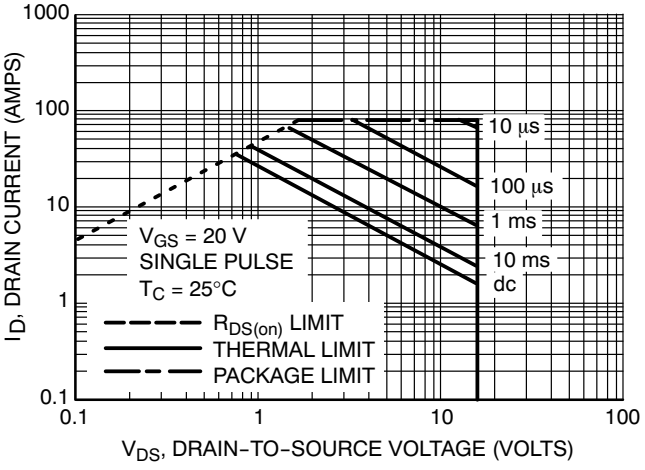


Figure 11. Maximum Rated Forward Biased Safe Operating Area

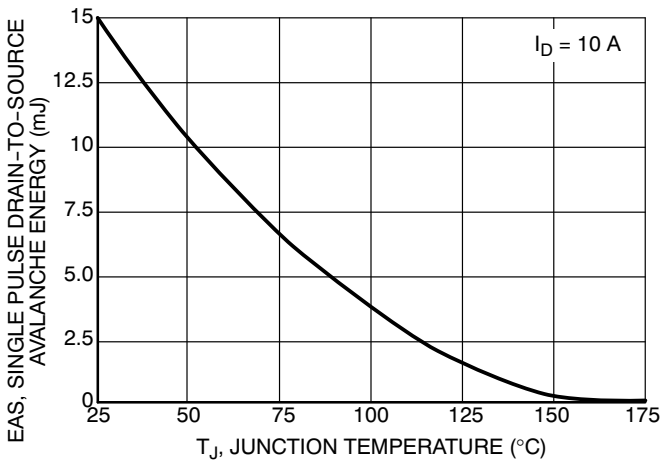


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

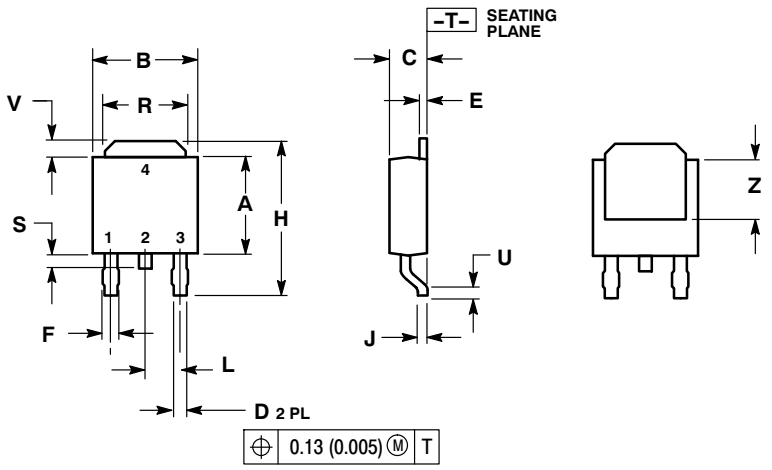
ORDERING INFORMATION

Device	Package	Shipping†
NTD3817NT4G	DPAK (Pb−Free)	2500 / Tape & Reel
NTD3817N−1G	IPAK (Pb−Free)	75 Units / Rail
NTD3817N−35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb−Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369AA−01
ISSUE A

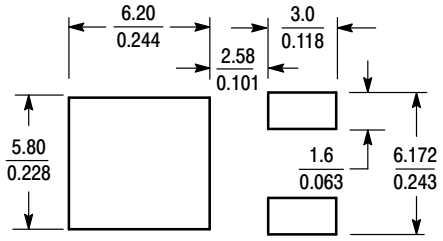


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*

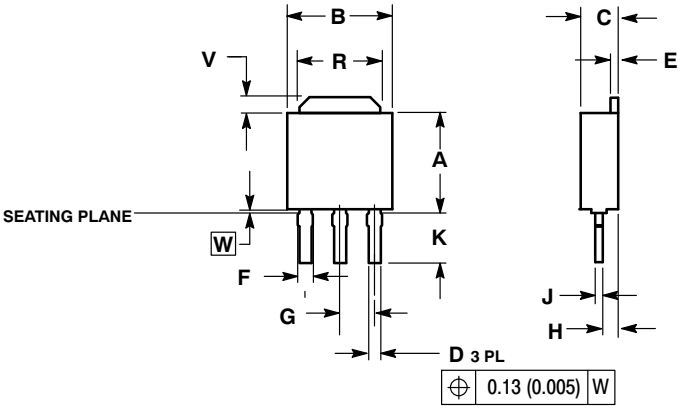


SCALE 3:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

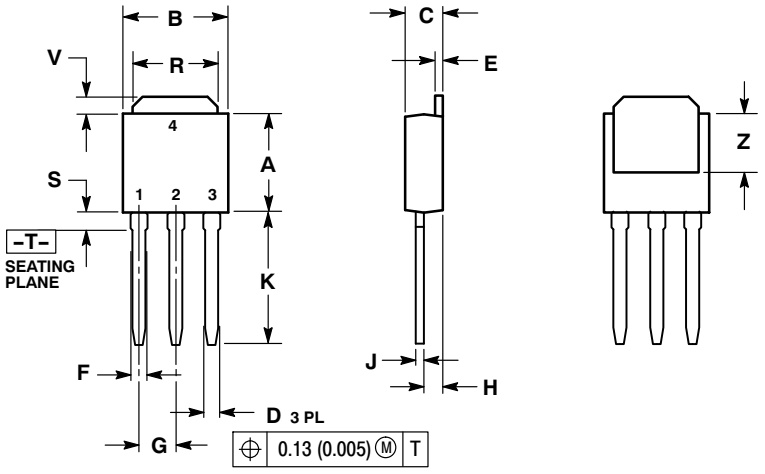
3 IPAK, STRAIGHT LEAD
CASE 369AC−01
ISSUE O



NOTES:
1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

IPAK (STRAIGHT LEAD DPAK)
CASE 369D−01
ISSUE B



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E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

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