

# NTMFS4C028N

## MOSFET – Power, Single, N-Channel, SO-8 FL 30 V, 52 A



ON Semiconductor®

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### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

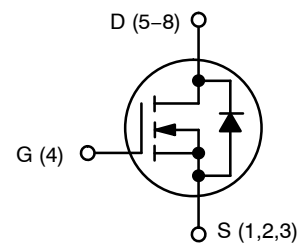
- CPU Power Delivery
- DC-DC Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	16.4	A
		$T_A = 80^\circ\text{C}$	12.3	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	2.51	W	
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	25.3	A
		$T_A = 80^\circ\text{C}$	19.0	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	$P_D$	6.0	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	9.0	A
		$T_A = 80^\circ\text{C}$	6.8	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	0.76	W	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	52	A
		$T_C = 80^\circ\text{C}$	39	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	25.5	W	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	146	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{Dmax}$	80	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$		-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	23	A	
Drain to Source $dV/dt$	$dV/dt$	7.0	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{GS} = 10$ V, $I_L = 29$ A <sub>pk</sub> , $L = 0.1$ mH, $R_{GS} = 25 \Omega$ ) (Note 3)	$E_{AS}$	42	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

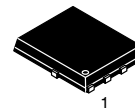
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
30 V	4.73 m $\Omega$ @ 10 V	52 A
	7.0 m $\Omega$ @ 4.5 V	

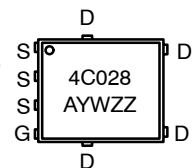


N-CHANNEL MOSFET

### MARKING DIAGRAMS



SO-8 FLAT LEAD CASE 488AA STYLE 1



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4C028NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4C028NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS4C028N

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. Parts are 100% tested at  $T_J = 25^\circ\text{C}$ ,  $V_{GS} = 10\text{ V}$ ,  $I_L = 20\text{ A}_{pk}$ ,  $EAS = 20\text{ mJ}$ .

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.9	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	49.8	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	164.6	
Junction-to-Ambient – ( $t \leq 10\text{ s}$ ) (Note 4)	$R_{\theta JA}$	21.0	

4. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
5. Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSS(t)}$	$V_{GS} = 0\text{ V}$ , $I_{D(aval)} = 8.4\text{ A}$ , $T_{case} = 25^\circ\text{C}$ , $t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			14.4		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 24\text{ V}$			1.0	$\mu\text{A}$
		$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$			10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	1.3		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.8		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 30\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 18\text{ A}$		3.9	4.73	$\text{m}\Omega$
				5.8	7.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}$ , $I_D = 15\text{ A}$		50		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$	0.3	1.0	2.0	$\Omega$

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $V_{DS} = 15\text{ V}$		1252		$\text{pF}$
Output Capacitance	$C_{OSS}$			610		
Reverse Transfer Capacitance	$C_{RSS}$			126		
Capacitance Ratio	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 15\text{ V}$ , $f = 1\text{ MHz}$		0.101		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}$ , $V_{DS} = 15\text{ V}$ ; $I_D = 30\text{ A}$		10.9		$\text{nC}$
Threshold Gate Charge	$Q_{G(TH)}$			1.9		
Gate-to-Source Charge	$Q_{GS}$			3.4		
Gate-to-Drain Charge	$Q_{GD}$			5.4		
Gate Plateau Voltage	$V_{GP}$			3.1		
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}$ , $V_{DS} = 15\text{ V}$ ; $I_D = 30\text{ A}$		22.2	

### SWITCHING CHARACTERISTICS (Note 7)

6. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
7. Switching characteristics are independent of operating junction temperatures.

# NTMFS4C028N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>SWITCHING CHARACTERISTICS</b> (Note 7)							
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		10		ns	
Rise Time	$t_r$			32			
Turn-Off Delay Time	$t_{d(OFF)}$			16			
Fall Time	$t_f$			6.0			
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0		ns	
Rise Time	$t_r$			28			
Turn-Off Delay Time	$t_{d(OFF)}$			20			
Fall Time	$t_f$			4.0			
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.79	1.1	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$		31		ns	
Charge Time	$t_a$			15			
Discharge Time	$t_b$			16			
Reverse Recovery Charge	$Q_{RR}$				15		nC

6. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

7. Switching characteristics are independent of operating junction temperatures.

# NTMFS4C028N

## TYPICAL CHARACTERISTICS

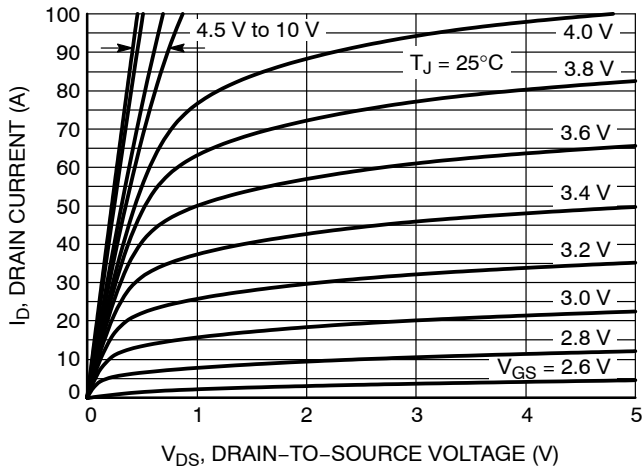


Figure 1. On-Region Characteristics

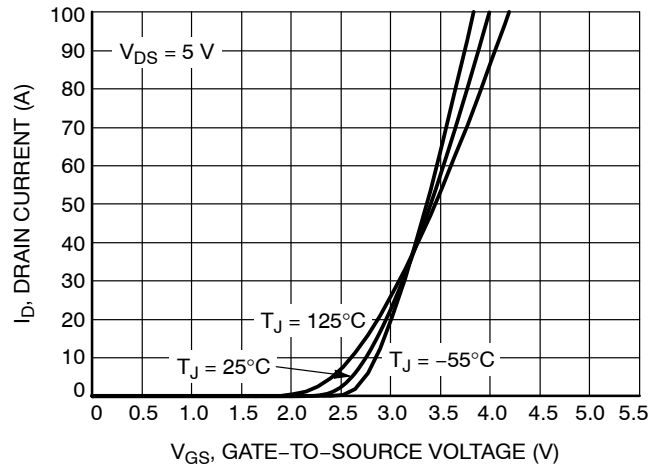


Figure 2. Transfer Characteristics

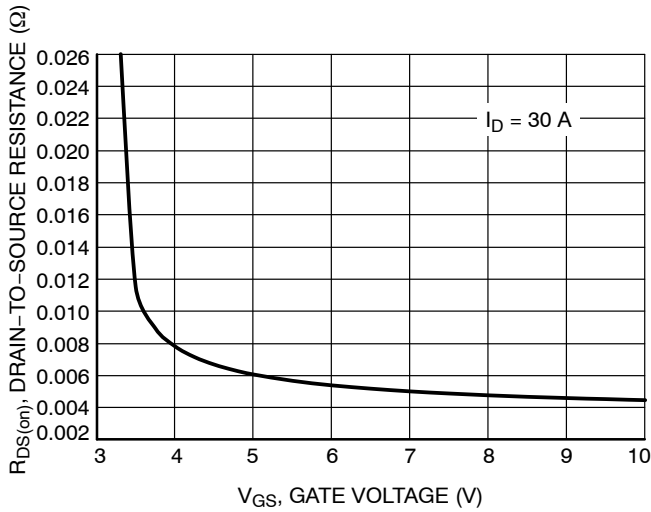


Figure 3. On-Resistance vs. Gate-to-Source Voltage

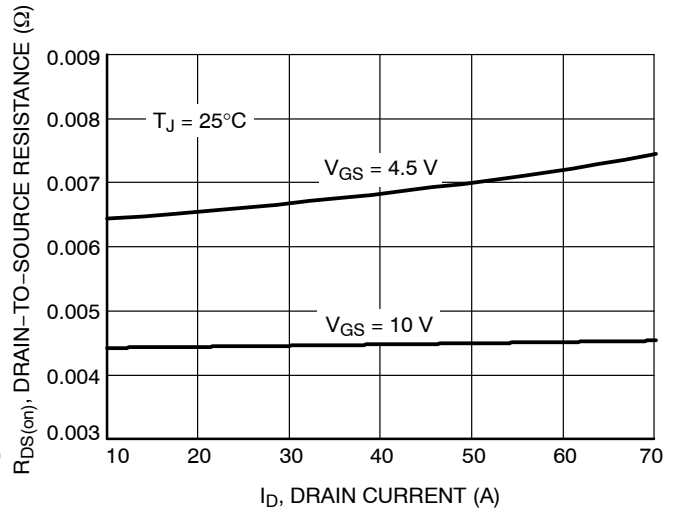


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

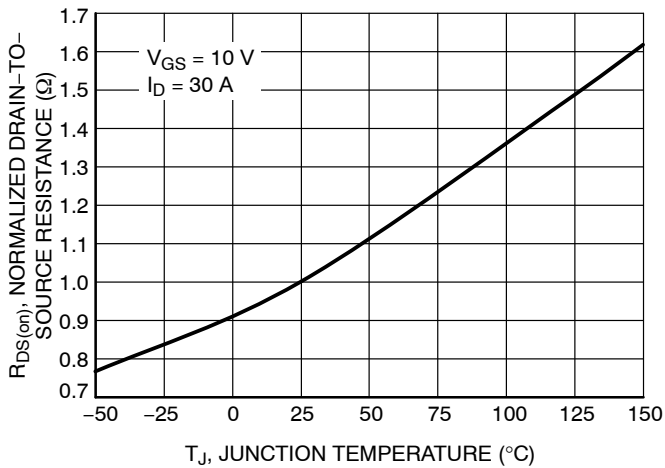


Figure 5. On-Resistance Variation with Temperature

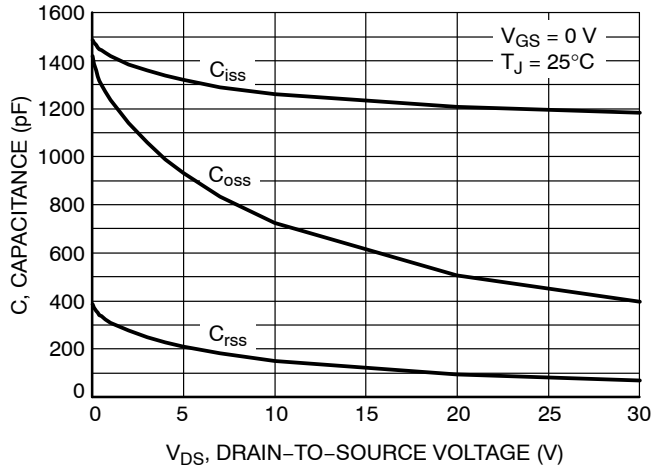
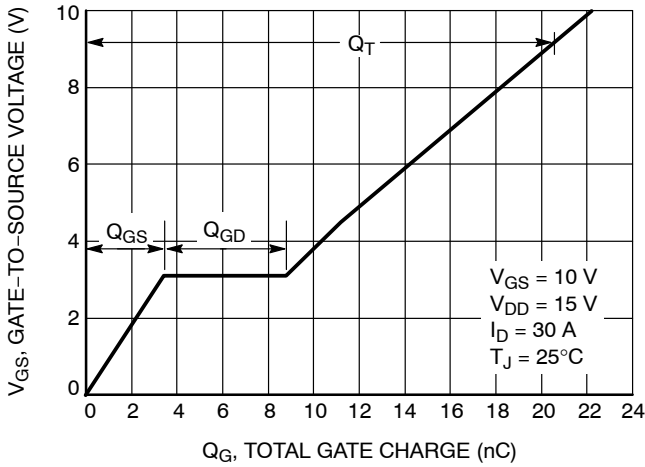


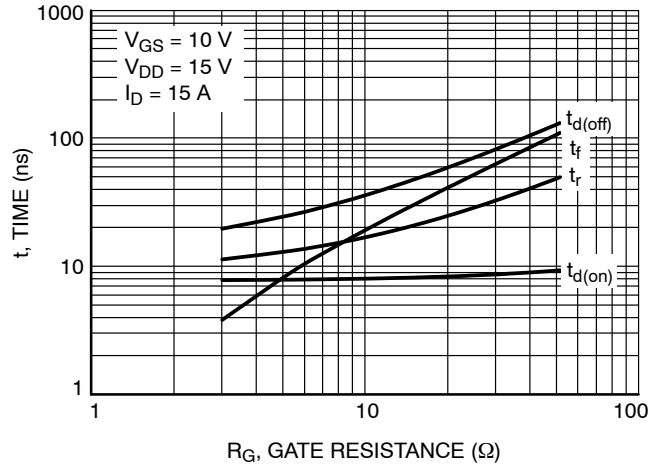
Figure 6. Capacitance Variation

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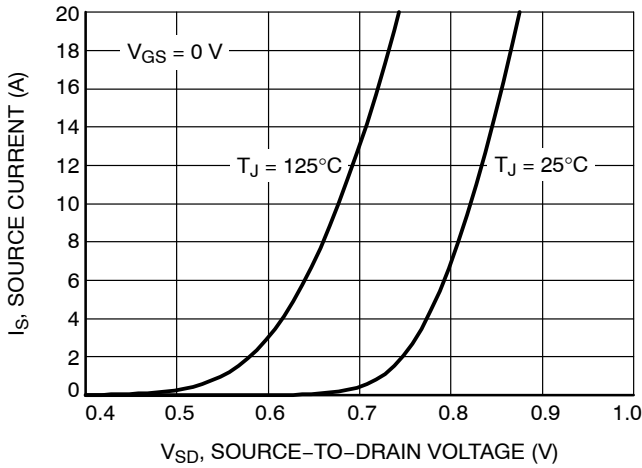
## TYPICAL CHARACTERISTICS



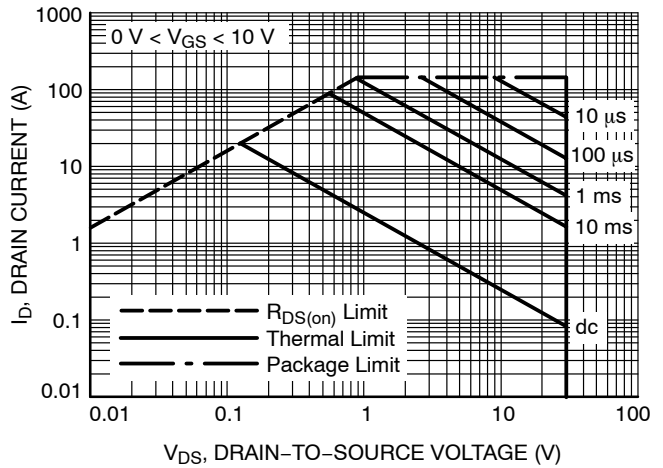
**Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



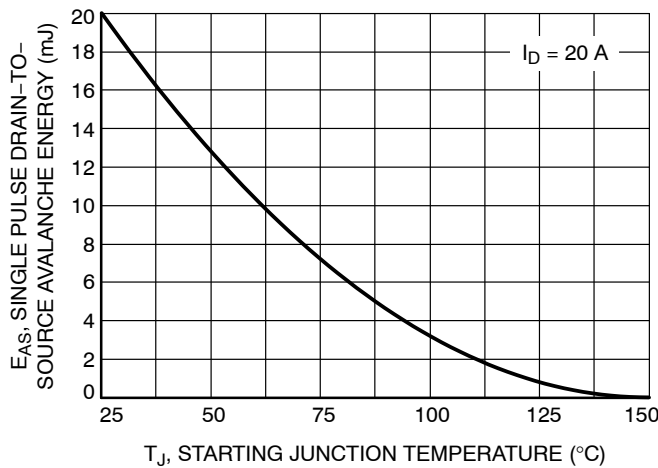
**Figure 8. Resistive Switching Time Variation vs. Gate Resistance**



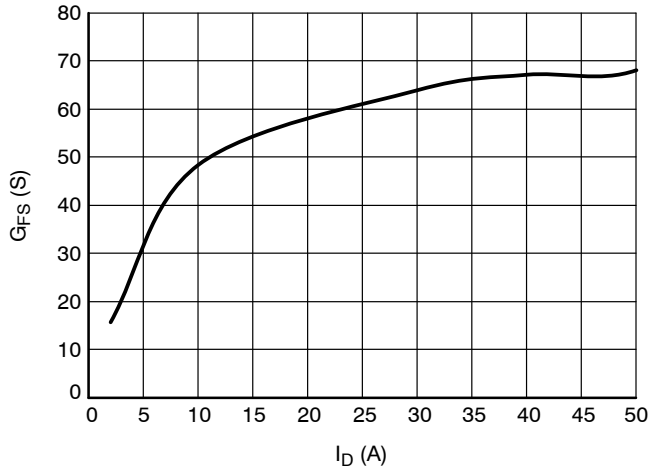
**Figure 9. Diode Forward Voltage vs. Current**



**Figure 10. Maximum Rated Forward Biased Safe Operating Area**



**Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature**



**Figure 12.  $G_{FS}$  vs.  $I_D$**

# NTMFS4C028N

## TYPICAL CHARACTERISTICS

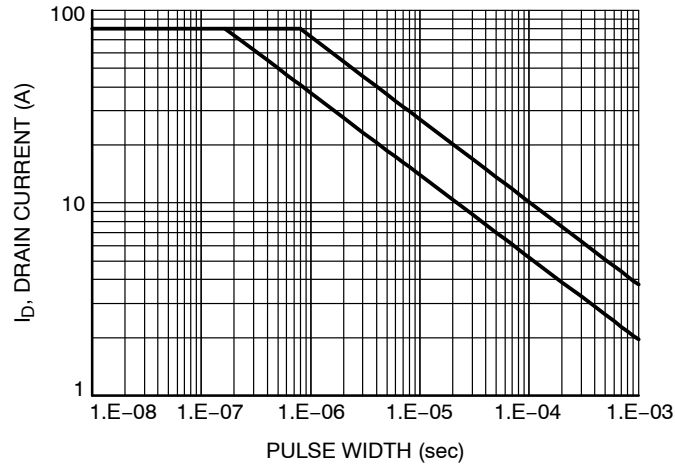


Figure 13. Avalanche Characteristics

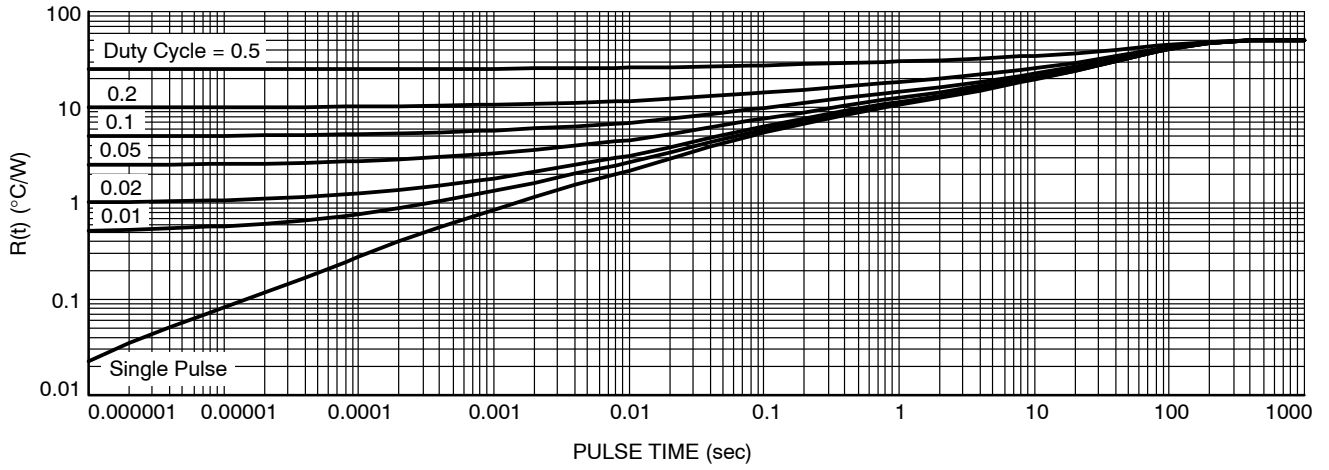


Figure 14. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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