LatticeCORE

JESD207 IP Core User's Guide

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IPUG111_01.0

JESD207 is a Radio Front End – Base Band Digital Parallel (RBDP) interface between a Radio Front-end integrated circuit (RFIC) and a Baseband integrated circuit (BBIC).

This document provides technical information about the Lattice JESD207 IP core. This IP core together with DDR and PLL functionality integrated in the LatticeECP3™ FPGAs implements baseband (BB) side data and control plane paths. It can be used to connect to a radio front-end (RF) transceiver device with integrated analog to digital converter (ADC) and digital to analog converter (DAC).

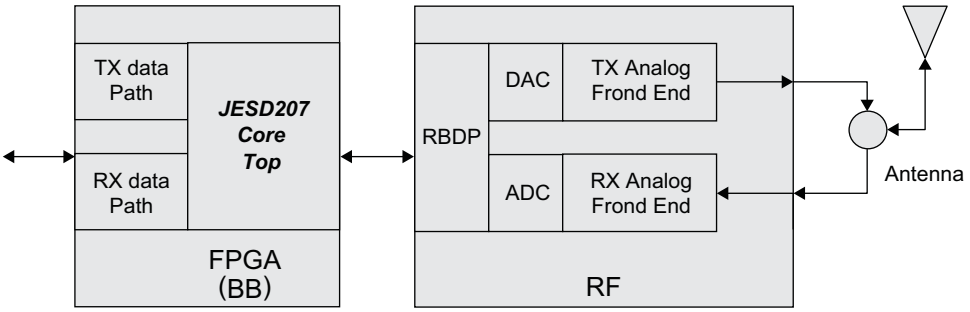
The Lattice JESD207 IP core is fully compliant to the JESD207 JEDEC specification:

Radio Front End - Baseband Digital Parallel (RBDP) Interface- JESD207, JEDEC solid state technology association, March, 2007.

Application System

Figure 1-1 shows a typical system application. The baseband is implemented in LatticeECP3 FPGA and the RF circuit is implemented on another device that provides RDBP interface. A JESD207 IP core is instantiated in LatticeECP3™ FPGA and connected to the RF device via JESD207 interface.

Figure 1-1. JESD207 IP Block Diagram



Quick Facts

Table 1-1 gives quick facts about the JESD207 IP core.

Table 1-1. JESD207 IP Core Quick Facts

		JESD207 IP Core Configuration			
Core Requirements	FPGA Families Supported	LatticeECP3			
	Minimal Device Needed	LFE3-17EA			
Configuration		DP_WIDTH=10, CP_SUPPORT=No	DP_WIDTH=12, CP_SUPPORT=No	DP_WIDTH=10, CP_SUPPORT=Yes, CP_WIRES=4	DP_WIDTH=12, CP_SUPPORT=Yes, CP_WIRES=3
Resource Utilization	Targeted Device	LFE3-150EA-6FN1156C			
	Data Path Width	103	121	208	226
	LUTs	25	29	314	319
	Slices	55	64	220	229
Design Tool Support	Lattice Implementation	Lattice Diamond® 2.0			
	Synthesis	Synopsys® Synplify® Pro for Lattice F-2012.03L			
	Simulation	Aldec® Active-HDL™ 9.2SP1 Lattice Edition			
		Mentor Graphics® ModelSim® SE 6.6e			

Features

Data Path Feature

- Data path clock and data rate controlled by RFIC (configured by BBIC) up to 90 MHz and 180 MSps
- Data width matched to baseband sample width – 10 or 12 bits
- Raw data path interface transfer bandwidth up to 1.8 or 2.2 Gbps
- Double data rate (DDR) source-synchronous data path transfer timing
- Low latency (single baseband complex sample period) data transfer
- Low implementation complexity

Control Plane Path Feature

- Clock rate and serial transfer rate controlled by BBIC up to 50 MHz
- 1-bit command + 7-bit address control field format
- Flexible transaction format using one or more 8-bit data fields per transaction to allow per-transaction optimization of latency or bandwidth
  - minimum 325ns transaction latency with 8-bit data transactions (maximum 24 Mbps data rate)
  - data rates above 40 Mbps can be achieved with extended transactions
- Serial clock can be stopped between transactions, reducing control plane power consumption to negligible levels.

Release Information

- JESD207 core version 1.0
- Last updated March, 2013

Lattice JESD207 IP core includes Data path and Control Plane Path.

Data Path translates BB data path control signals to JESD207 control signals. On the transmit (TX) side, Data Path gets TX I and Q data from BB data interface, and forwards the data to double data rate (DDR) and Tri-state control module. On the receive (RX) side, it gets RX I and Q data from DDR and Tri-state control module and forwards the data to BB data interface. According to BB data control signals **tx_en** and **rx_en**, the module generates JESD207 data interface signals **txnrx** and **enable**.

Control Plane Path detects the start of a control plane transaction, buffers write/read, address and data inputs, and translates parallel BB control plane signals to JESD207 control plane interface format. The write/read, address and data will be transmitted in sequence. During read, Control Plane Path deserializes read data into parallel format and forwards the parallel read data to BB control plane interface.

The core top implementation is provided with the IP core. The IP core top implementation includes JESD207 core, ddr_trsc and mclk2sclk(PLL) modules.

The module mclk2sclk is a PLL. It takes mclk as the reference clock and generates sclk, and the clocks for ODDR components.

The module ddr_trsc implements DDR and Tri-state control functions. During transmit transactions, one of the transmission data (I data or Q data) is sampled on the rising edge, and the other one is sampled on the falling edge, and the I and Q data will be presented on **diq** by time division multiplexing. During receive transactions, the double rate data **diq** is sampled on both edges, and I and Q data are presented on the rising edge of fclk.

Control plane interface is SPI (Serial Peripheral Interface bus). Two different SPI control plane interfaces are specified in the JESD207 standard. The 3-wire SPI control plane interface includes **cp_clk**, **cp_cs**, **cpdio** (**cpdio** is bidirectional signal). The 4-wire SPI control plane interface includes **cp_clk**, **cp_cs**, **mosi** and **miso**.

For SPI control plane interface, JESD207 IP is the master device, and initiates the data frame. When wirte transaction, JESD207 IP sends command/address/data via **cpdio** or **mosi**. When read transaction, JESD207 IP sends command/address via **cpdio** or **mosi**, and gets the return data via **cpdio** or **msio**. **cp_cs** performs slave select (chip select).

Figure 2-1 shows the reference design (IP core top)implementation with 4-wire control plane interface and Figure 2-2 shows the reference design (IP core top) implementation with 3-wire control plane interface.

Block Diagram

Figure 2-1. JESD207 IP Block Diagram (with JESD207 4-Wire Control Plane Interface)

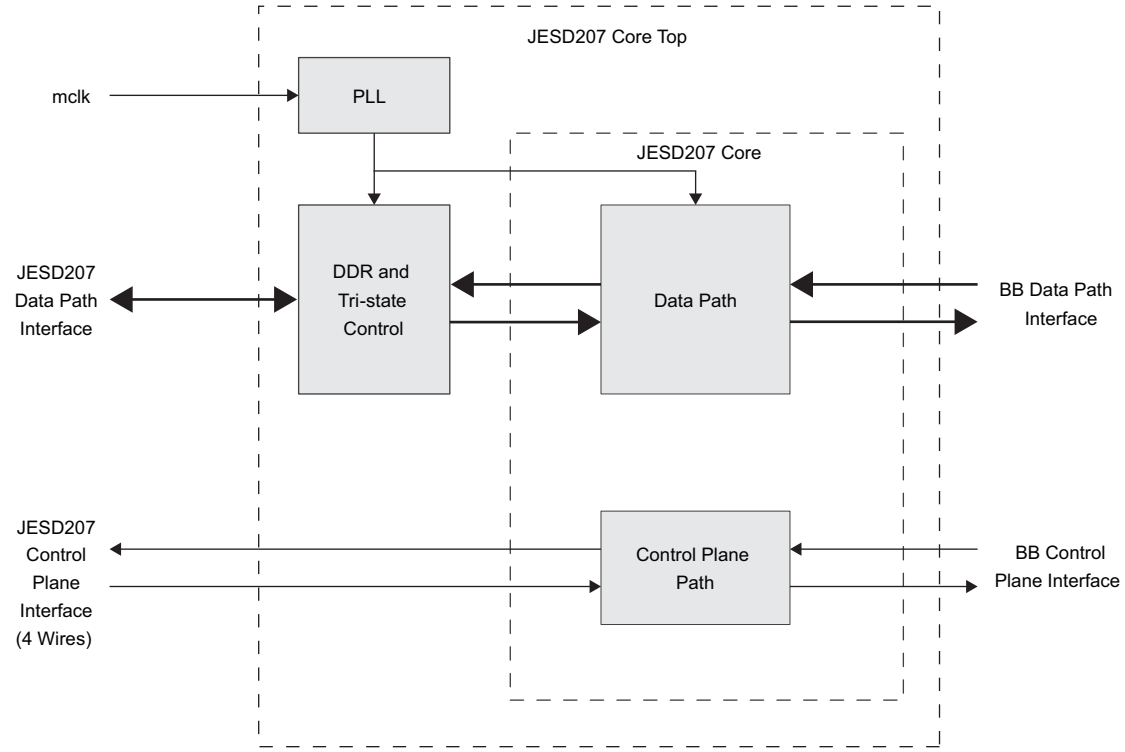
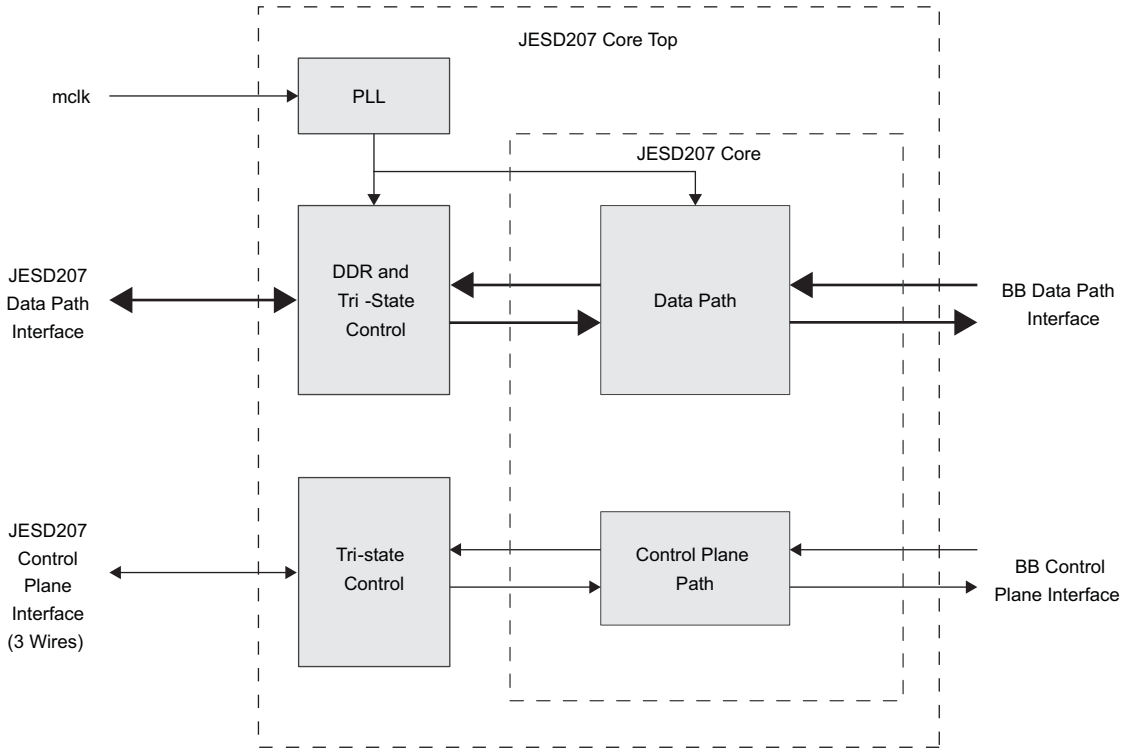


Figure 2-2. JESD207 IP Block Diagram (with JESD207 3-Wire Control Plane Interface)



Interface Description

The input/output (I/O) interface of the IP core top is shown in Figure 2-3 and briefly described in Table 2-1.

Figure 2-3. JESD207 IP Core Top I/O Interface

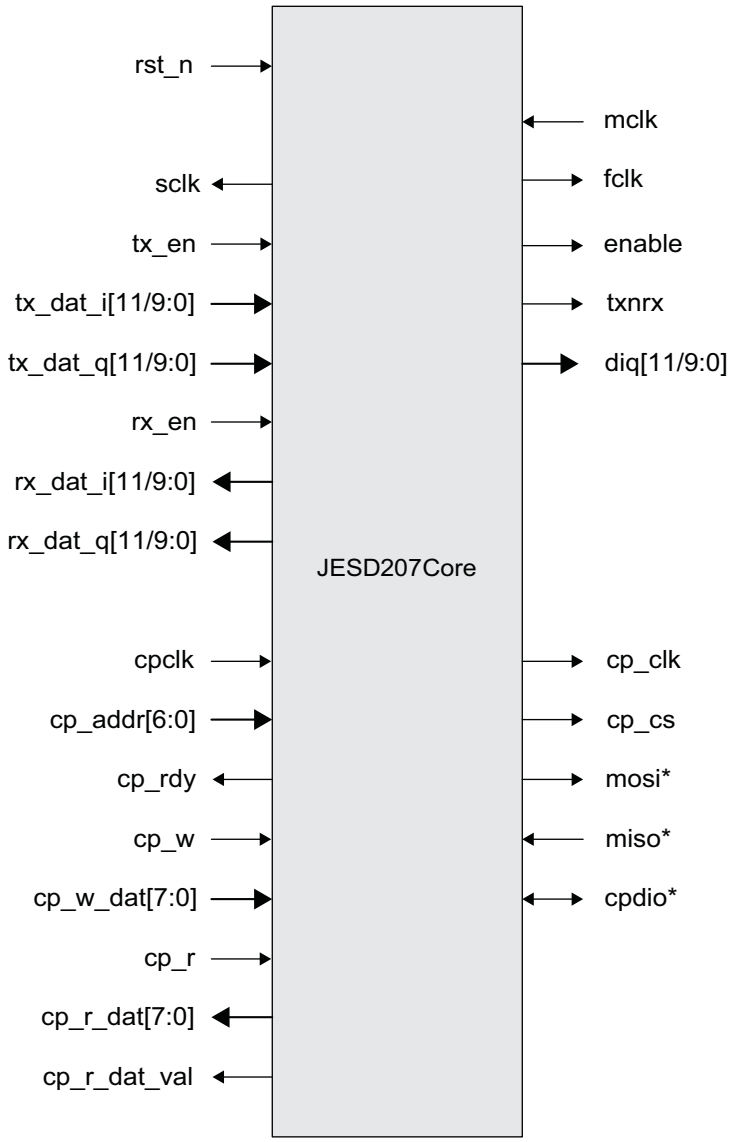


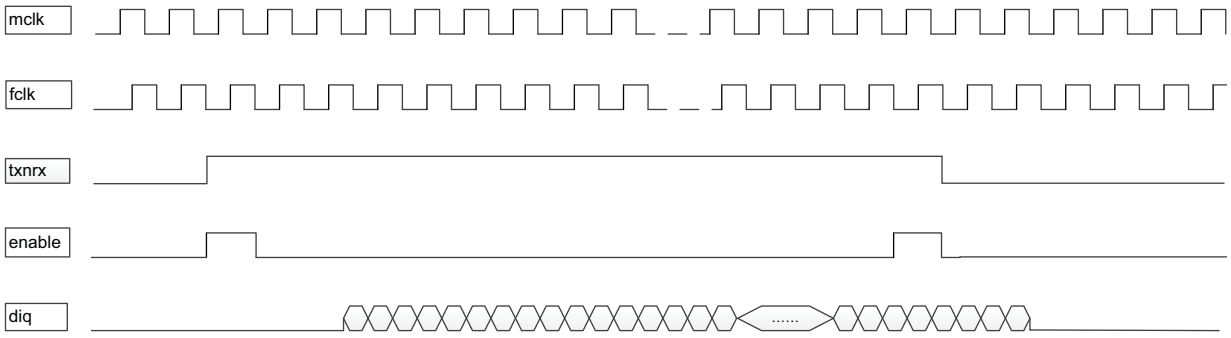
Table 2-1. JESD207 Interface Description

Port	Bits	I/O	Description
Reset			
rst_n	1	I	System wide asynchronous active-low reset signal.
BB Data path interface			
sclk	1	O	System clock for user interface.
tx_en	1	I	Transmission enable signal. When it is active, tx_dat_i and tx_dat_q will be transmitted.
tx_dat_i	12/10	I	Transmission I data.
tx_dat_q	12/10	I	Transmission Q data.
rx_en	1	I	Receive enable signal. When it is active, tx_dat_i and tx_dat_q will be received after 8 clock cycles.
rx_dat_i	12/10	O	Receive I data.
rx_dat_q	12/10	O	Receive Q data.
JESD207 Data path interface			
mclk	1	I	Master clock from RF side.
fclk	1	O	Slave clock to RF side.
enable	1	O	The signal is a data transfer burst control (along with txnrx). Asserted by the BB for a single cycle to indicate the start of each burst, and subsequently asserted a second time for a single cycle to indicate the end of each burst.
txnrx	1	O	The signal is a data transfer burst control (along with enable). The level on txnrx controls the direction of the transfer burst. When ‘1’, it is a TX burst. When ‘0’, it is a RX burst.
diq	12/10	IO	Bidirectional signal. Transmission and receive I/Q data will be presented on it by time division multiplexing.
BB Control plane interface			
cp_clk	1	I	The input clock for control plane path.
cp_addr	7	I	Control plane address, for RF configuration registers.
cp_rdy	1	O	When a read/write is ongoing, cp_rdy is de-inserted low. Otherwize, it is inserted high.
cp_w	1	I	Control write signal.
cp_w_dat	8	I	Control write data is presented when cp_w is inserted.
cp_r	1	I	Control read signal.
cp_r_dat	8	O	Control read data is presented when cp_r_dat_val is inserted.
cp_r_dat_val	1	O	Control read data valid.
JESD207 Control Plane interface			
cp_clk	1	O	Control plane output serial clock.
cp_cs	1	O	Control plane chip select signal, active low.
mosi	1	O	Master output slave input. *Only for 4-wire SPI control plane interface.
miso	1	I	Master input slave output. *Only for 4-wire SPI control plane interface.
cpdio	1	IO	Bidirectional control plane data signal. *Only for 3-wire SPI control plane interface.

Timing description

The data path timing for transmit and receive operations are shown in the following figures.

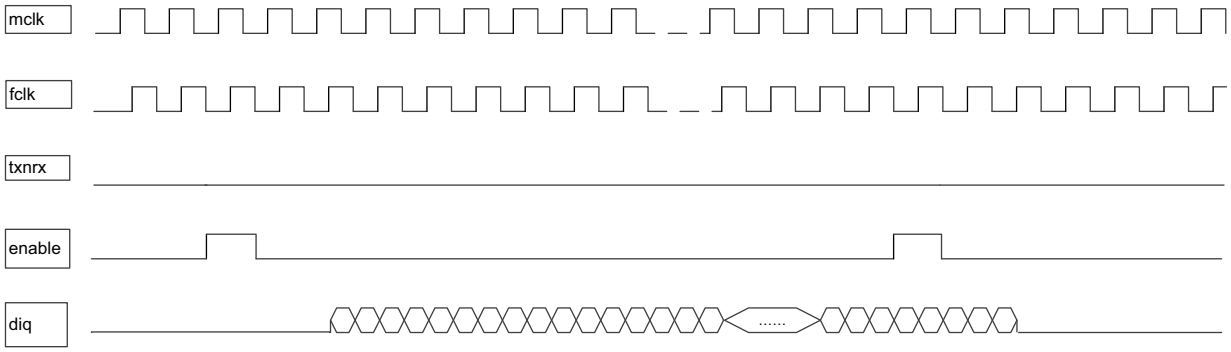
Figure 2-4. JESD207 Transmit Burst



During a transmit burst, the JESD207 IP drives the data values on **diq.** **diq** is presented in the center of **fclk** levels (both of high and low level), and allows the RFIC to use **fclk** to capture **diq**.

The transmit burst start latency is 2.25 **fclk** cycles.

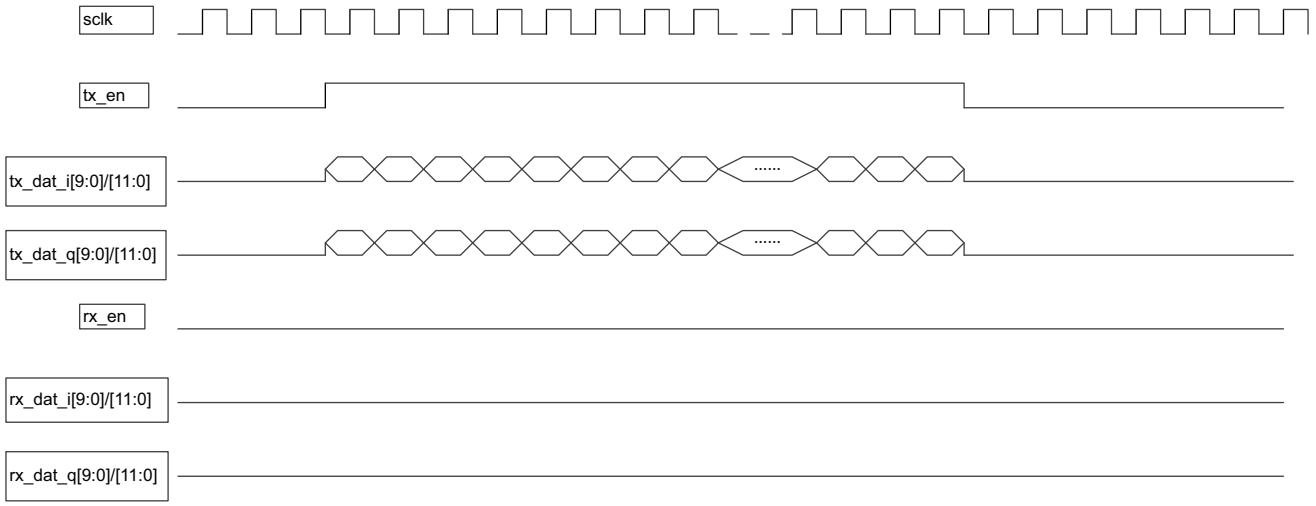
Figure 2-5. JESD207 Receive Burst



During a receive burst, the RFIC drives the data values on **diq.** **diq** is presented in the center of **mclk** levels (both of high and low level), and allows the JESD207 IP to use **mclk** to capture **diq**.

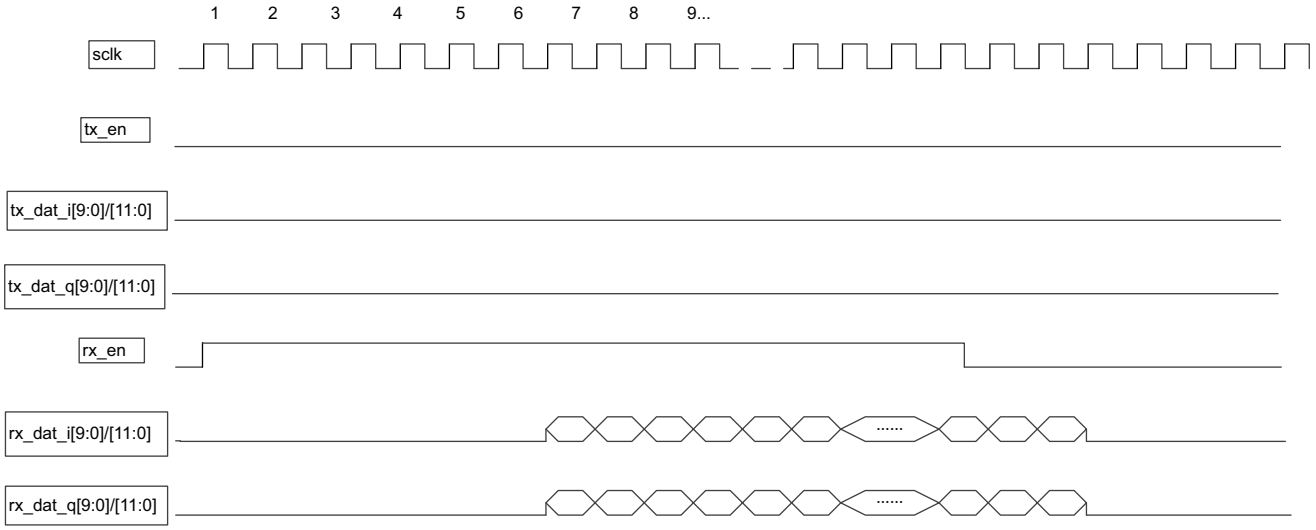
The receive burst start latency is 2 **fclk** cycles.

Figure 2-6. BB Data Interface Transmit Burst



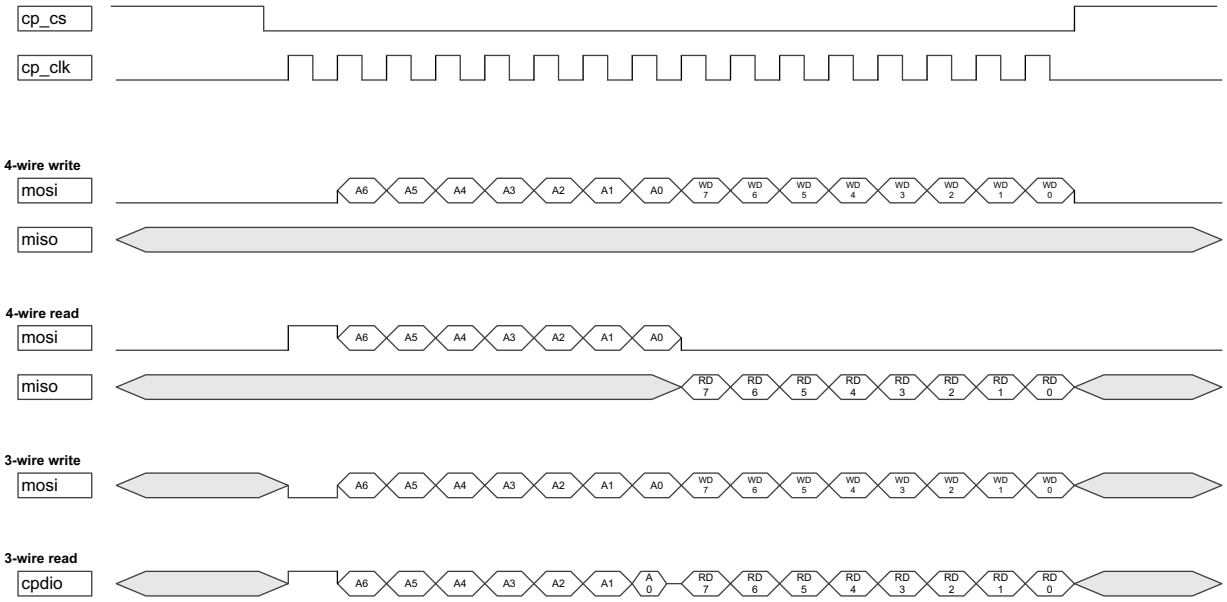
During a transmit burst, **tx_dat_i** and **tx_dat_q** is presented at the falling edge of **sclk** when **tx_en** is active high. If **tx_en** is inactive low, **tx_dat_i** and **tx_dat_q** will be ignored.

Figure 2-7. BB Data Interface Receive Burst



During a receive burst, **rx_dat_i** and **rx_dat_q** is presented at the rising edge of **sclk** with 8 clock cycles latency after **rx_en** is active high.

Figure 2-8. JESD207 Control Plane Interface Timing Sequence



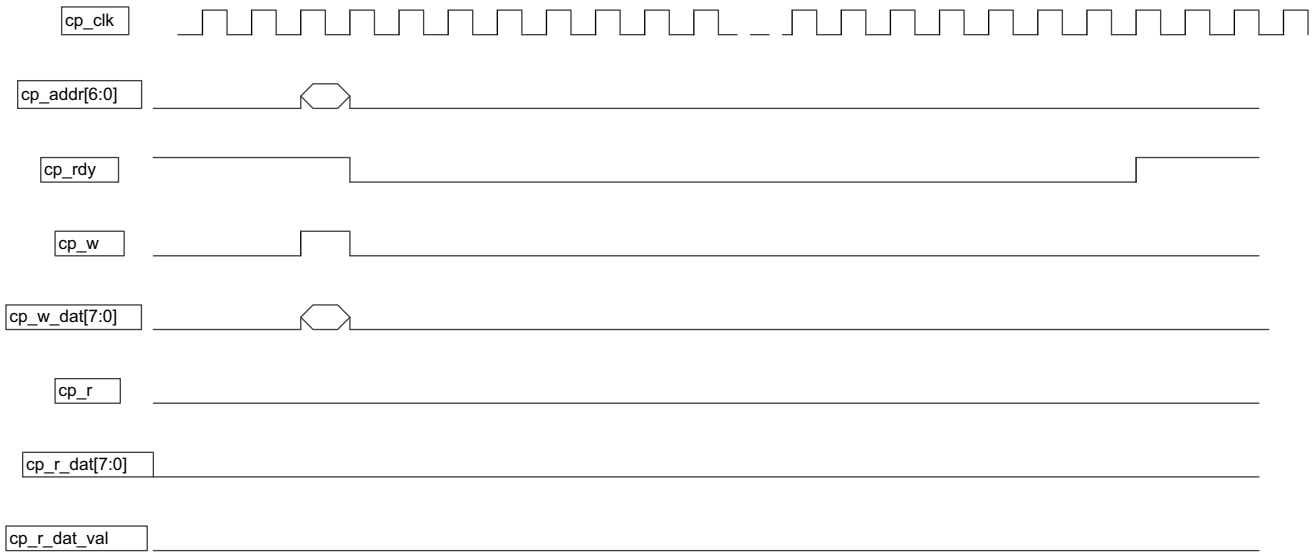
JESD207 control plane interface follows SPI standard. The grey part in the figure meas ‘don’t care’.

A6~A0 are address bits, WD7~WD0 are write data bits, and RD7~RD0 are read data bits.

During a SPI transaction, command/address/data are presented on the bus in order. Command and address is driven by the master device (JESD207 IP). And data is driven by the master device (JESD207 IP) when write transaction, is driven by the slave device (RFIC) when read transaction.

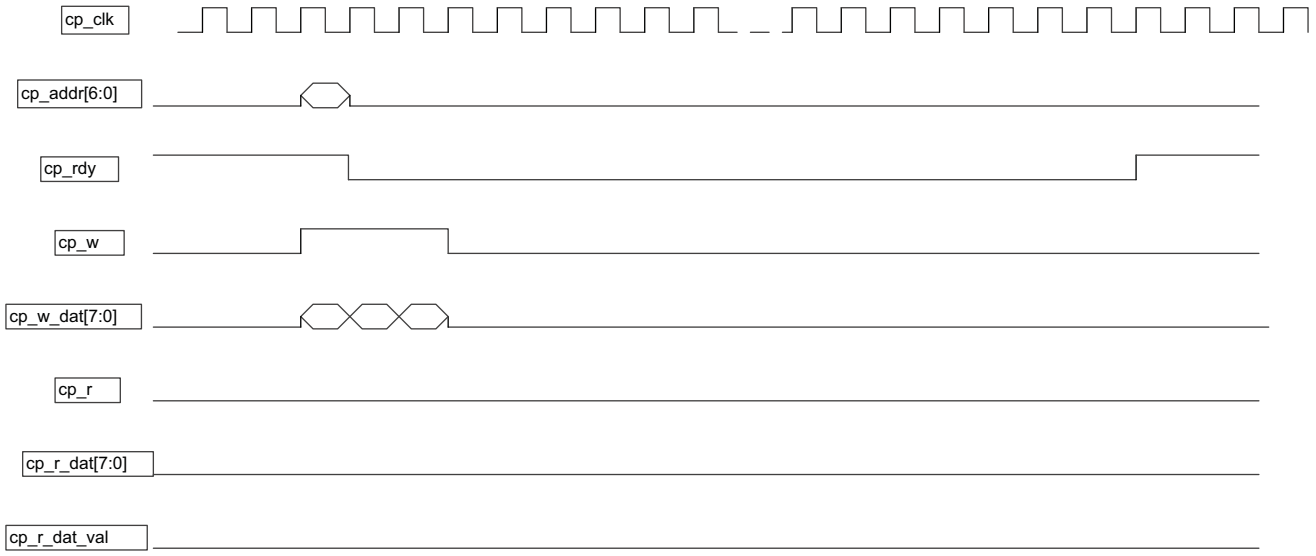
As 3-wire SPI, cpdio is no driven after A0 for a while.

Figure 2-9. BB Control Plane Single Write Transaction



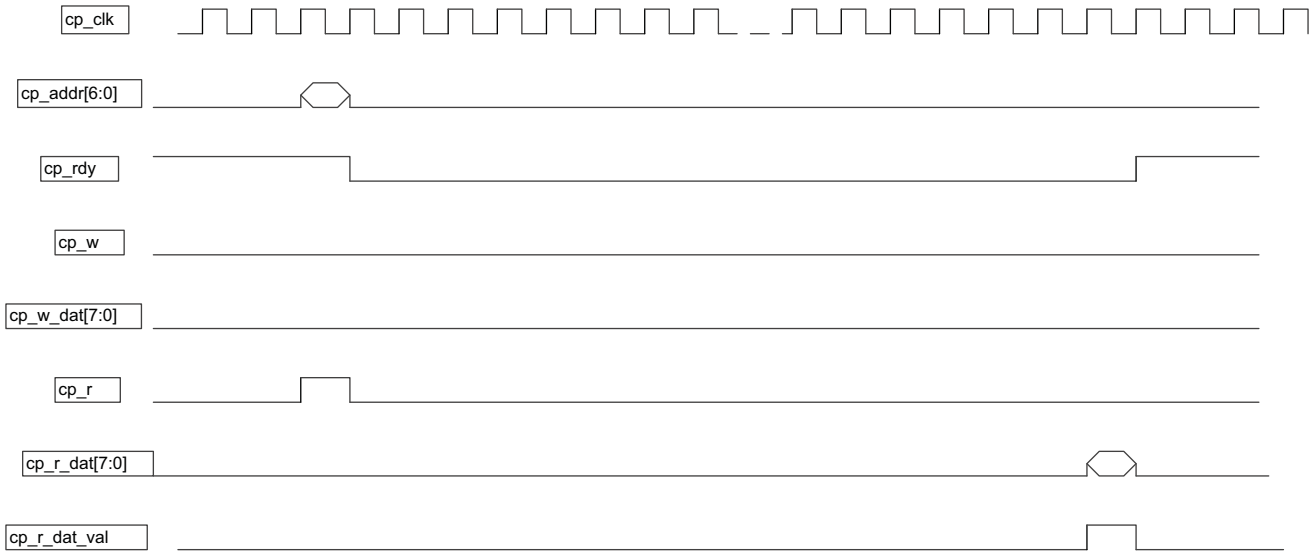
During control plane single write transaction, **cp_addr**/**cp_w_dat** is presented with **cp_w** active high when **cp_rdy** is active high. If **cp_rdy** is low, any transaction is not allowed to be initiated.

Figure 2-10. BB Control Plane Burst Write Transaction



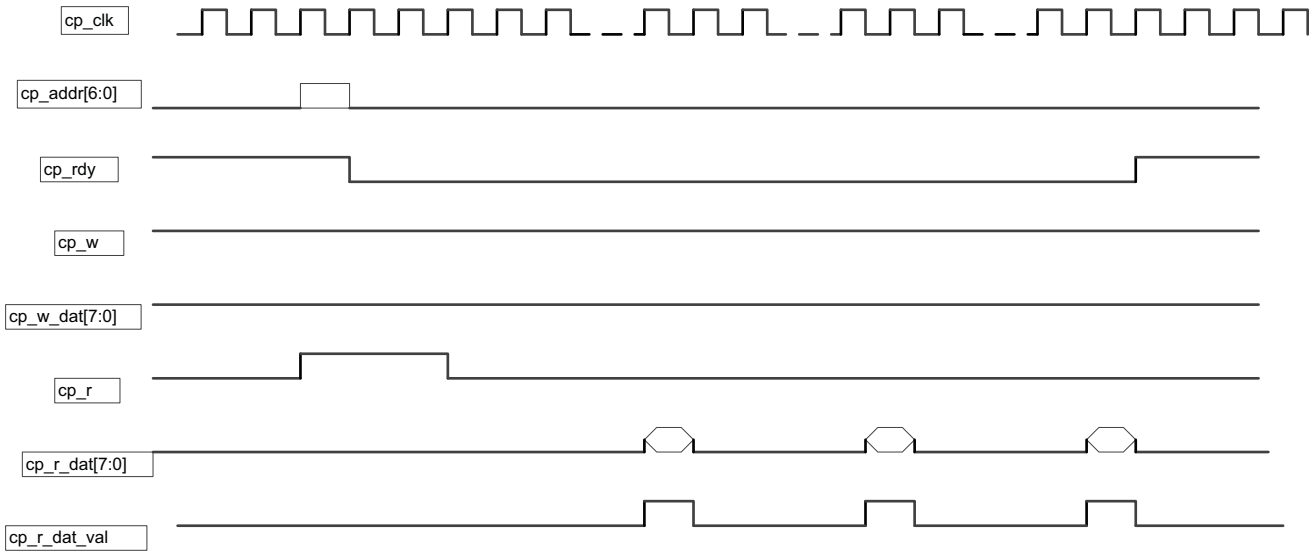
During control plane burst write transaction, **cp_addr** and first **cp_w_dat** is presented with cp_w active high when **cp_rdy** is active high, and **cp_w_dat** is consecutive with **cp_w high**.

Figure 2-11. BB Control Plane Single Read Transaction



During control plane single read transaction, **cp_addr** is presented with **cp_w** active high when **cp_rdy** is active high. As read response, **cp_r_dat** will be presented with **cp_r_dat_val** active high.

Figure 2-12. BB Control Plane Burst Read Transaction



During control plane burst read transaction, cp_r is consecutive high when **cp_rdy** is active high. **cp_addr** is presented with the first **cp_r** high cycle. As read response, **cp_r_dat** will be presented with **cp_r_dat_val** active high.

This section describes how to generate the Lattice JESD207 IP core using the Diamond IPexpress tool. Refer to IP Core Generation and Evaluation for a description of how to generate the IP.

The Lattice JESD207 configuration GUI is accessed via the IPexpress tool and provides an interface for setting the desired parameters and invoking the IP core generator. Since the values of some parameters affect the size of the resultant core, the maximum value for these parameters may be limited by the size of the target device. Table 3-1 provides a list of user configurable parameters for the Lattice JESD207 core.

Table 3-1. Lattice JESD207 IP Core Parameters

Parameter	Range/Options	Default
Data Path width	10, 12	10
Control Plane support	No, Yes	No
Control Plane data format	4-wire, 3-wire	4-wire

Implementation

The Implementation tab provides settings for JESD207 structure and synthesis options.

Figure 3-1. Implementation Tab (Without Control Plane Support as Default)

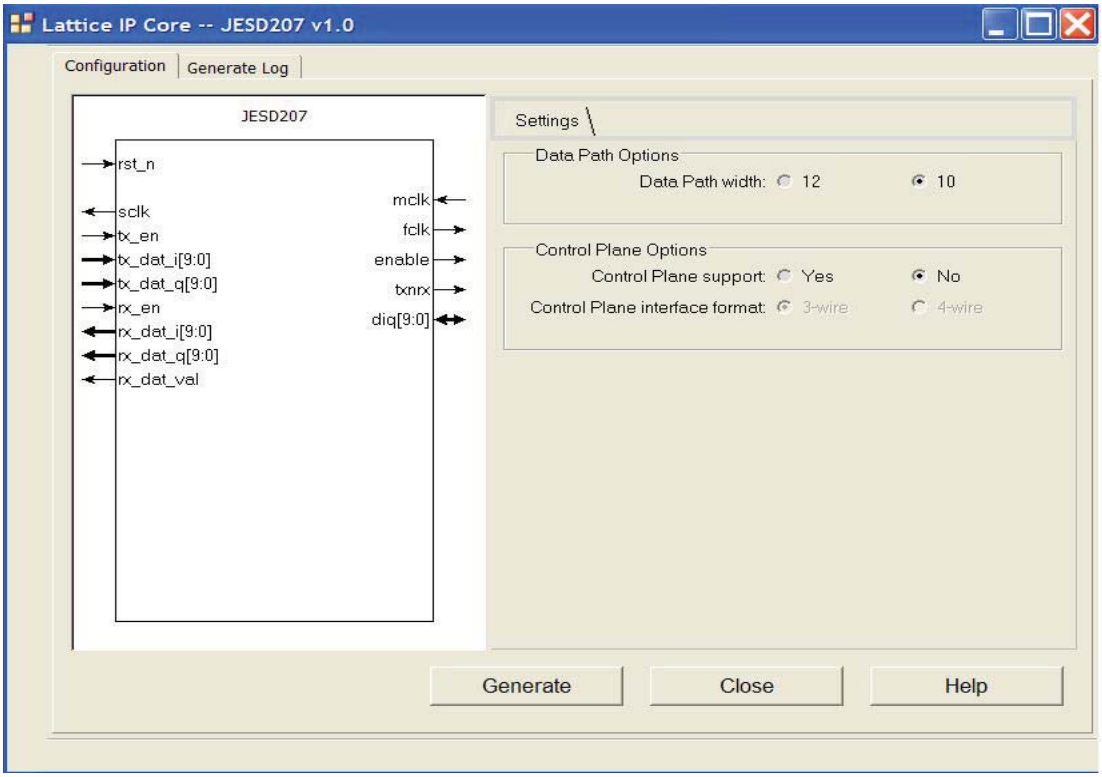


Figure 3-2. Implementation Tab (With 4-Wire Control Plane Support)

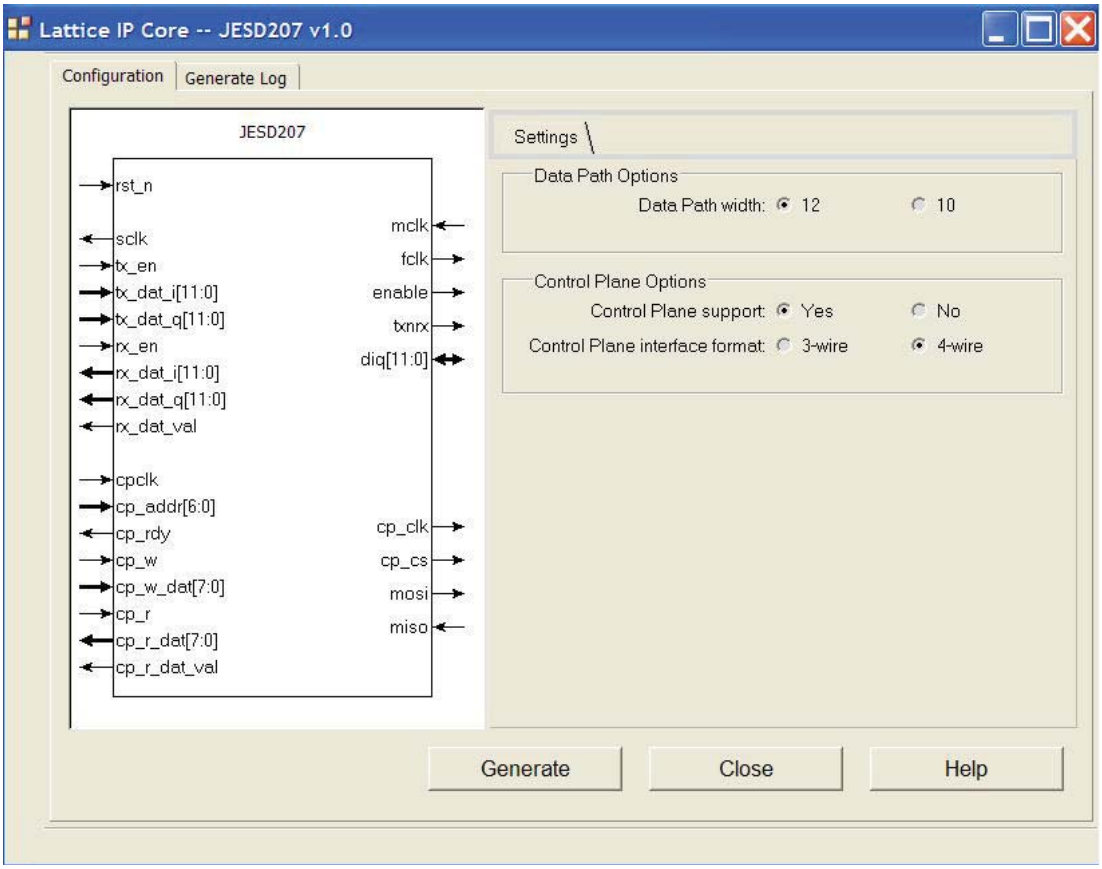
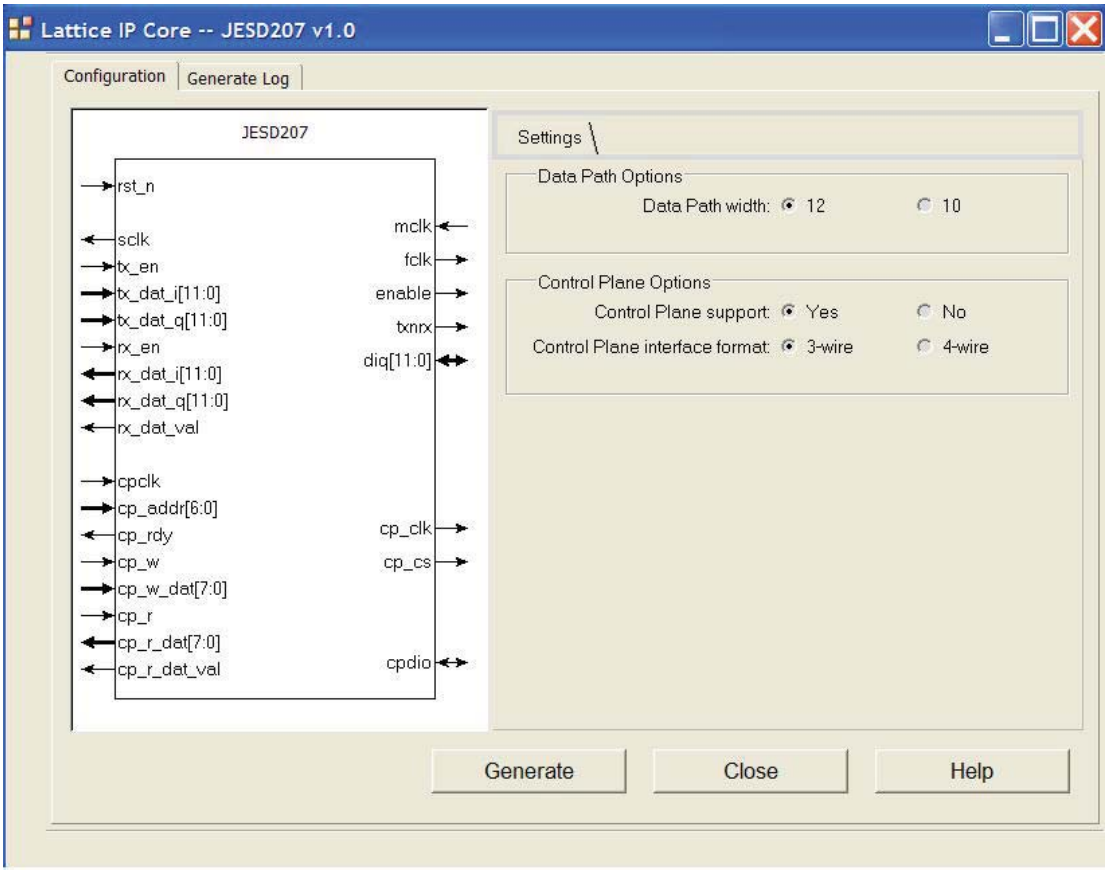


Figure 3-3. Implementation Tab (With 3-Wire Control Plane Support)



Implementation Note: The PLL module mclk2sclk generated with the IP is for an mclk frequency of 90 MHz. If the mclk in the user's design is having a different frequency, the module mclk2sclk has to be regenerated using IP Express. mclk2sclk.v is in \<project_dir>\jesd207_eval\<username>\src\rtl\template\ecp3.

IP Core Generation and Evaluation

This section provides information on how to generate the Lattice JESD207 IP core using the Diamond IPexpress tool, and how to include the core in a top-level design.

Licensing the IP Core

An IP core- and device-specific license is required to enable full, unrestricted use of the Lattice JESD207 IP core in a complete, top-level design. Instructions on how to obtain licenses for Lattice IP cores are given at:

www.latticesemi.com/products/intellectualproperty/aboutip/index.cfm.

Users may download and generate the Lattice JESD207 IP core and fully evaluate the core through functional simulation and implementation (synthesis, map, place and route) without an IP license. The JESD207 IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core which operate in hardware for a limited time (approximately four hours) without requiring an IP license. See Hardware Evaluation for further details. However, a license is required to enable timing simulation, to open the design in the Diamond and to generate bitstream file that do not include the hardware evaluation timeout limitation.

Getting Started

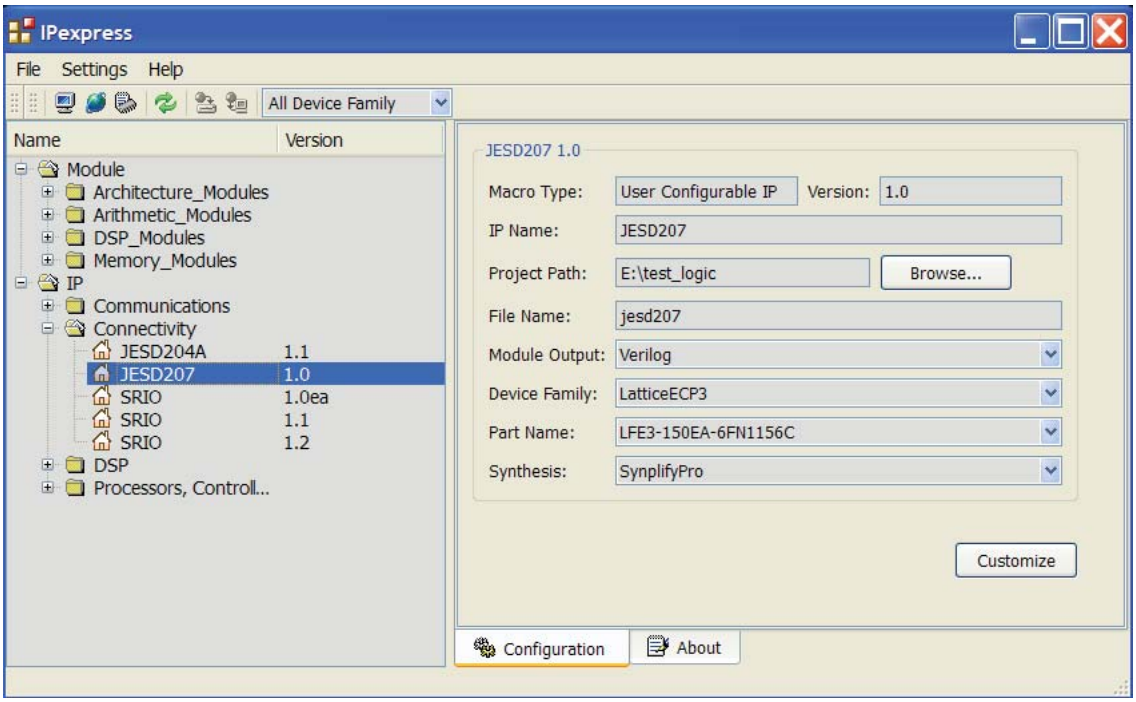
The JESD207 IP core is available for download from the Lattice IP Server using the IPexpress tool. The IP files are automatically installed using ispUPDATE technology in any customer-specified directory. After the IP core has been installed, the IP core will be available in the IPexpress GUI dialog box shown in Figure 4-1. To generate a specific IP core configuration, the user specifies:

- Project Path – Path to the directory where the generated IP files will be located.
- File Name – "username" designation given to the generated IP core and corresponding folders and files.
- Module Output – Verilog or VHDL.
- Device Family – Device family to which IP is to be targeted (e.g. Lattice ECP2M, LatticeECP3, etc.). Only families that support the particular IP core are listed.
- Part Name – Specific targeted part within the selected device family.

Configuring JESD207 Core in IPexpress

The JESD207 configuration GUI is accessed via the Diamond IPexpress tool, and provides an interface for setting the desired parameters and invoking the IP core generator. The start-up IPexpress page allows the user to select the IP to be generated, project directory, user designated module name, design entry type, and target device. The "File Name" will be used as username in the core generation. The JESD207 IP core is found under IP->Connectivity, as shown below.

Figure 4-1. IPexpress Dialog Box

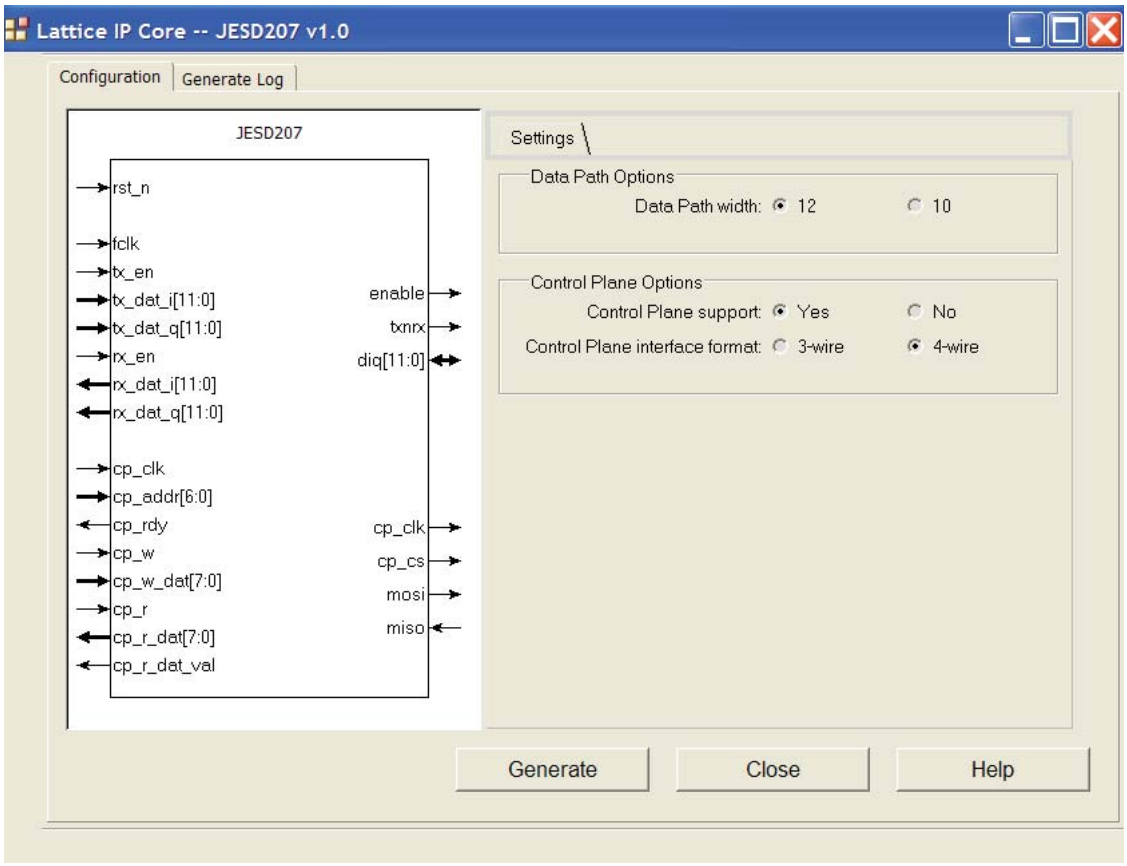


Note: File Name cannot be “jesd207_core,” as this name has been used in the internal design of the core.

If the IPexpress tool is called from within an existing project, Project Path, Module Output, Device Family and Part Name default to the specified project parameters. Refer to the IPexpress tool online help for further information.

To create a custom configuration, the user clicks the Customize button in the IPexpress tool dialog box to display JESD207 IP core Configuration GUI, as shown in Figure 4-2. From this dialog box, the user can select the IP parameter options specific to their application.

Figure 4-2. Configuration GUI



IPexpress-Created Files and Top Level Directory Structure

When the user clicks the Generate button in the IP Configuration dialog box, the IP core and supporting files are generated in the specified “Project Path” directory. The directory structure of the generated files is shown in Figure 4-3. This example shows the directory structure generated with JESD207 for LatticeECP3 device.

Figure 4-3. Lattice JESD207 IP Core Directory Structure

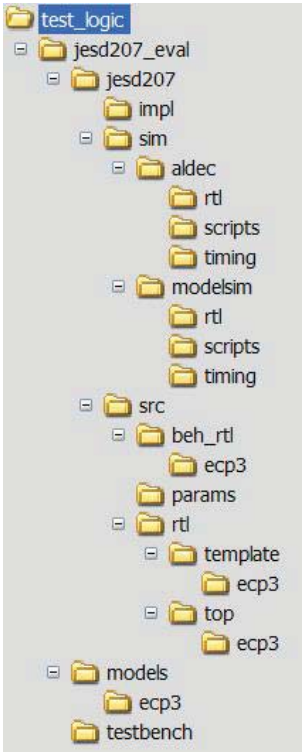


Table 4-1 provides a list of key files and directories created by the IPexpress tool and how they are used. The IPexpress tool creates several files that are used throughout the design cycle. The names of most of the created files are customized to the user's module name specified in the IPexpress tool.

Table 4-1. File List

File	Description
<username>.lpc	This file contains the IPexpress tool options used to recreate or modify the core in the IPexpress tool.
<username>.ipx	The IPX file holds references to all of the elements of an IP or Module after it is generated from the IPexpress tool. The file is used to bring in the appropriate files during the design implementation and analysis. It is also used to re-load parameter settings into the IP/Module generation GUI when an IP/Module is being re-generated.
<username>.ngo	This file provides the synthesized IP core.
<username>_bb.v	This file provides the synthesis black box for the user's synthesis.
<username>_inst.v	This file provides an instance template for JESD207 IP core.
<username>_beh.v	This file provides the front-end simulation library for JESD207 IP core.

Table 4-2 provides a list of key additional files providing IP core generation status information and command line generation capability are generated in the user's project directory.

Table 4-2. Additional Files

File	Description
<username>_generate.tcl	This file is created when the GUI "Generate" button is pushed. This file may be run from command line.
<username>_generate.log	This is the synthesis and map log file.
<username>_gen.log	This is the IPexpress IP generation log file.

Instantiating the Core

The generated JESD207 IP core package includes black-box (<username>_bb.v) and instance (<username>_inst.v) templates that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file that can be used as an instantiation template for the IP core is provided in \<project_dir>\jesd207_eval\<username>\src\rtl\top. Users may also use this top-level reference as the starting template for the top-level for their complete design.

Running Functional Simulation

Simulation support for JESD207 IP core is provided for Aldec Active-HDL (Verilog and VHDL) simulator, Mentor Graphics ModelSim simulator. The functional simulation includes a configuration-specific behavioral model of JESD207 IP core. The test bench sources stimulus to the core, and monitors output from the core. The generated IP core package includes the configuration-specific behavior model (<username>_beh.v) for functional simulation in the “Project Path” root directory. The simulation scripts supporting ModelSim evaluation simulation is provided in \<project_dir>\jesd207_eval\<username>\sim\modelsim\scripts. The simulation script supporting Aldec evaluation simulation is provided in \<project_dir>\ jesd207_eval\<username>\sim\aldec\scripts. Both Modelsim and Aldec simulation is supported via test bench files provided in \<project_dir>\ jesd207_eval\testbench. Models required for simulation are provided in the corresponding \models folder. Users may run the Aldec evaluation simulation by doing the following:

1. Open Active-HDL.
2. Under the Tools tab, select **Execute Macro**.
3. Browse to folder \<project_dir>\jesd207_eval\<username>\sim\aldec\scripts and execute one of the "do" scripts shown.

Users may run the Modelsim evaluation simulation by doing the following:

1. Open ModelSim.
2. Under the File tab, select **Change Directory** and choose the folder <project_dir>\jesd207_eval\<username>\sim\modelsim\scripts.
3. Under the Tools tab, select **Execute Macro** and execute \scripts\<username>_rtl_se.do.

Synthesizing and Implementing the Core in a Top-Level Design

Synthesis support for JESD207 IP core is provided for Synopsys Synplify. The JESD207 IP core itself is synthesized and is provided in NGO format when the core is generated in IPexpress. Users may synthesize the core in their own top-level design by instantiating the core in their top-level as described previously and then synthesizing the entire design with either Synplify or Precision RTL synthesis.

The top-level files <username>_ top.v provided in \<project_dir>\jesd207_eval\<username>\src\top support the ability to implement JESD207 core in isolation. Push-button implementation of this top-level design with either Synplify or Precision RTL Synthesis is supported via the project files <username>_eval.ldf located in the \<project_dir>\ jesd207_eval\<username>\impl.

To use this project file in Diamond:

1. Choose **File** > **Ope**n > **Projec**t.
2. Browse to \<project_dir>\ jesd207_eval\<username>\impl\ in the Open Project dialog box.
3. Select and open <username>_top.ldf. At this point, all of the files needed to support top-level synthesis and implementation will be imported to the project.
4. Select the **Process** tab in the left-hand GUI window.

5. Implement the complete design via the standard Diamond GUI flow.

Hardware Evaluation

The JESD207 IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs.

Choose **Project > Active Strategy > Translate Design Settings**. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default.

Updating/Regenerating the IP Core

By regenerating an IP core with the IPexpress tool, you can modify any of its settings including device type, design entry method, and any of the options specific to the IP core. Regenerating can be done to modify an existing IP core or to create a new but similar one.

Regenerating an IP Core in Diamond

To regenerate an IP core in Diamond:

1. In IPexpress, click the **Regenerate** button.
2. In the Regenerate view of IPexpress, choose the IPX source file of the module or IP you wish to regenerate.
3. IPexpress shows the current settings for the module or IP in the Source box. Make your new settings in the **Target** box.
4. If you want to generate a new set of files in a new location, set the new location in the **IPX Target File** box. The base of the file name will be the base of all the new file names. The IPX Target File must end with an .ipx extension.
5. Click **Regenerate**. The module's dialog box opens showing the current option settings.
6. In the dialog box, choose the desired options. To get information about the options, click Help. Also, check the About tab in IPexpress for links to technical notes and user guides. IP may come with additional information. As the options change, the schematic diagram of the module changes to show the I/O and the device resources the module will need.
7. To import the module into your project, if it's not already there, select **Import IPX to Diamond Project** (not available in stand-alone mode).
8. Click **Generate**.
9. Check the Generate Log tab to check for warnings and error messages.
10. Click **Close**.

The IPexpress package file (.ipx) supported by Diamond holds references to all of the elements of the generated IP core required to support simulation, synthesis and implementation. The IP core may be included in a user's design by importing the .ipx file to the associated Diamond project. To change the option settings of a module or IP that is already in a design project, double-click the module's .ipx file in the File List view. This opens IPexpress and the module's dialog box showing the current option settings. Then go to step 6.

Support Resources

This chapter contains information about Lattice Technical Support, additional references, and document revision history.

Lattice Technical Support

There are a number of ways to receive technical support.

E-mail Support

techsupport@latticesemi.com

Local Support

Contact your nearest Lattice sales office.

Internet

www.latticesemi.com

JEDEC Website

The JEDEC website contains specifications and documents referred to in this user's guide. The JEDEC URL is:

http://www.jedec.org

References

JESD207 Standard

- JEDEC STANDARD Radio Front End - Baseband Digital Parallel (RBDP) Interface JESD207, March 2007.

LatticeECP3

- HB1009, LatticeECP3 Family Handbook

Revision History

Date	Document Version	IP Core Version	Change Summary
August 2013	01.0	1.0	Initial release.

Resource Utilization

This appendix provides resource utilization information for Lattice FPGAs using the JESD207 IP core.

IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the Diamond design tools. Details regarding the usage of IPexpress can be found in the IPexpress and Diamond help system. For more information on the Diamond design tools, visit the Lattice web site at www.latticesemi.com//Products/DesignSoftware.

LatticeECP3 Devices

Table A-1. Performance and Resource Utilization[1]

DP_WIDTH	CP_SUPPORT	CP_WIRES	Register	LUTs	Slices	Fmax
10	Yes	4	219	318	233	118.666
10	Yes	3	208	314	219	118.666
12	Yes	4	239	322	243	118.977
12	Yes	3	239	323	244	121.788

1. Performance and utilization data are generated targeting a LFE3-17EA-7FTN256C device using Lattice Diamond 2.0 and Synplify Pro F-2012.03L software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

Ordering Part Number

The Ordering Part Number (OPN) for JESD207 IP core targeting LatticeECP3 devices is JESD207-E3-U1.