# EMI2124

# Single Pair Common Mode Filter with ESD Protection

**ON Semiconductor®**

**http://onsemi.com**

### Description

The EMI2124 is an integrated common mode filter providing both ESD protection and EMI filtering for high speed serial digital interfaces such as USB2.0.

The EMI2124 provides EMI filtering for one differential data line pair and ESD protection for one data pair plus USB ID pin. It provides a separate Vbus line protection typically used for charging. It is supplied in a small RoHS-compliant WDFN8 package.

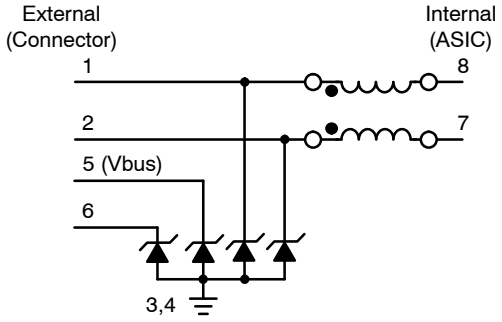
### Features

- Highly Integrated Common Mode Filter (CMF) with ESD Protection provides protection and EMI Reduction for systems using high speed Serial Data Lines with cost and space savings over Discrete Solutions
- Large Differential Mode Bandwidth with Cutoff Frequency > 2 GHz
- High Common Mode Stop Band Attenuation: >25 dB at 700 MHz, >30 dB at 800 MHz Typical
- Provides Data Lines ESD Protection to IEC61000-4-2 Level 4, ±12 kV Contact Discharge
- Provides $V_{ID}$ & $V_{BUS}$ ESD Protection to IEC61000-4-2 Level 4, ±30 kV Contact Discharge
- Low Channel Input Capacitance provides Superior Impedance Matching Performance
- Low Profile Package with Small Footprint in WDFN8 2.0 mm length x 2.2 mm width x 0.75 mm height Pb−Free Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

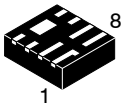
### Applications

- USB2.0 and other High Speed Differential Data Lines in Mobile Phones and Digital Still Cameras
- MIPI D−PHY

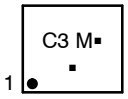
### SIMPLIFIED SCHEMATIC




### MARKING DIAGRAM



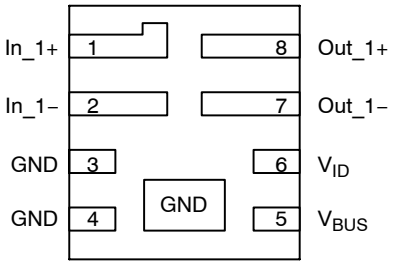

**WDFN8**
**CASE 511BN**




C3 = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

### PIN CONNECTIONS




(Top View)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| EMI2124MTTAG | WDFN8 (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## PIN DESCRIPTION

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 1 | In_1+ | I/O | CMF Channel 1+ to Connector (External) |
| 2 | In_1− | I/O | CMF Channel 1− to Connector (External) |
| 8 | Out_1+ | I/O | CMF Channel 1+ to ASIC (Internal) |
| 7 | Out_1− | I/O | CMF Channel 1− to ASIC (Internal) |
| 5 | $V_{BUS}$ | I/O | Supply Protection to Connector − $V_{BUS}$ (External − $V_{BUS}$) |
| 6 | $I_D$ | I/O | Supply Protection to Connector (External − $V_{ID}$) |
| 3,4 | GND | GND | Ground |

## MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise stated)

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Operating Temperature Range | $T_{OP}$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{STG}$ | −65 to +150 | °C |
| Maximum Lead Temperature for Soldering Purposes (1/8” from Case for 10 Seconds) | $T_L$ | 260 | °C |
| DC Current per Line | $I_{LINE}$ | 100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Channel Leakage Current | $I_{LEAK}$ | $T_A$ = 25°C, $V_{IN}$ = 5 V, GND = 0 V | | | 1.0 | μA |
| Channel Negative Voltage | $V_F$ | $T_A$ = 25°C, $I_F$ = 10 mA | 0.1 | | 1.5 | V |
| Channel Input Capacitance to ground (Pins 1,2,8,7 to GND) | $C_{IN}$ | $T_A$ = 25°C, At 1 MHz, GND = 0 V, $V_{IN}$ = 1.65 V | | 0.8 | 1.3 | pF |
| Channel Resistance (Pins 1−8, 2−7) | Rch | | | 8.0 | | Ω |
| Differential Mode Cut − Off Frequency | $f_{3dB}$ | 50 Ω source and load termination | | 2.0 | | GHz |
| Common Mode Stop Band Attenuation | $F_{atten}$ | @ 800 MHz | | 30 | | dB |
| In−system ESD Withstand Voltage<br>a) Contact discharge per IEC 61000−4−2 standard, Level 4 **(External Pins − Pin1, Pin2)**<br>b) Contact discharge per IEC 61000−4−2 standard, Level 1 **(Internal Pins)**<br>c) Contact discharge per IEC 61000−4−2 standard, Level 4 **(External Pins − $V_{BUS}$, $V_{ID}$)** | $V_{ESD}$ | (Notes 1 and 2) | <br>±12<br><br>±2<br><br>±30 | | | kV |
| TLP Clamping Voltage − pin1, pin2 (See Figure 10) | $V_{CL}$ | Forward $I_{PP}$ = 8 A<br>Forward $I_{PP}$ = 12 A<br>Reverse $I_{PP}$ = −8 A<br>Reverse $I_{PP}$ = −12 A | | 13<br>16<br>−6<br>−8.5 | | V<br>V<br>V<br>V |
| TLP Clamping Voltage − $V_{BUS}$ (See Figure 11) | $V_{CL}$ | Forward $I_{PP}$ = 8 A<br>Forward $I_{PP}$ = 12 A<br>Reverse $I_{PP}$ = −8 A<br>Reverse $I_{PP}$ = −12 A | | 23<br>25<br>−4<br>−5.4 | | V<br>V<br>V<br>V |
| Reverse Working Voltage (Pins 1,2,8,7 and 6) | $V_{RWM}$ | (Note 3) | | | 5.0 | V |
| Breakdown Voltage (Pins 1,2,8,7 and 6) | $V_{BR}$ | $I_T$ = 1 mA; (Note 4) | 5.5 | | 9.0 | V |
| Reverse Working Voltage ($V_{BUS}$) | $V_{RWM(2)}$ | (Note 3) | | | 12 | V |
| Breakdown Voltage ($V_{BUS}$) | $V_{BR(2)}$ | $I_T$ = 1 mA; (Note 4) | 15 | | 16.8 | V |
| Maximum Peak Pulse Current ($V_{ID}$ to GND) | $I_{PP}$ | 8x20 μs Waveform | | | 12 | A |
| Clamping Voltage ($V_{ID}$ to GND) | $V_C$ | IPP = 5 A | | | 10 | V |
| Maximum Peak Pulse Current ($V_{BUS}$ to GND) | $I_{PP(2)}$ | 8x20 μs Waveform | | | 5 | A |
| Clamping Voltage ($V_{BUS}$ to GND) | $V_{C(2)}$ | IPP = 5 A | | 25 | | V |
| Dynamic Resistance<br>Positive Transients<br>Negative Transients | $R_{DYN}$ | $T_A$ = 25C, $I_{PP}$=1 A, $t_P$= 8/20 μs, Any I/O to GND | | <br>0.67<br>0.59 | | <br>Ω<br>Ω |

1. Standard IEC 61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330, GND grounded.
2. These measurements performed with no external capacitor.
3. TVS devices are normally selected according to the working peak reverse voltage ($V_{RWM}$), which should be equal or greater than the DC or continuous peak operating voltage level.
4. $V_{BR}$ is measured at pulse test current $I_T$.

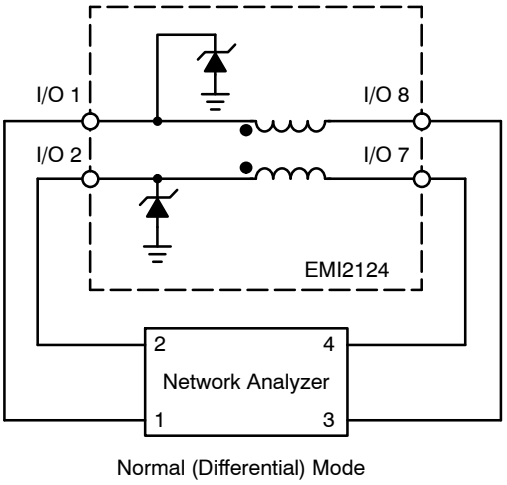



**Figure 1. Normal (Differential) Mode Test Configuration**

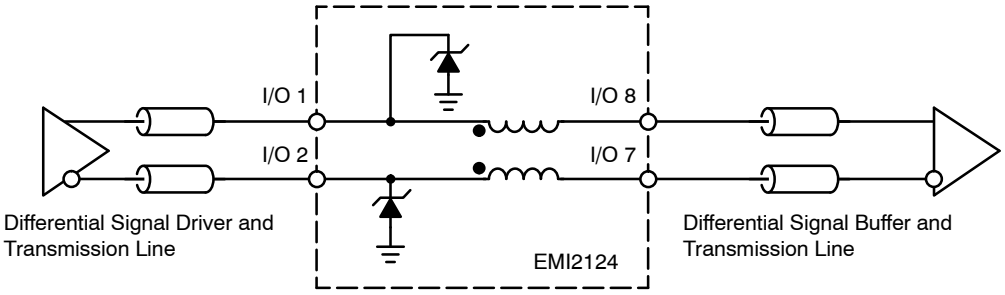



**Figure 2. Application Circuit**

## TYPICAL CHARACTERISTICS

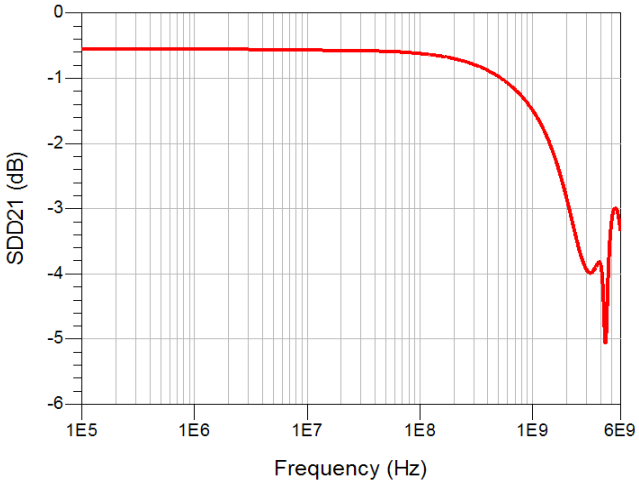



**Figure 3. Differential Mode Attenuation vs. Frequency (Zdiff = 100 Ω)**

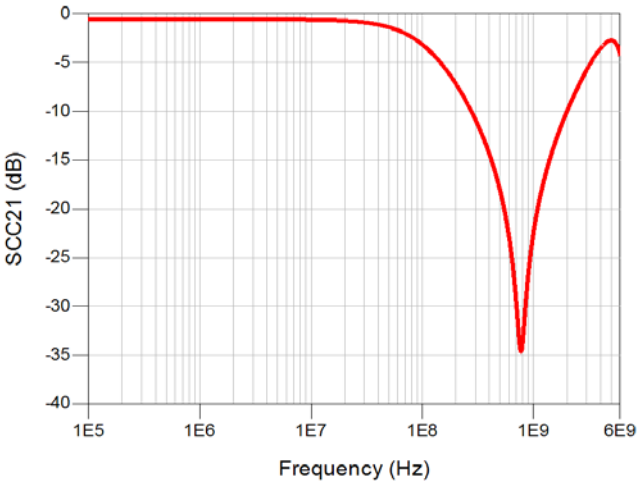



**Figure 4. Common Mode Attenuation vs. Frequency (Zcomm = 50 Ω)**

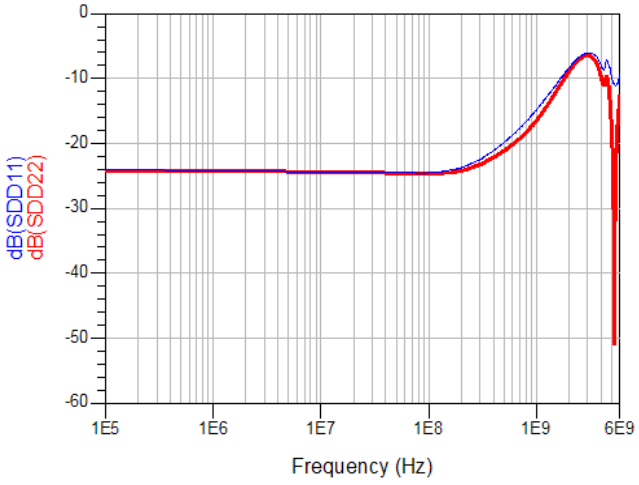



**Figure 5. Differential Return Loss vs. Frequency (Zdiff=100 Ω)**

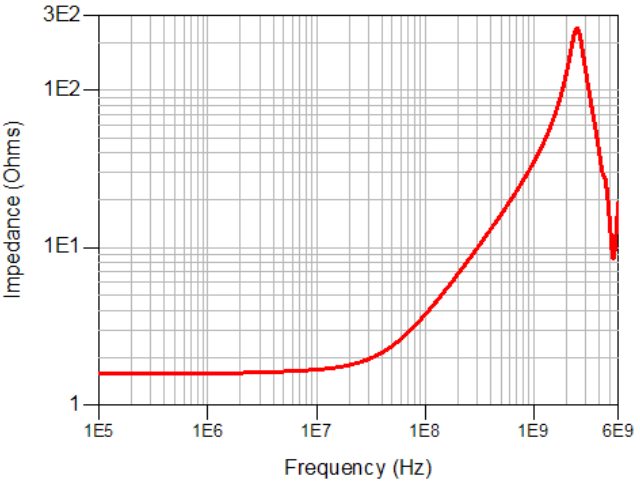



**Figure 6. Differential Impedance vs. Frequency (Zdiff=100 Ω)**

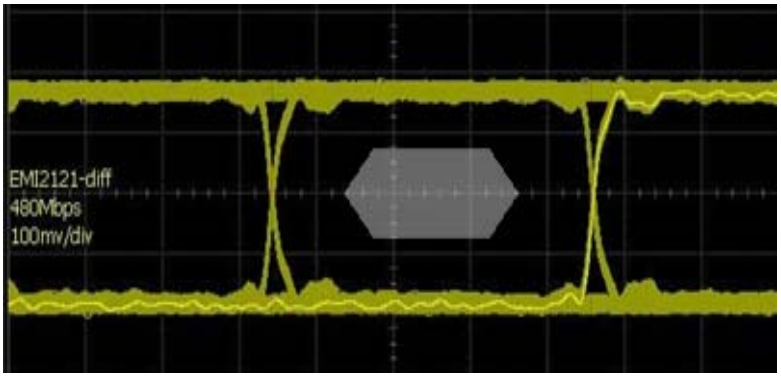



**Figure 7. EMI2124 Measured Eye Diagram @ 480 Mbps**

## Transmission Line Pulse (TLP) Measurements

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10 s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC61000-4-2 current waveform is compared with TLP current pulses at 8 and 16 A. A TLP curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. Typical TLP I-V curves for the EMI2124 are shown in Figure 10.

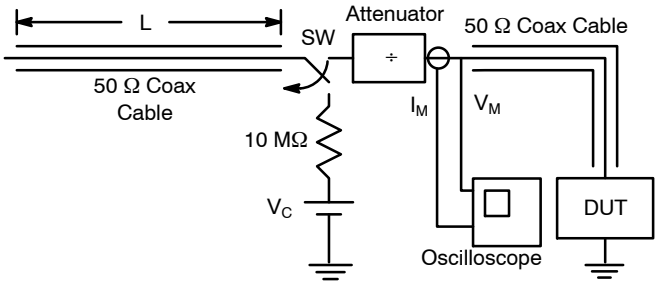



**Figure 8. Simplified Schematic of a Typical TLP System**

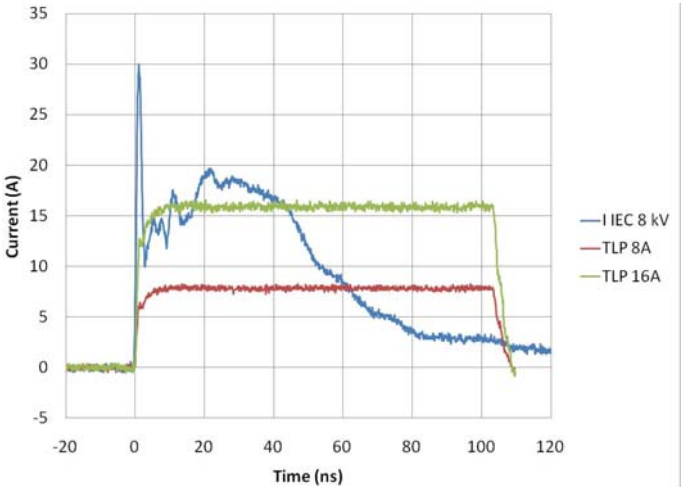



**Figure 9. Comparison Between 8 kV IEC61000−4−2 and 8 A and 16 A TLP Waveforms**

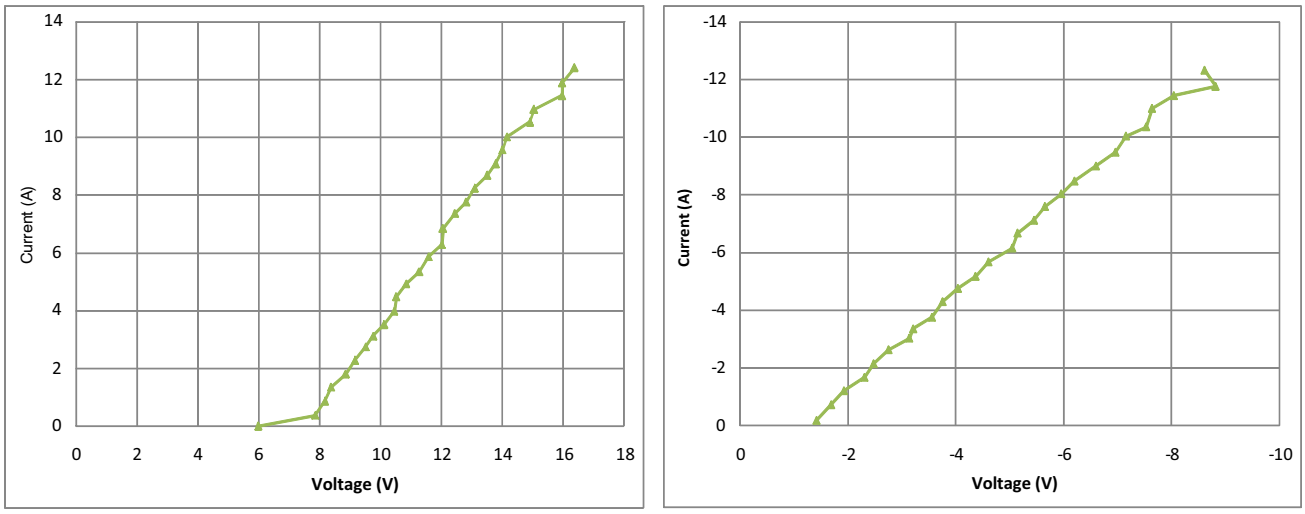



**Figure 10. Positive and Negative TLP Waveforms (Pin1, Pin2)**

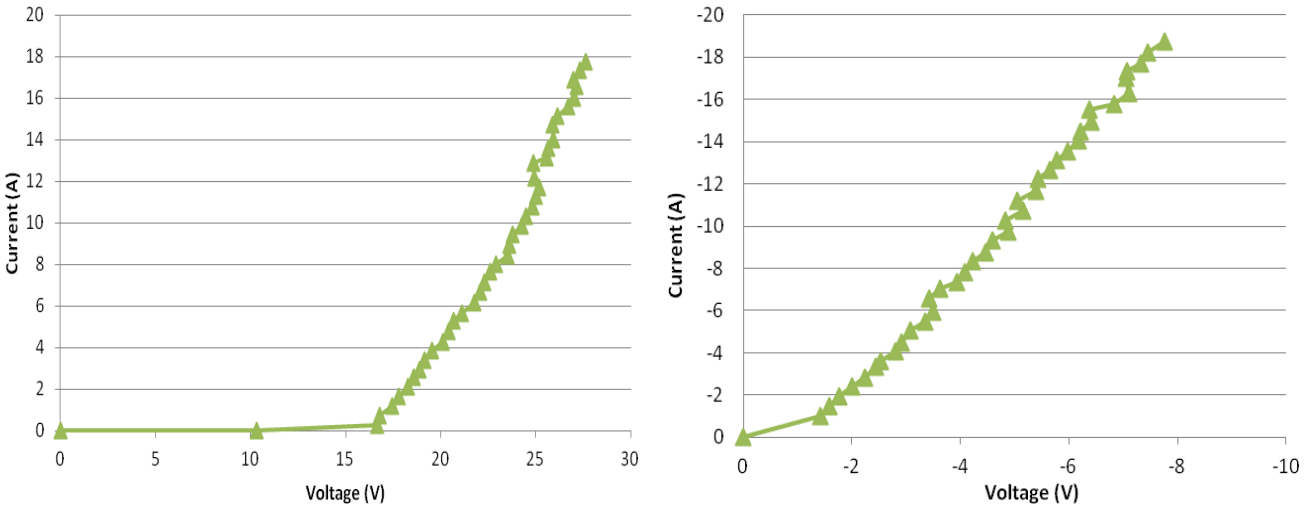


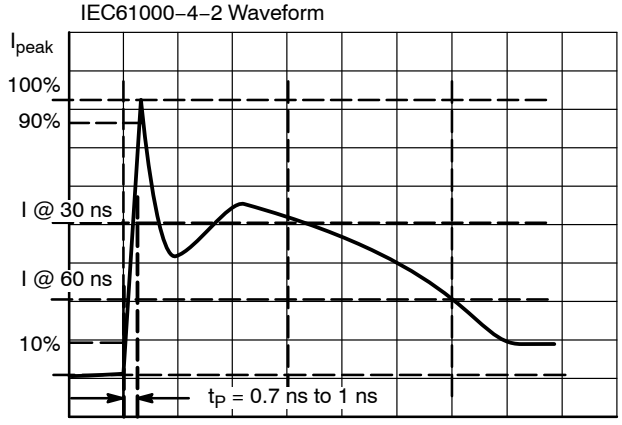

**Figure 11. Positive and Negative TLP Waveforms ($V_{BUS}$)**

## ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to On Semiconductor Application Notes AND8307/D and AND8308/D.

**IEC61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |



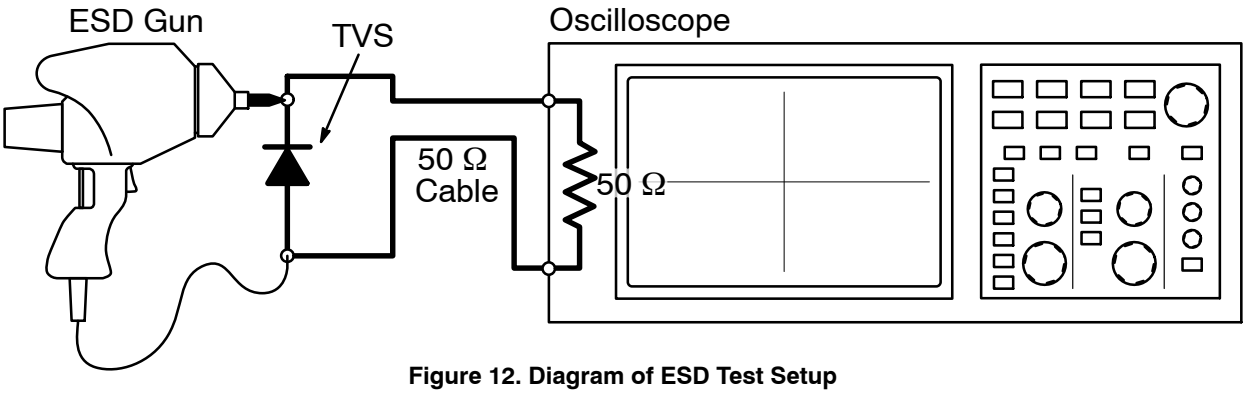




**Figure 12. Diagram of ESD Test Setup**

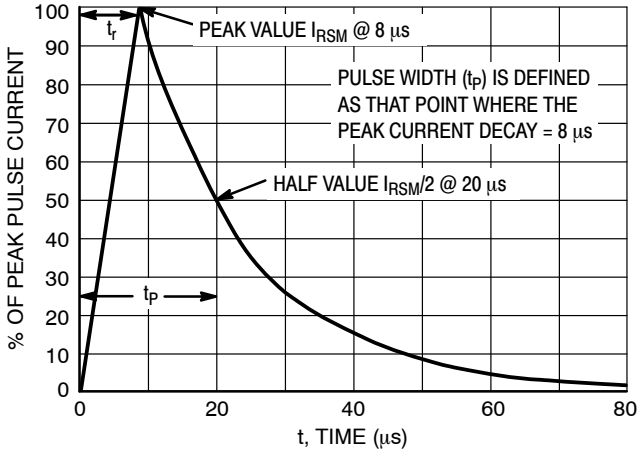



**Figure 13. 8 x 20 μs Pulse Waveform**

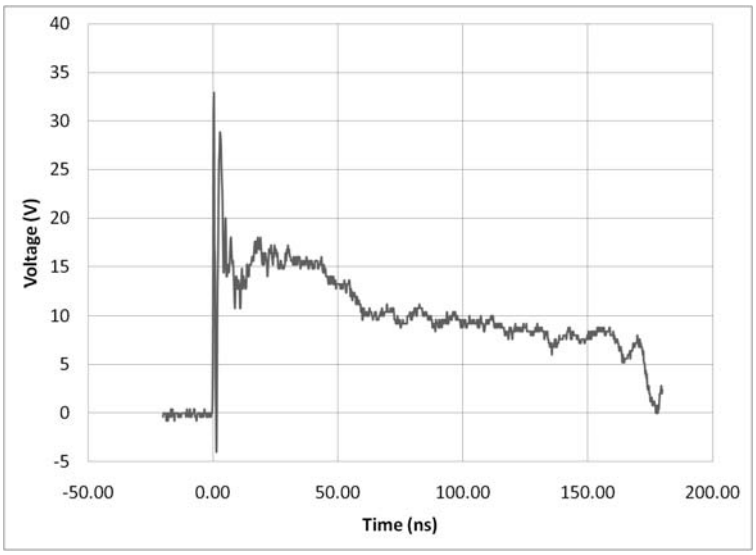



**Figure 14. ESD Clamping Voltage +8 kV per IEC6100−4−2 (external to internal pin)**

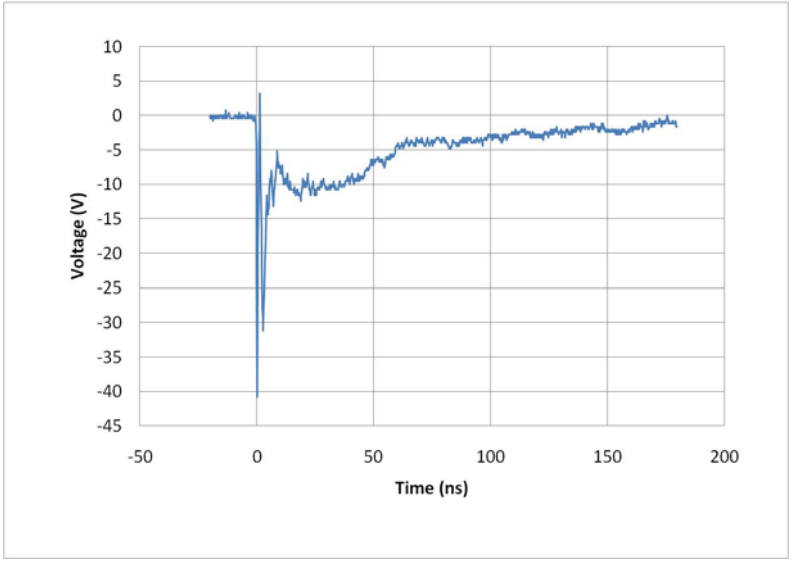


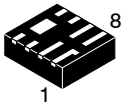

**Figure 15. ESD Clamping Voltage −8 kV per IEC6100−4−2 (external to internal pin)**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

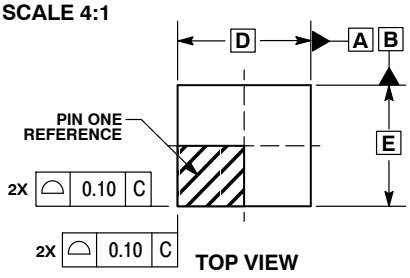
ON Semiconductor®

**WDFN8, 2.2x2, 0.5P**
CASE 511BN
ISSUE A

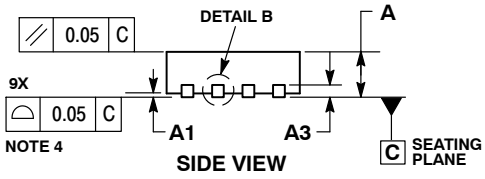
DATE 11 DEC 2012



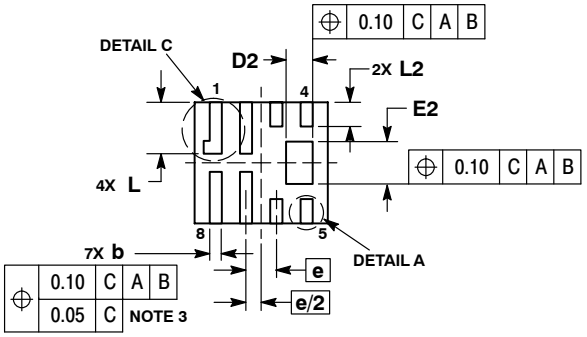

SCALE 4:1



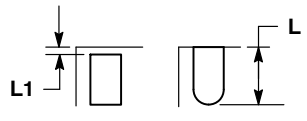

TOP VIEW



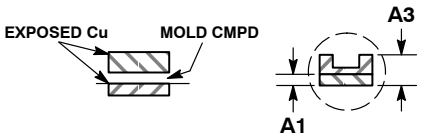

SIDE VIEW



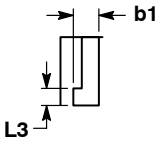

BOTTOM VIEW




DETAIL A
OPTIONAL CONSTRUCTIONS




DETAIL B
OPTIONAL CONSTRUCTIONS

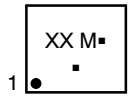



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| b1 | 0.25 | 0.35 |
| D | 2.20 BSC | |
| D2 | 0.34 | 0.54 |
| E | 2.00 BSC | |
| E2 | 0.60 | 0.80 |
| e | 0.50 BSC | |
| L | 0.75 | 0.95 |
| L1 | 0.05 | 0.15 |
| L2 | 0.30 | 0.50 |
| L3 | 0.15 | 0.25 |

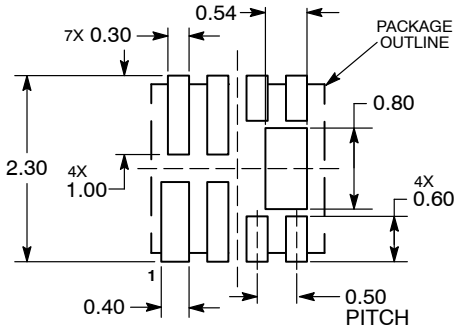
### GENERIC MARKING DIAGRAM*




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON52381E** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **WDFN8, 2.2X2.0, 0.5P** | **PAGE 1 OF 1** |

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