2.5 A PWM Step-up DC/DC Converter

NO.EA-278-180731

OUTLINE

The R1213K is a low supply current PWM step-up DC/DC converter capable of providing an output current up to 2.5 A. Internally, the device consists of an Nch MOSFET driver, an oscillator, a PWM comparator, a voltage reference unit, an error amplifier, a soft-start circuit, an under voltage lockout circuit (UVLO), a thermal shutdown protection circuit, an overcurrent protection circuit and an latch-type protection circuit.

The R1213K requires minimal external component count. By simply using an inductor, resistors, capacitors and a diode, a high-efficiency step-up DC/DC converter can be easily configured.

The R1213K can adjust the output voltage, the soft-start time, the phase compensation using the external resistors and capacitors.

The R1213K has a shutdown control function which can be activated by a protection circuit to turn off the external Pch MOSFET for breaking the current path between the input and output.

The R1213K provides an overcurrent protection circuit, a latch-type protection circuit, a thermal shutdown protection circuit and an UVLO circuit. The overcurrent protection circuit limits the L_X peak current and a latch-type protection circuit latches the Nch MOSFET off to stop the operation of the DC/DC converter if the output voltage drop due to overcurrent continues more than the protection delay time.

The R1213K is offered in a 12-pin DFN(PLP)2730-12 package.

FEATURES

- Input Voltage Range (Maximum Rating) ····· 2.3 V to 5.5 V (6.5 V)
- Supply Current ····· Typ. 550 µA (non-switching)
- Supply Current ····· Typ. 3 mA (switching)
- Standby Current ····· Max. 1.5 µA (CE = “L”)
- Output Voltage Range ····· 3.0 V to 15.0 V, Externally Adjustable (V_{FB} = 0.8 V)
- Feedback Voltage Accuracy ····· ±8 mV
- Feedback Voltage Temperature Coefficient ····· ±50 ppm/°C
- Output Current ····· 1.0 A: V_{IN} = 3.3 V, V_{OUT} = 3.8 V
  500 mA: V_{IN} = 2.3 V, V_{OUT} = 5.0 V
  250 mA: V_{IN} = 2.7 V, V_{OUT} = 9.6 V
  150 mA: V_{IN} = 3.0 V, V_{OUT} = 15 V
- Nch ON Resistance ····· Typ. 0.07 Ω
- Shutdown Control Function ····· Activated by the external Pch MOSFET
- Thermal Shutdown Circuit ····· Activated at 150°C (Hys.= 40°C)
- Overcurrent Protection Circuit ····· Activated at Typ. 3.0 A

- Latch-type Protection Circuit ····· Protection Delay Time: Typ. 32 ms
- FLAG Output Function ····· Activated at ”H”
- UVLO Detector Threshold ····· Typ. 2.0 V
- Oscillator Frequency ····· Typ. 1.0 MHz
- Maximum Duty Cycle ····· Min. 85%, Typ. 90%
- Soft-start Time ····· Set by the SS Pin
- Phase Compensation ····· Set by the AMPOUT Pin
- Package ····· DFN(PLP)2730-12

APPLICATION

- Flash LEDs
- Data Cards
- DSCs
- LCD Source Bias Supplies

SELECTION GUIDE

The R1213K offers users to select the output voltage type matched to their set output voltage. Selecting the matched output voltage type can ensure high-speed transient response and stability.

Selection Guide

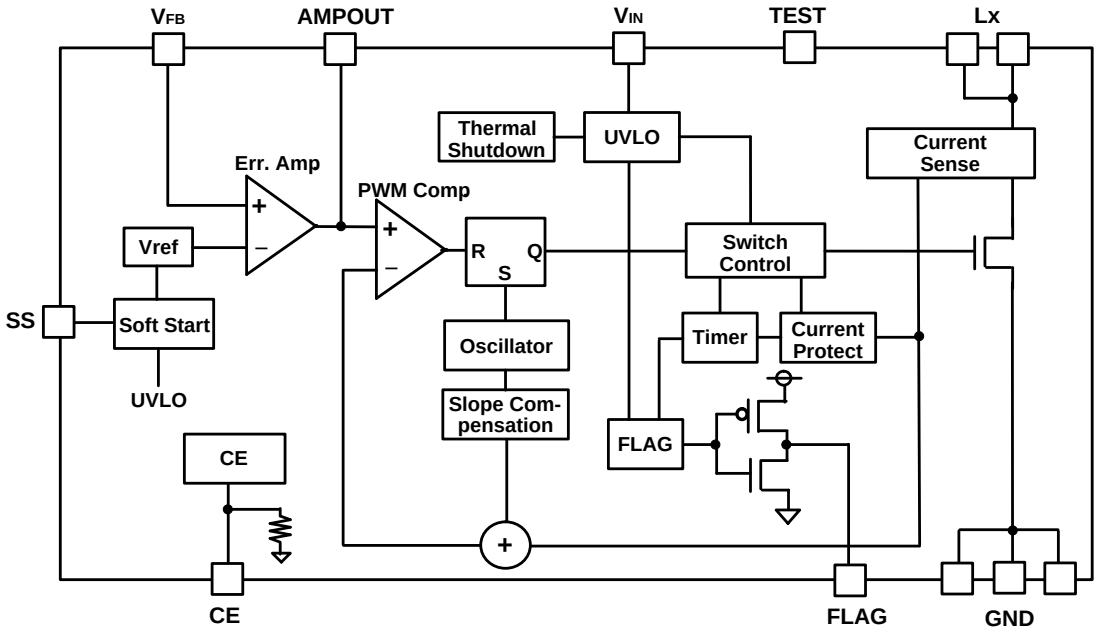
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1213K001∗-TR	DFN(PLP)2730-12	5,000 pcs	Yes	Yes

∗: Specify the output voltage type.

A: Low Output Voltage Type (V_{OUT}: 3.0 V to 6.0 V)

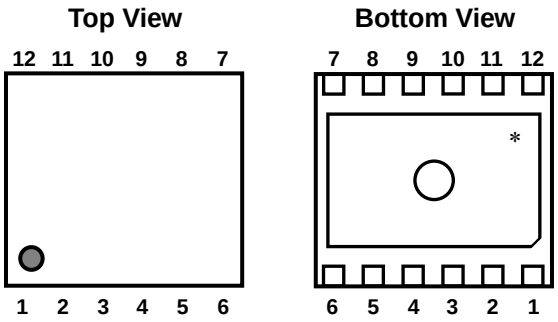
B: High Output Voltage Type (V_{OUT}: 6.0 V to 15 V)

BLOCK DIAGRAMS



R1213K Block Diagram

PIN DESCRIPTION



DFN(PLP)2730-12 Pin Configuration

DFN(PLP)2730-12 Pin Description

Pin No	Symbol	Pin Description
1	AMPOUT	Amplifier Output Pin
2	V_{FB}	Feedback Voltage Pin
3	CE	Chip Enable Pin, Active-high
4	GND	Ground Pin(1)
5	GND	Ground Pin(1)
6	GND	Ground Pin(1)
7	TEST	TEST Pin(2)
8	L_X	Switching Pin(1)
9	L_X	Switching Pin(1)
10	V_{IN}	Input Voltage Pin
11	FLAG	Shutdown Control Pin(3)
12	SS	Soft-start Pin

∗ The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

(1) The No.4, No.5 and No.6 pins must be connected together. The No.8 and No.9 pins must be connected together.
(2) The TEST pin must be connected to GND or left floating.
(3) The FLAG pin should be left floating when it is not used.

ABSOLUTE MAXIMAM RATINGS

Absolute Maximum Ratings (GND = 0 V)

Symbol	Item	Rating	Unit
V_{IN}	V_{IN} Pin Voltage	−0.3 to 6.5	V
V_{AMPOUT}	AMPOUT Pin Voltage	−0.3 to V_{IN} + 0.3	V
V_{CE}	CE Pin Voltage	−0.3 to 6.5	V
V_{FB}	V_{FB} Pin Voltage	−0.3 to 6.5	V
V_{SS}	SS Pin Voltage	−0.3 to V_{IN} + 0.3	V
V_{FLG}	FLAG Pin Voltage	−0.3 to V_{IN} + 0.3	V
V_{TST}	TEST Pin Voltage	−0.3 to V_{IN} + 0.3	V
V_{LX}	L_X Pin Voltage	−0.3 to 18.0	V
P_D	Power Dissipation(1) (DFN(PLP)2730-12, JEDEC STD. 51-7 Test Land Pattern)	3100	mW
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

■ RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.3 to 5.5	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
Istandby	Standby Current	V_{IN} = 5.5 V, V_{CE} = 0 V		0.1	1.5	µA
I_{DD1}	Supply Current 1 (non-switching)	V_{IN} = 5.5 V, V_{FB} = 0.9 V		550	800	µA
I_{DD2}	Supply Current 2	V_{IN} = 5.5 V, V_{FB} = 0 V		3.0	4.5	mA
V_{UVLO1}	UVLO Detector Threshold	V_{FB} = 0 V	1.9	2.0	2.1	V
V_{UVLO2}	UVLO Released Voltage	V_{FB} = 0 V		V_{UVLO1} +0.12	2.25	V
V_{OUT}	Output Voltage Range	R1213K001A	3.0		6.0	V
		R1213K001B	6.0		15	
V_{FB}	Feedback Voltage Accuracy	V_{IN} = 3.6 V	0.792	0.8	0.808	V
ΔV_{FB} /ΔTa	Feedback Voltage Temperature Coefficient	−40°C ≤ Ta ≤ 85°C		±50		ppm /°C
I_{LXLEAK}	L_X Leakage Current	V_{LX} = 16 V, V_{CE} = 0 V		0.01	2.0	µA
I_{FBH}	V_{FB} "H" Input Current	V_{IN} = 5.5 V, V_{FB} = 5.5 V			0.15	µA
I_{FBL}	V_{FB} "L" Input Current	V_{IN} = 5.5 V, V_{FB} = 0 V	−0.15			µA
I_{CEL}	V_{CEL} Input Current	V_{IN} = 5.5 V, V_{CE} = 0 V	−0.2		0.2	µA
R_{CE}	CE Pull-down Resistance			1000		kΩ
I_{SS}	Soft-start Current	V_{IN} = 3.6 V		10		µA
V_{CEH}	CE Input Voltage "H"	V_{IN} = 5.5 V	1.5			V
V_{CEL}	CE Input Voltage "L"	V_{IN} = 2.3 V			0.3	V
fosc	Oscillator Frequency	V_{IN} = 3.6 V, V_{FB} = 0 V	0.85	1.00	1.15	MHz
Maxduty	Maximum Duty Cycle	V_{IN} = 3.6 V, V_{FB} = 0 V	85	90	95	%
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature		150		°C
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature		110		°C
gm	Trans-conductance(1)	V_{IN} = 3.6 V		220		µS
I_{LXLIM}	L_X Current Limit	V_{IN} = 3.6 V	2.5	3.0	3.8	A
R_{ON}	Nch ON Resistance(1)	V_{IN} = 3.6 V		0.07		Ω
tprot	Latch-type Protection Delay Time	V_{IN} = 3.6 V		32		ms
I_{RUSH}	Inrush Current(2)				1.5	A

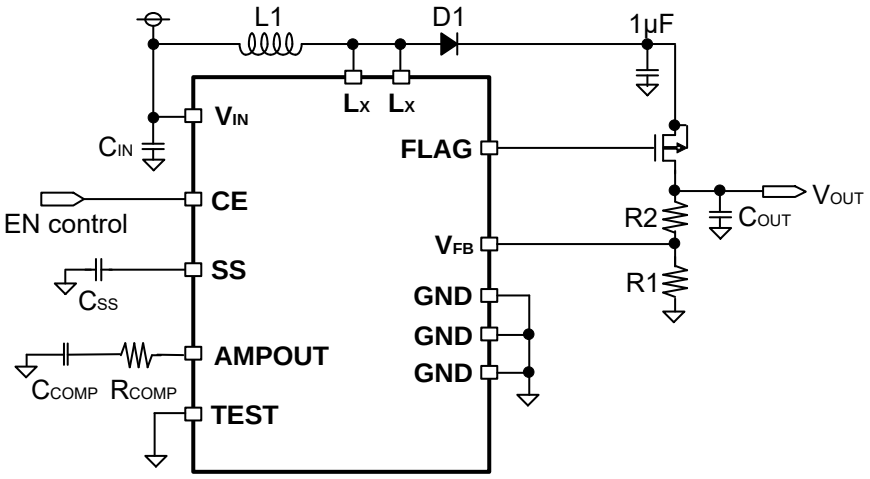
(1) Guaranteed by design engineering, not mass production tested.

(2) Guaranteed by design engineering when the external Pch MOSFET is connected to the FLAG pin. Refer to the recommended components at *APPLICATION INFORMATION* and *TECHNICAL NOTES*.

■ APPLICATION INFORMATION

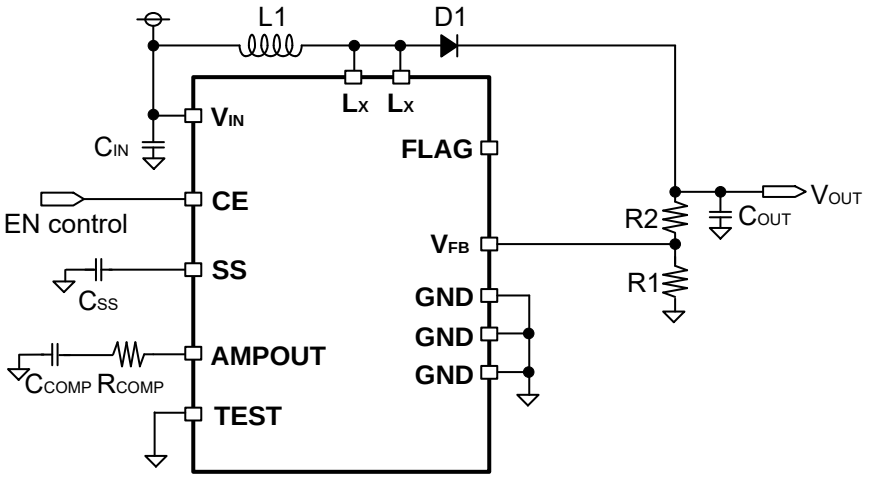
Typical Application

External Pch MOSFET is Connected for Breaking the Current Path between V_{IN} – V_{OUT} (V_{OUT} < 13 V)



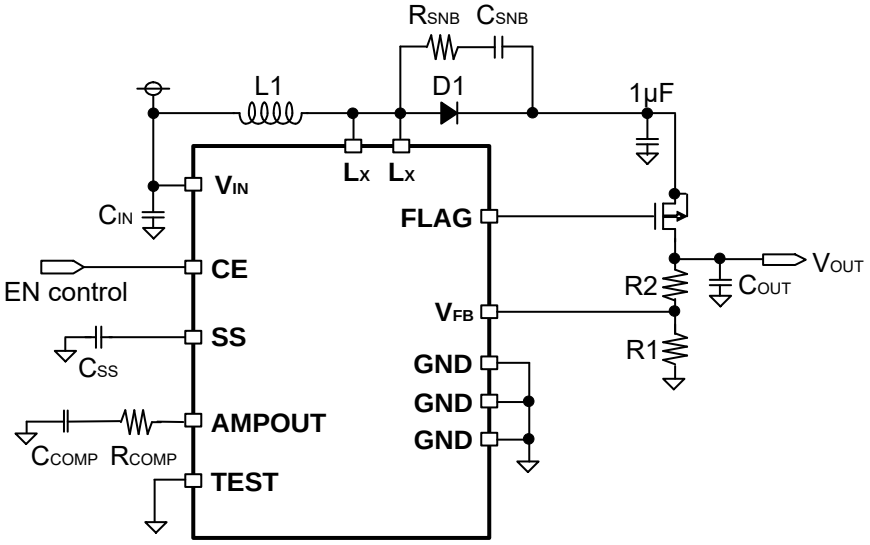
Notes: The GND pins and also the L_X pins must be mutually short-circuited right near the ground plane on the board. The TEST pin must be connected to the ground plane on the board or be left floating.

External Pch MOSFET is <u>NOT</u> Connected for Breaking the Current Path between V_{IN} – V_{OUT} (V_{OUT} < 13 V)



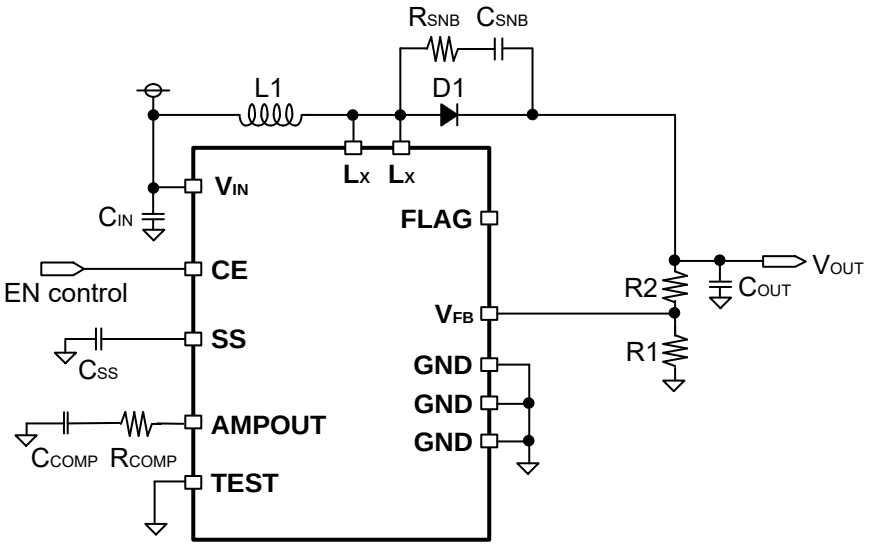
Notes: The GND pins and also the L_X pins must be mutually short-circuited right near the ground plane on the board. The TEST pin must be connected to the ground plane on the board or be left floating. The FLAG pin must be left floating.

External Pch MOSFET is Connected for Breaking the Current Path between V_{IN} – V_{OUT} (V_{OUT} ≥ 13 V)



Notes: The GND pins and also the L_X pins must be mutually short-circuited right near the ground plane on the board. The TEST pin must be connected to the ground plane on the board or be left floating.
The snubber circuit must be added for preventing spike noise on the L_X pin.

External Pch MOSFET is <u>NOT</u> Connected for Breaking the Current Path between V_{IN} – V_{OUT} (V_{OUT} ≥ 13 V)



Notes: The GND pins and also the L_X pins must be mutually short-circuited right near the ground plane on the board. The TEST pin must be connected to the ground plane on the board or be left floating. The FLAG pin must be left floating. The snubber circuit must be added for preventing spike noise on the L_X pin.

Recommended Components

	V_{IN}	Cap.	Spec.	Part Name	Manufacturer
C_{IN}	All	10 µF	6.3 V	C2012JB0J106M	TDK

	V_{OUT}	Cap.	Spec.	Part Name	Manufacturer
C_{OUT}	≤ 5 V	10 µF	6.3 V	C2012JB0J106M	TDK
	≤ 10 V	10 µF	16 V	C2012X5R1C106K	TDK
	all	10 µF	25 V	C3216X5R1E106K	TDK
	all	10 µF	25 V	TMK325BJ106MN	Taiyo Yuden

	V_{OUT}	Spec.	Part Name	Manufacturer
D1	all	40 V, 3 A	CMS16	TOSHIBA
	all	40 V, 3 A	RB056L-40	ROHM

	V_{OUT}	Ind.	Spec.	Part Name	Manufacturer
L1[(1)]	3.0V ≤ V_{OUT} ≤ 4.5V	2.2 µH	2.2 A	SPM3012T-2R2N	TDK
			2.7 A	SPM4012T-2R2N	TDK
			3.5 A	NR5040T2R2N	Taiyo Yuden
	4.5V < V_{OUT} ≤ 12V	4.7 µH	1.7 A	SPM4012T-4R7N	TDK
			3.1 A	NR5040T4R7N	Taiyo Yuden
	12V < V_{OUT} ≤ 15V	6.8 µH	1.4 A	VLF5014ST-6R8N	TDK
			2.8 A	RLF7030T-6R8N	TDK
			3.7 A	NR8040T6R8N	Taiyo Yuden

	V_{OUT}	Spec. (I_{DS}, V_{DS}, V_{GS})	Part Name	Manufacturer
Pch.MOSFET	all	4.5 A, −30 V, ±20 V	UPA1914	Renesas

(1) It is recommended that the rated current of the inductor be higher than the LX limit current. Performing the current limitation outside of the R1213K requires the use of small components.

• Selection of Resistors and Capacitors for Phase Compensation

The R1213x requires an external phase compensation on the feedback loop for output voltage control to prevent the large output ripple, the unstable operation and the deterioration of device efficiency. Connect a resistor (RCOMP) and a capacitor (CCOMP) between the AMPOUT and GND pins.
RCOMP and CCOMP can be calculated as follows:

[R1213K001A]

$R_{COMP} = 90 \times V_{IN} \times V_{OUT} \times C_{OUT} / (L \times I_{OUTMAX})$

$C_{COMP} = 30 \times V_{OUT} \times L \times I_{OUTMAX} / (VIN^2 \times R_{COMP})$

[R1213K001B]

$R_{COMP} = 45 \times V_{IN} \times V_{OUT} \times C_{OUT} / (L \times I_{OUTMAX})$

$C_{COMP} = 30 \times V_{OUT} \times L \times I_{OUTMAX} / (V_{IN}^2 \times R_{COMP})$

The appropriate values for R_{COMP} and C_{COMP} vary depending on the peripheral components and circuit board. Determine the appropriate values for R_{COMP} and C_{COMP} according to the transient response.

V_{IN} (V)	V_{OUT} (V)	I_{OUTMAX} (mA)	C_{IN} (µF)	C_{OUT} (µF)	L1 (µH)	D1	R_{COMP} (kΩ)	C_{COMP} (nF)
3.3	3.8	1200	10	20	2.2	3 A	8.2	3.3
3.3	5	800	10	20	4.7	3 A	8.2	6.8
3.3	12	250	10	20	4.7	3 A	27	1.8
5.0	15	650	10	20	6.8	3 A	15	5.1

• Output Voltage Setting

The output voltage can be calculated by the values of resistors (R1 and R2) as follows:

Output Voltage = $V_{FB} \times (R1 + R2) / R1$

(V_{FB} = 0.8 V)

Notes: Set the sum of R1 and R2 to be 200 kΩ or less.

• Soft-start Time Setting

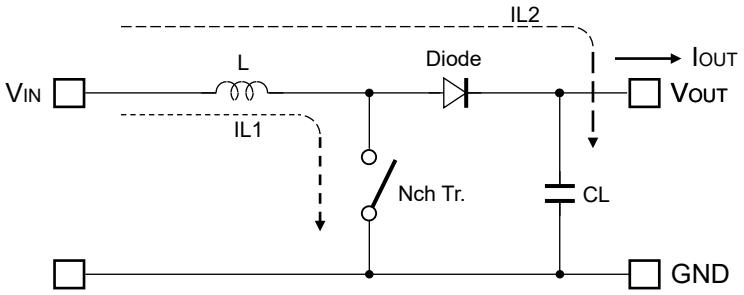
The soft-start time can be adjusted by a capacitor (C_{SS}) between the SS and GND pins.
The soft-start time can be calculated as follows:

Soft-start time = $C_{SS} \times V_{FB} / I_{SS}$

= $8 \times C_{SS} \times 10^4$ [sec]

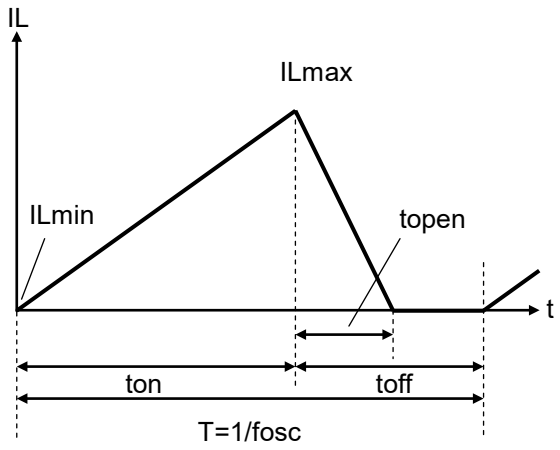
(V_{FB} = 0.8 V, I_{SS} = 10 µA)

- **Operation of Step-Up Dc/Dc Converter and Output Current**

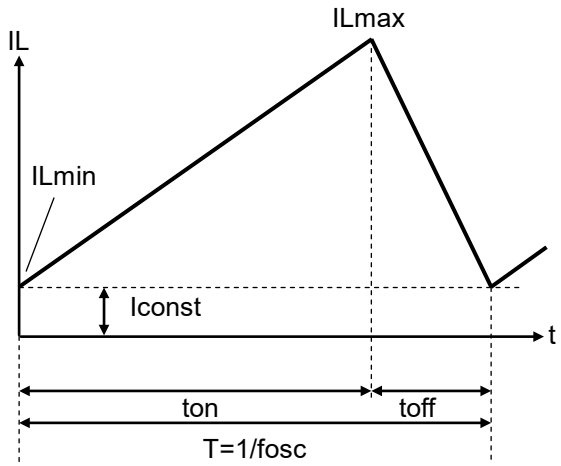


Basic Circuit

Current (IL) Flowing Through Inductor (L)



Discontinuous Inductor Current Mode



Continuous Inductor Current Mode

The PWM control type of the step-up DC/DC converter has two operation modes characterized by the continuity of inductor current: discontinuous inductor current mode and continuous inductor current mode.

When an Nch transistor is in On-state, the voltage to be applied to the inductor (L) is described as V_{IN}. An increase in the inductor current (IL1) can be written as follows:

$IL1 = V_{IN} \times ton / L$ ..... Formula 1

In the step-up DC/DC converter circuit, the energy accumulated during the On-state is transferred into the capacitor even in the Off-state. A decrease in the inductor current (IL2) can be written as follows:

$IL2 = (V_{OUT} - V_{IN}) \times topen / L$ ..... Formula 2

In the PWM control, IL1 and IL2 become continuous when topen = toff, which is called continuous inductor current mode.

When the device is in continuous inductor current mode and operates in steady-state conditions, the variations of IL1 and IL2 are same:

V_{IN} x ton / L = (V_{OUT} - V_{IN}) x toff / L ..... Formula 3

Therefore, the duty cycle in continuous inductor current mode is:

duty (%)= ton / (ton + toff) = (V_{OUT} − V_{IN}) / V_{OUT} ..... Formula 4

When topen = toff, the average of IL1 is:

IL1 (Ave.) = V_{IN} x ton / (2 x L) ..... Formula 5

If the input voltage (V_{IN}) is equal to the output voltage (V_{OUT}), the output current (I_{OUT}) is:

I_{OUT} = V_{IN}^2 x ton / (2 x L x V_{OUT}) ..... Formula 6

If I_{OUT} is larger than Formula 6, the device switches to continuous inductor current mode

The L_X peak current flowing through L (ILmax) is:

ILmax = I_{OUT} x V_{OUT} / V_{IN} + V_{IN} x ton / (2 x L) ..... Formula 7

ILmax = I_{OUT} x V_{OUT} / V_{IN} + V_{IN} x T x (V_{OUT} − V_{IN}) / (2 x L x V_{OUT}) ..... Formula 8

As a result, ILmax becomes larger compared to I_{OUT}. The overcurrent protection circuit operates if the ILmax becomes more than the L_X current limit. When considering the input and output conditions or selecting the external components, please pay attention to ILmax.

Notes: The above calculations are based on the ideal operation of the device. They do not include the losses caused by the external components or Nch transistor. The actual maximum output current will be 50% to 80% of the above calculation results. Especially, if IL is large or V_{IN} is low, it may cause the switching losses.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Ensure that the V_{IN} and GND lines are firmly connected. A large switching current flows through the V_{IN} and GND lines. If their impedance is too high, noise pickup or unstable operation may result.

- When an Nch MOSFET driver is turned off, the inductor may generate a spike-shaped high voltage. Use a high-break-down-voltage capacitor (C_{OUT}) and a high-break-down-voltage diode that are 1.5 times or more than the set output voltage.

- Choose a schottky diode (D1) that has low forward voltage, low reverse current, and is fast in switching speed.

- Use an inductor that has a low DC resistance, has an enough tolerable current and is less likely to cause magnetic saturation.

- The FLAG pin (Shutdown Control Pin) turns off the external Pch MOSFET to break the current path between V_{IN} and V_{OUT} during standby, UVLO, thermal shutdown and latch-type protection. Place a capacitor of 1 µF between the source of the external Pch MOSFET and GND to protect the external Pch MOSFET from overvoltage caused by the inductor current.
  During the soft-start, the FLAG pin turns on or off the external Pch MOSFET synchronizing with the switching of the Nch MOSFET to prevent the inrush current. Select the external Pch MOSFET with fast switching speed (Approx. 100 ns) and small gate capacity (3 nF or less).

- The spike noise of L_X should not exceed the absolute maximum rating. The spike noise of L_X may exceed the absolute maximum ratings under $V_{OUT} \geq 13$ V. To reduce the spike noise of L_X, place a snubber circuit (R_{SNB} and C_{SNB} are connected in series) parallel to the diode (D1). A snubber circuit may also be required under $V_{OUT} < 13$ V if the spike noise of L_X is large. It is recommended that a capacitor (C_{SNB}) be 1100 pF and a resistor (R_{SNB}) be 0.68 Ω. The appropriate values for C_{SNB} and R_{SNB} vary significantly depending on the circuit board and affect the device efficiency. Actual circuit board testing is required.

- Latch-type protection circuit latches the Nch MOSFET off to stop the operation of the DC/DC converter if the output voltage drop due to overcurrent continues more than the protection delay time. When the latch-type protection circuit operates, the FLAG pin outputs “H” and turns the external Pch MOSFET off to break the current path between V_{IN} and V_{OUT}.
  The protection delay time is set to typically 32 ms. If the output voltage returns to normal during the protection delay time, the internal timer will be reset.
  To release the latch-type protection, set the CE pin “H” or make the power supply voltage lower than the UVLO detector threshold.

- Connect the TEST pin to GND or otherwise leave it floating.

- Connect the FLAG pin to the external Pch MOSFET gate only.

- To prevent inrush current, connect the SS pin to a capacitor (C_{SS}) only.

- The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating. To enhance the thermal performance of multilayer circuit board, provide a thermal via under the tab on the bottom of the package.

- In Fig. A and Fig. B, the current paths on the boost DC/DC converter are shown. The current paths when the MOSFET turns on are shown in Fig. A, and the current paths when the MOSFET turns off are shown in Fig. B. The pointed parts with red arrows in Fig. B are where the current flows only when the MOSFET turns on, or off. The parasitic impedance, inductance, or parasitic capacitance of these parts have some impact on the stability of DC/DC converter, and may cause a noise generation. Therefore the parasitic impedance, capacitance, inductance must be as small as possible. Furthermore, the current paths shown in Fig. A and Fig. B must be as short as possible and as wide as possible.

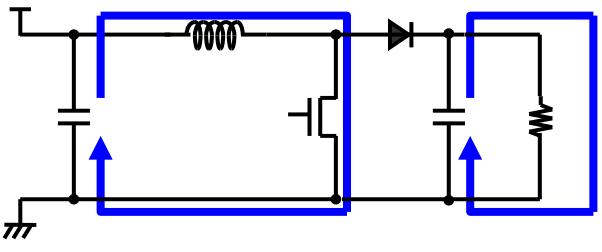


Figure A. MOSFET-ON (Boost)

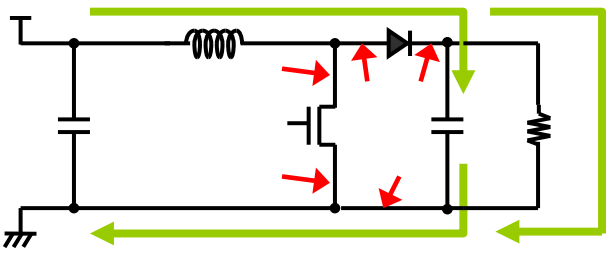
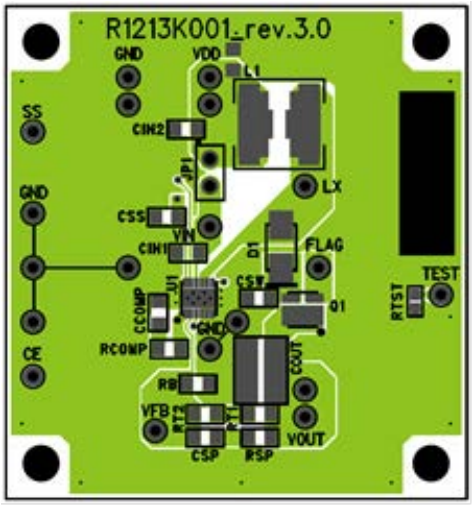


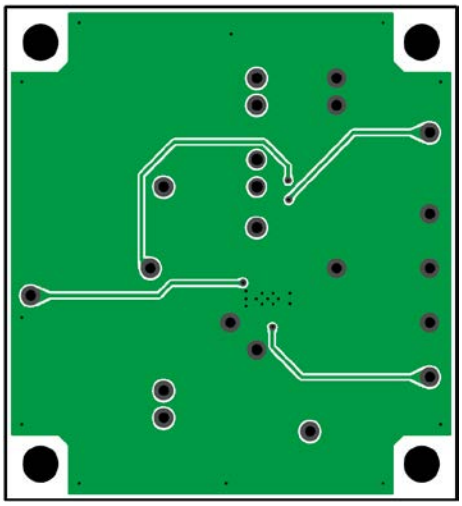
Figure B. MOSFET-OFF (Boost)

- **PCB Layout**

R1213K001A/B (PKG: DFN(PLP)2730-12pin)



Typical Board Layout – Top Layer



Typical Board Layout – Back Layer

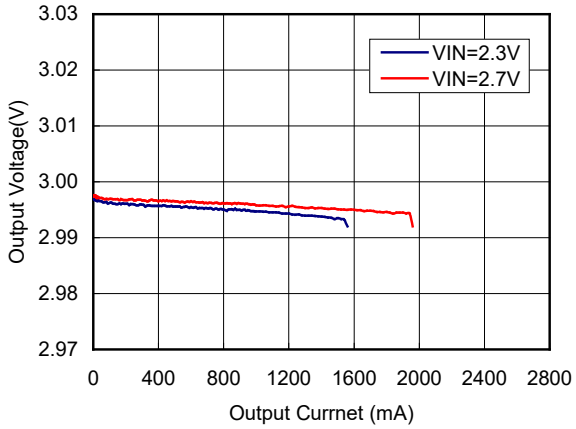
Note: R2 patterns are the layout for 2 serial resistance chips, RT1 and RT2 to set preferred value easier.

TYPICAL CHARACTERISTICS

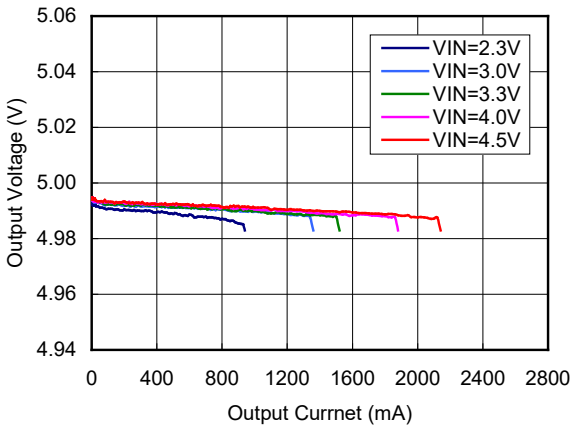
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current (Ta = 25°C)

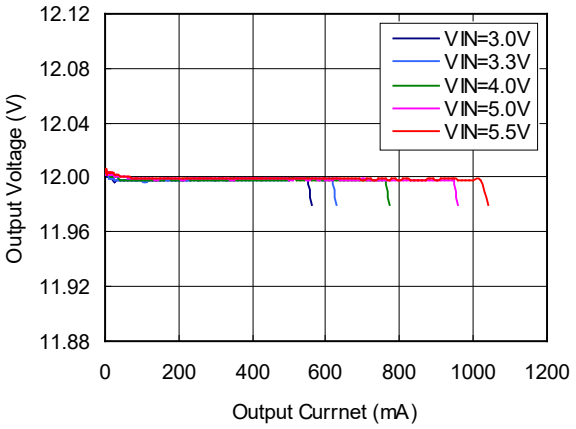
V_{OUT} = 3.0 V



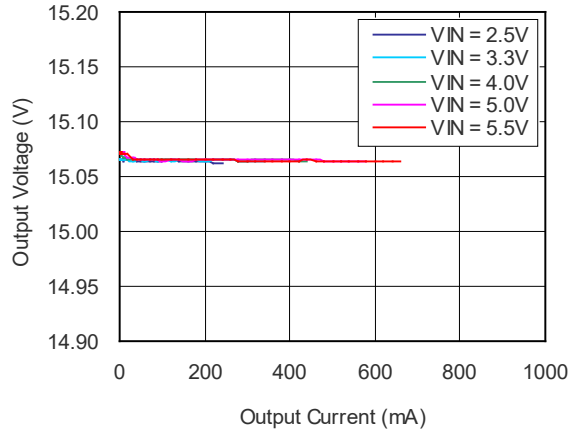
V_{OUT} = 5.0 V



V_{OUT} = 12 V

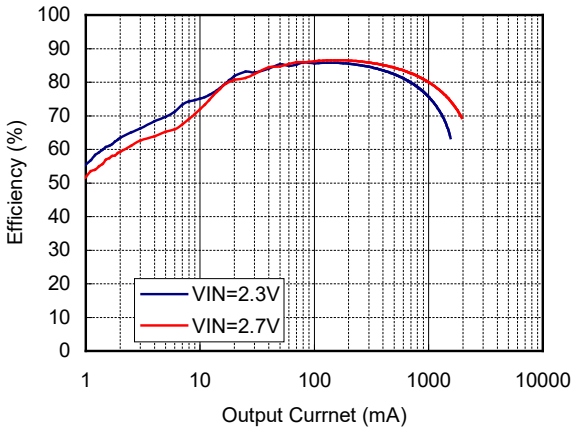


V_{OUT} = 15 V

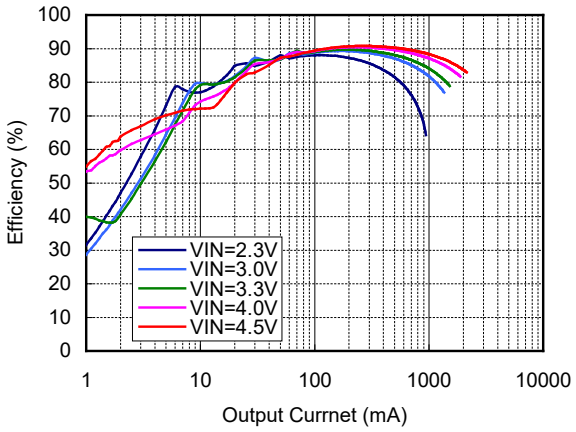


2) Efficiency vs. Output Current (Ta = 25°C)

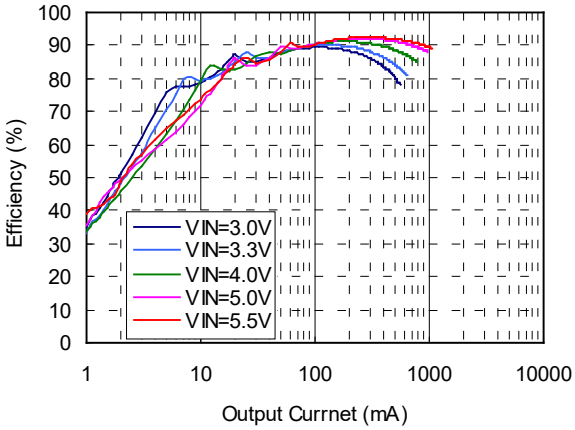
V_{OUT} = 3.0 V



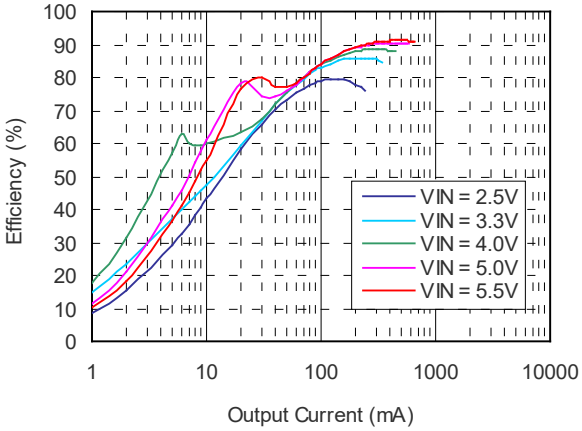
V_{OUT} = 5.0 V



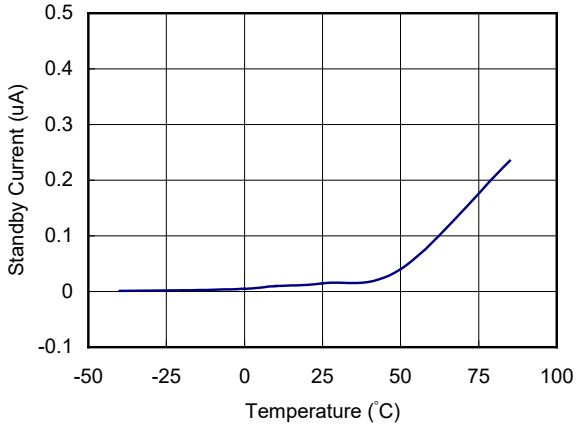
V_{OUT} = 12 V



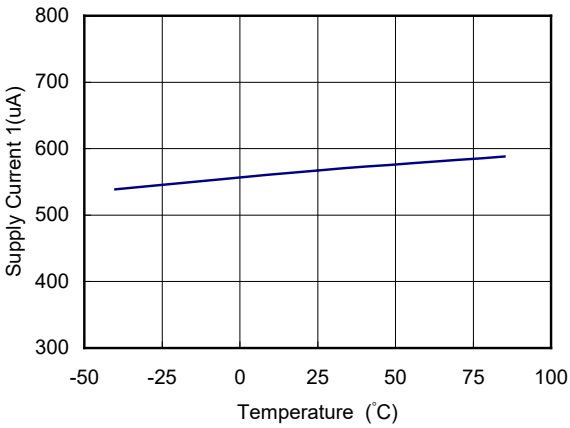
V_{OUT} = 15 V



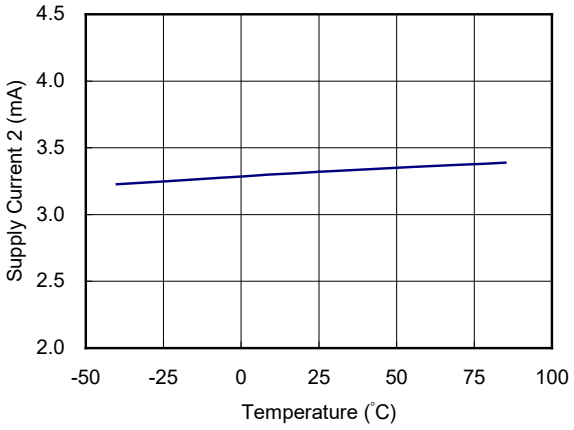
3) Standby Current vs. Temperature



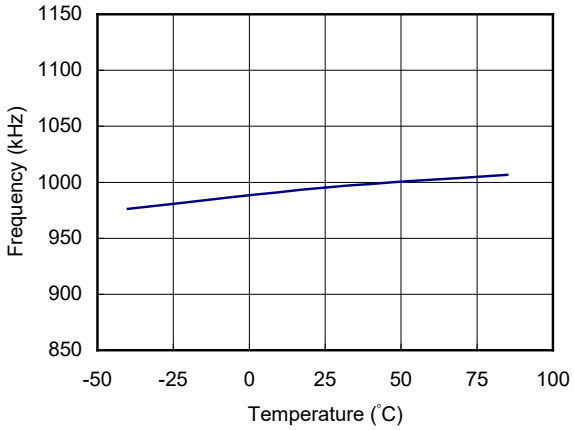
4) Supply Current 1 vs. Temperature



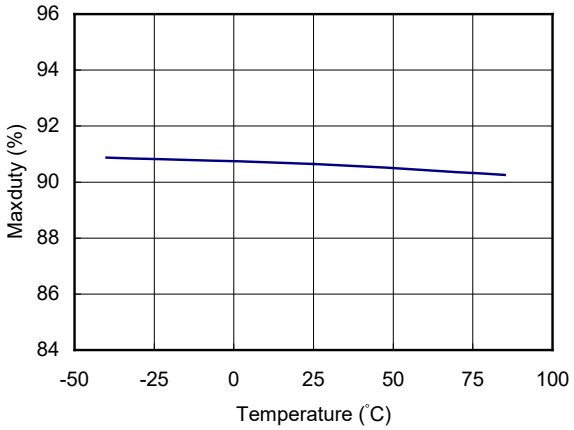
5) Supply Current 2 vs. Temperature



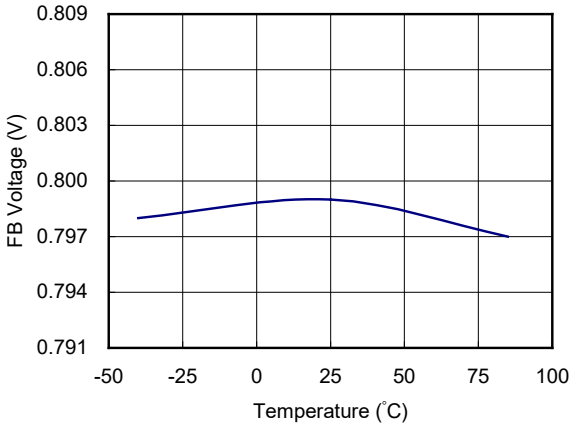
6) Frequency vs. Temperature



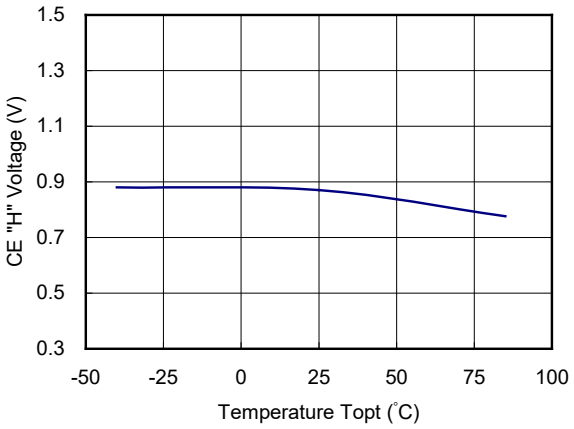
7) Maxduty vs. Temperature



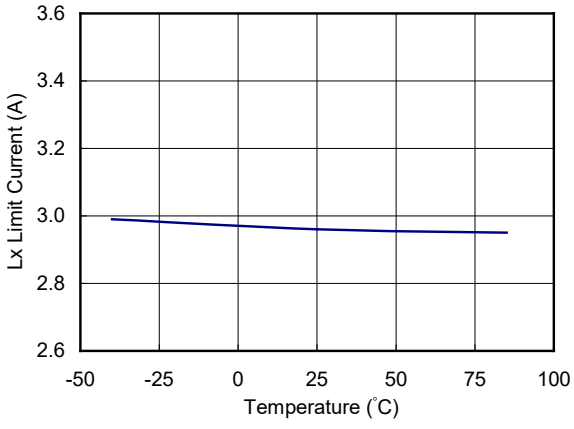
8) FB Voltage vs. Temperature



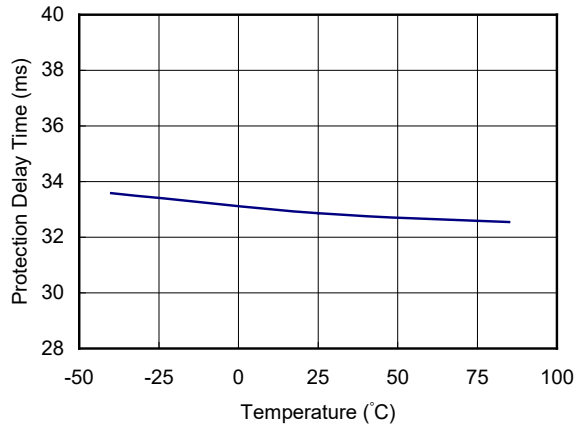
9) CE “H” Input Voltage vs. Temperature



10) Lx Limit Current vs. Temperature

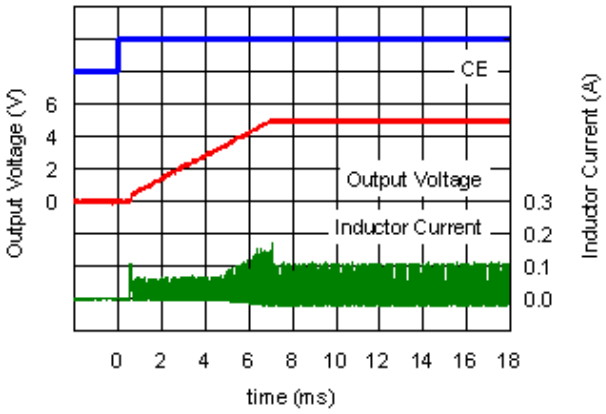


11) Protection Delay Time vs. Temperature

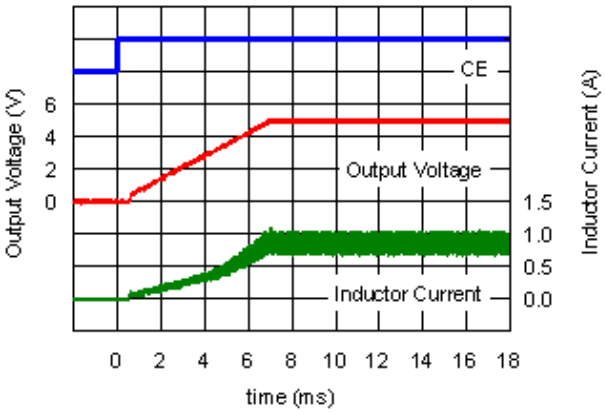


12) Start-up Waveform (Ta = 25°C, C_{SS} = 0.1 µF, External Pch MOSFET Connected between V_{IN} – V_{OUT})

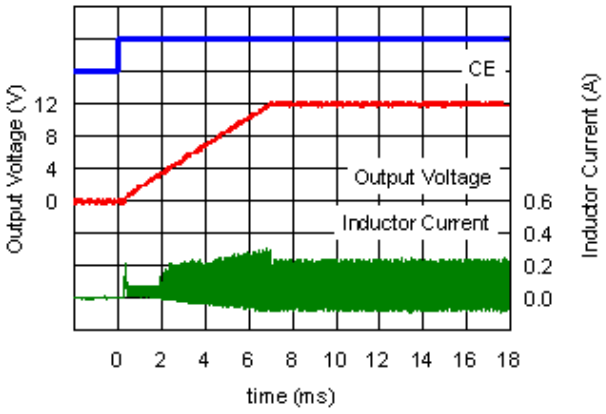
・V_{IN} = 3.3 V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA



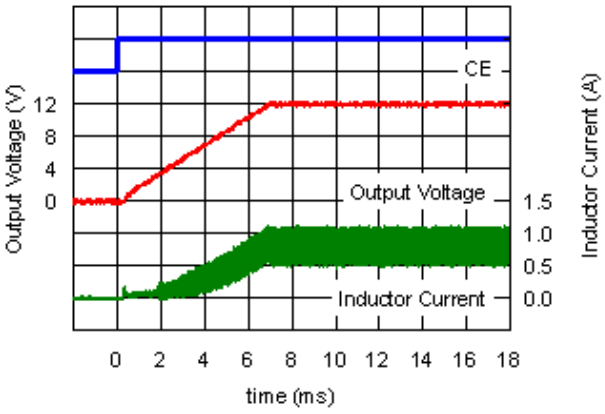
・V_{IN} = 3.3 V, V_{OUT} = 5.0 V, I_{OUT} = 500 mA



・V_{IN} = 3.3 V, V_{OUT} = 12 V, I_{OUT} = 10 mA

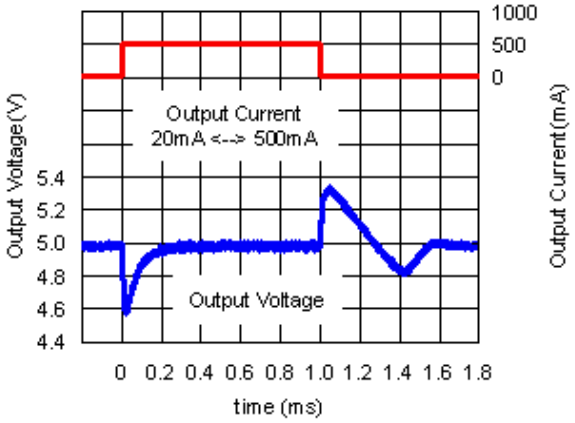


・V_{IN} = 3.3 V, V_{OUT} = 12 V, I_{OUT} = 200 mA

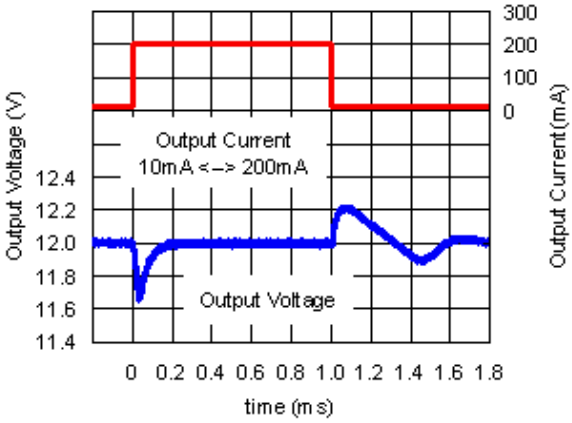


13) Load Transient Response Waveform (Ta = 25°C)

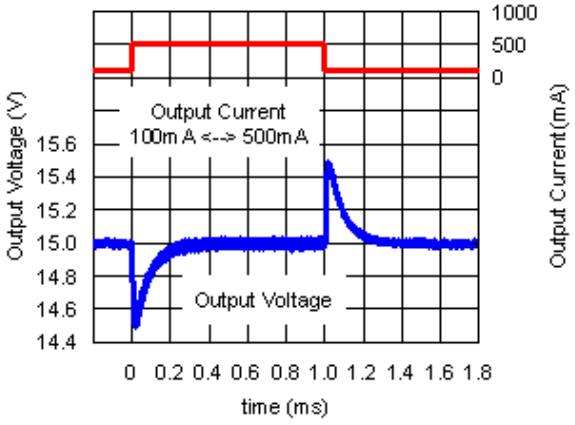
・V_{IN} = 3.3 V, V_{OUT} = 5.0 V, I_{OUT} = 20 ⇔ 500 mA
L = 4.7 µH, C_{OUT} = 20 µF, R_{COMP} = 8.2 kΩ,
C_{COMP} = 6.8 nF



・V_{IN} = 3.0 V, V_{OUT} = 12 V, I_{OUT} = 10 ⇔ 200 mA
L = 4.7 µH, C_{OUT} = 20 µF, R_{COMP} = 27 kΩ,
C_{COMP} = 1.8 nF

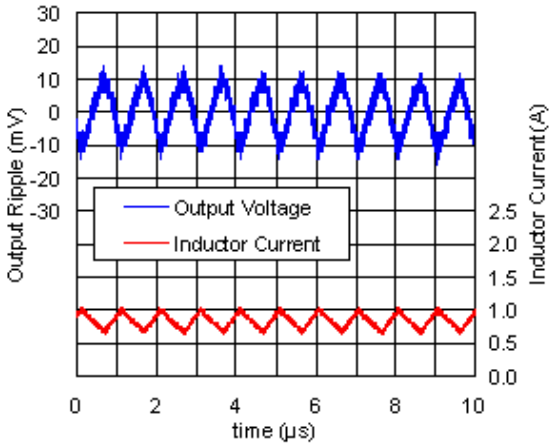


・V_{IN} = 5.0 V, V_{OUT} = 15.0 V, I_{OUT} = 100 ⇔ 500 mA
L = 6.8 µH, C_{OUT} = 20 µF, R_{COMP} = 15 kΩ,
C_{COMP} = 5.1 nF

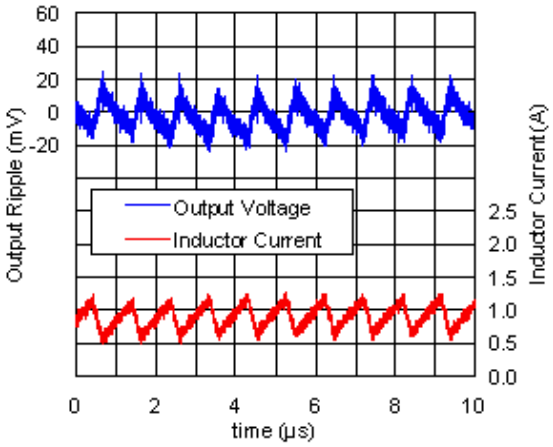


14) Output Voltage Waveform (Ta = 25°C)

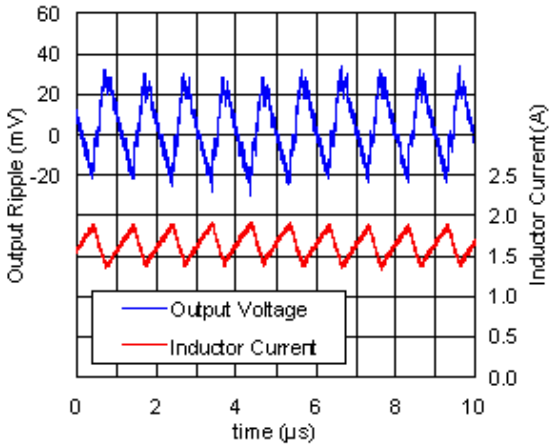
・V_{IN} = 3.3 V, V_{OUT} = 5.0 V, I_{OUT} = 500 mA
L = 4.7 µH, C_{OUT} = 20 µF



・V_{IN} = 3.3 V, V_{OUT} = 12 V, I_{OUT} = 200 mA
L = 4.7 µH, C_{OUT} = 20 µF



・V_{IN} = 5.0 V, V_{OUT} = 15 V, I_{OUT} = 500 mA
L = 6.8 µH, C_{OUT} = 20 µF



Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

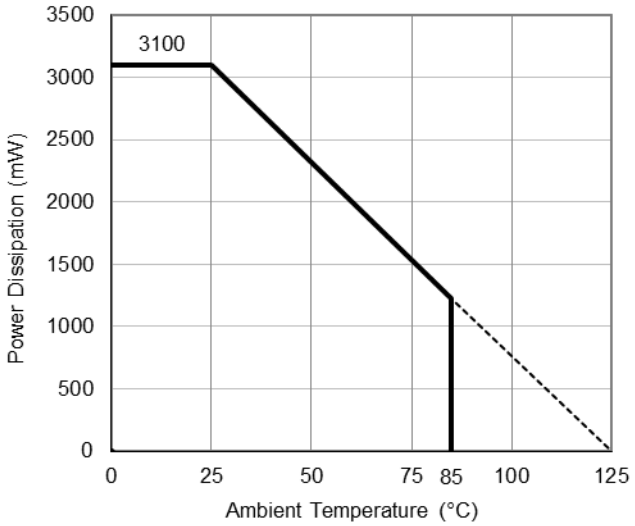
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 23 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

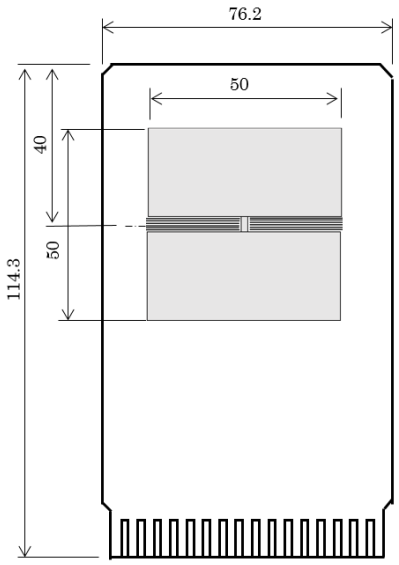
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

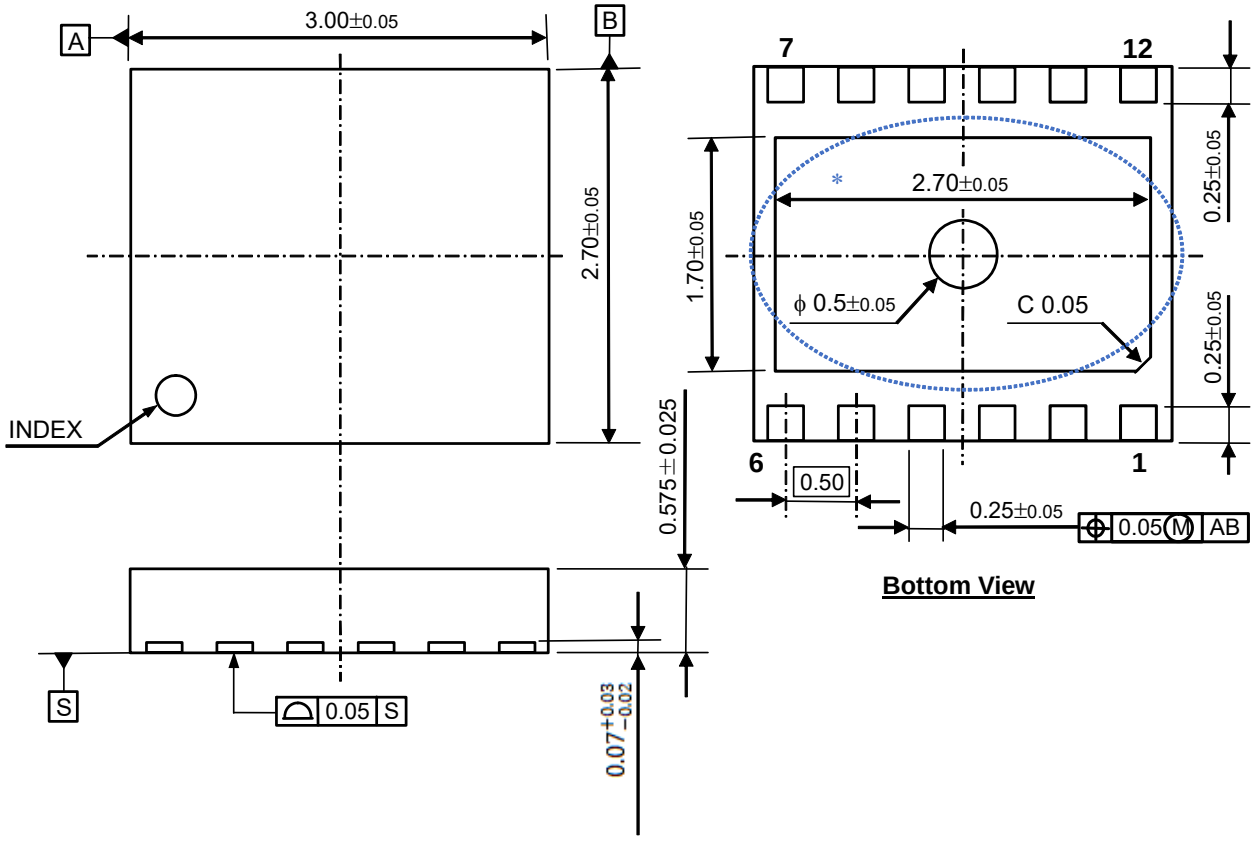
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



DFN(PLP)2730-12 Package Dimensions (Unit: mm)

*The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

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10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.
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