DAC8831/32 Evaluation Module

This user's guide describes the DAC8831/32 Evaluation Module. It covers the operating procedures and characteristics of the EVM board along with the device that it supports. The physical printed circuit board (PCB) layout, schematic diagram, and circuit descriptions are included.

Contents

List of Figures

List of Tables

1 EVM Overview

This section provides an overview of the DAC8831/32 evaluation module (EVM), and instructions on setting up and using this evaluation module. Throughout this document, the abbreviation *EVM* and the phrase *evaluation module* are synonymous with the DAC8831/32EVM. Unless otherwise specified, operation of the DAC8831EVM is identical to the operation of the DAC8832EVM; therefore, the abbreviation *DAC8831/32EVM* is used throughout this document

1.1 Features

This EVM features the DAC8831/32 16-bit resolution, unbuffered voltage output digital-to-analog converter (DAC). This EVM supports the 14-pin QFN package (RGY) only for the DAC8831 and the DAC8832. The design is based on the modular EVM format for Data Acquisitions Product group of Texas Instruments to provide quick and easy way to evaluate the functionality and performance of the high-resolution serial input DAC. This EVM includes an onboard reference and buffer circuits and allows high-speed serial interface with a variety of TI DSP and microcontroller interface boards.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply for the digital section (V_{DD}) of this EVM is dedicated to +5V via the J3-10 terminal and is referenced to ground through the J3-5 terminal.

The dc power supply requirements for the analog section of this EVM are as follows: the +5VA connects through J3-3 and the –5VA connects through J3-4. All the analog power supplies are referenced to analog ground through J3-6 terminal.

The device under test (U3) power supply only requires +5V to operate; therefore, the supply is derived from V_{DD} (via J3-10). The +5VA supply sources the positive rail of the external output op-amp, U1, while –V, which is configurable between –5VA and AGND via R2 and R7 shorting resistors, supplies the negative rail of the output op-amp. The supply for the voltage reference circuit U5, as well as the reference buffer U4, uses +5VA, and their respective grounds are tied together in a star connection. The J3 header provides connection to the common power bus described in the 5-6K Interface Board User's Guide (SLAU104). Table 1 shows the pinout of connector J3.

Table 1. Pinout of J3

Signal	Pin Number		Signal
Unused	1	2	Unused
+5VA	3	4	–5VA
DGND	5	6	AGND
Unused	7	8	Unused
Unused	9	10	+5VD

CAUTION

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The externally generated +2.5VDC precision voltage reference is jumper selectable via W1. The reference voltage can be selected either by the +2.5V onboard reference/buffer circuits (U4 and U5) or an external reference applied to J1-20. The EVM ships out of factory with the default position (shunt on W1 pins 1-2) of +2.5V reference that is supplied by REF3025 (U5), which is a 50ppm/°C with excellent line regulation and stability. The +2.5VDC reference will provide the DAC8831/32's voltage output range.

Moving the shunt at W1 to pins 2-3 allows an external reference applied to J1-20 to be used. Regardless of the reference source, U4 provides a reference buffer to the DAC8831/32. If no buffer circuit is desired, the EVM user can remove the resistor found at location R5 and apply an external reference directly to TP1, referenced to AGND.

1.3 EVM Basic Functions

This EVM is designed primarily as an evaluation platform to test certain functional characteristics of the DAC8831/32 digital-to-analog converter. The evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TI DSP or an appropriate signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8831/32EVM using a custom built cable.

The buffered DAC output can be monitored through pin 2 of J1 header connector. The EVM also provides a provision for Kelvin sense connection to increase performance of the DAC. This option does not come factory installed, and the EVM user must provide the necessary parts and labor.

A block diagram of the DAC8831/32EVM is shown in Figure 1 .

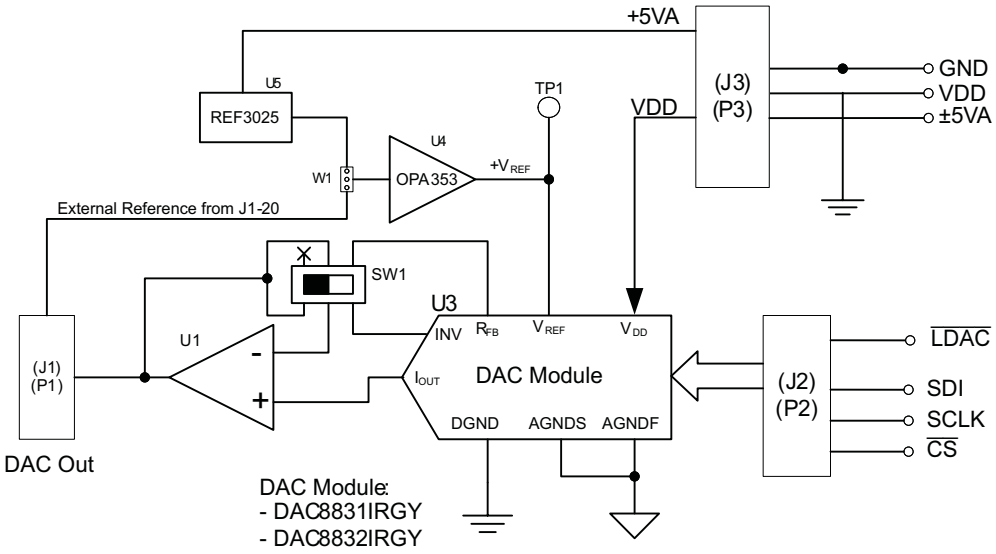


Figure 1. DAC8831/32EVM Block Diagram

1.4 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Related Documentation

Data Sheet	Literature Number
DAC8831	SLAS449
DAC8832	SBAS380
OPA735	SBOS282
OPA353	SBOS103
REF3025	SBVS032

1.5 Questions About This or Other Data Converter EVMs

If you have questions about this or other Texas Instruments Data Converter evaluation modules, feel free to e-mail the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product you have questions or concerns with.

2 PCB Design and Performance

This section talks about the layout design of the PCB describing the physical and mechanical characteristics of the EVM. It shows the resulting performance of the EVM, which can be compared to the device specification listed in the datasheet. The list of components used on the module is also included in this section.

2.1 PCB Layout

The DAC8831/32EVM is designed to demonstrate the performance quality of the installed DAC device under test, as specified in the datasheet. Careful analysis of the EVM's physical restrictions and factors that contributes to the EVM performance degradation is the key to a successful design implementation. The obvious attributes that contributes to the poor performance of the EVM can be avoided during the schematic design phase by properly selecting the right components and designing the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals and knowing or understanding the components mechanical attributes.

The obscure part of the design lies particularly in the layout process. The main concern is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane will do the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections; meaning, the analog traces should only be placed in the analog section, and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practice discussed can be seen in the following figures presented below.

The DAC8831/32EVM board is constructed on a two-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2000 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2 through Figure 5 show the individual artwork layers.

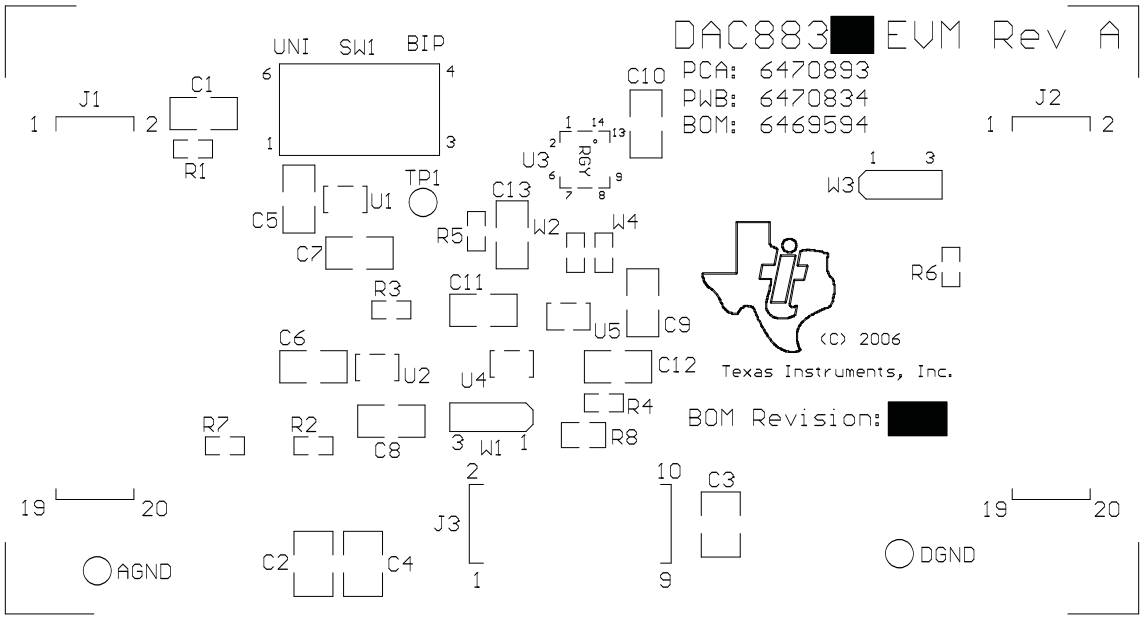


Figure 2. Top Silkscreen

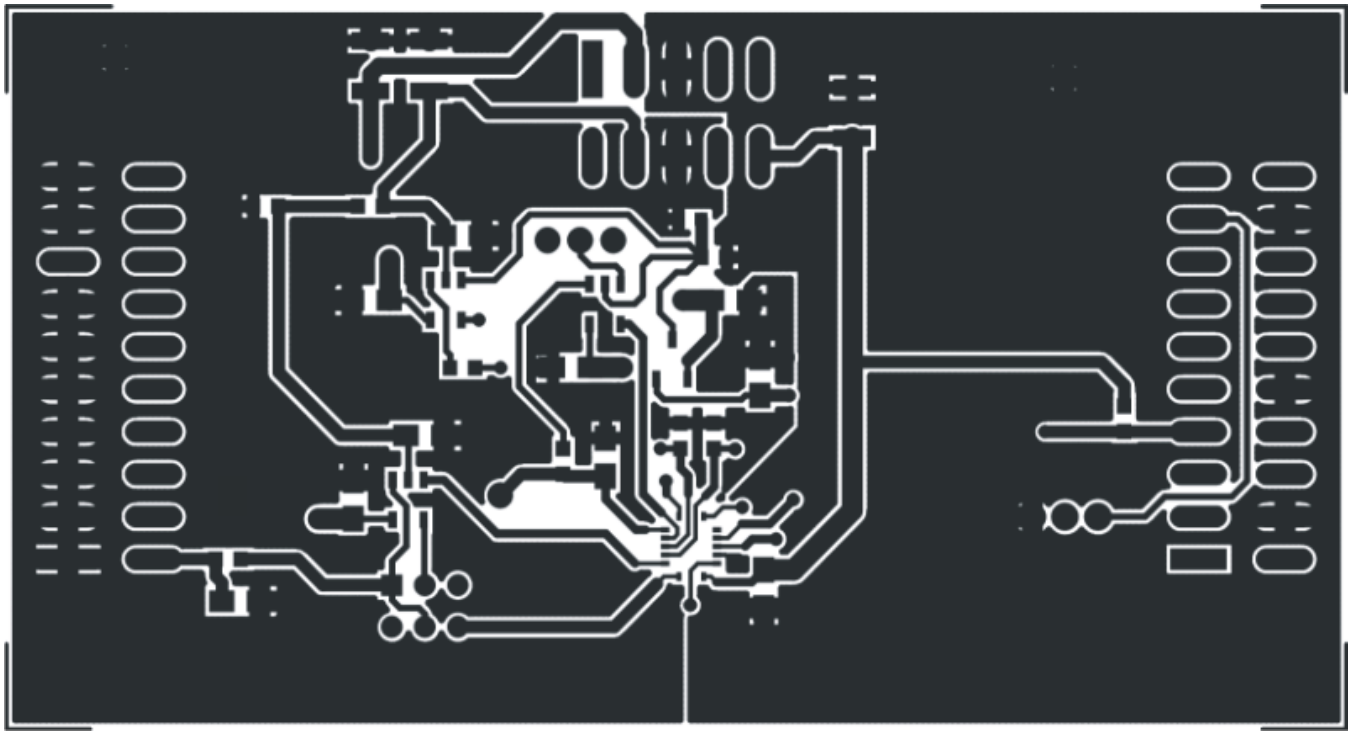


Figure 3. Layer 1 (Top Layer)

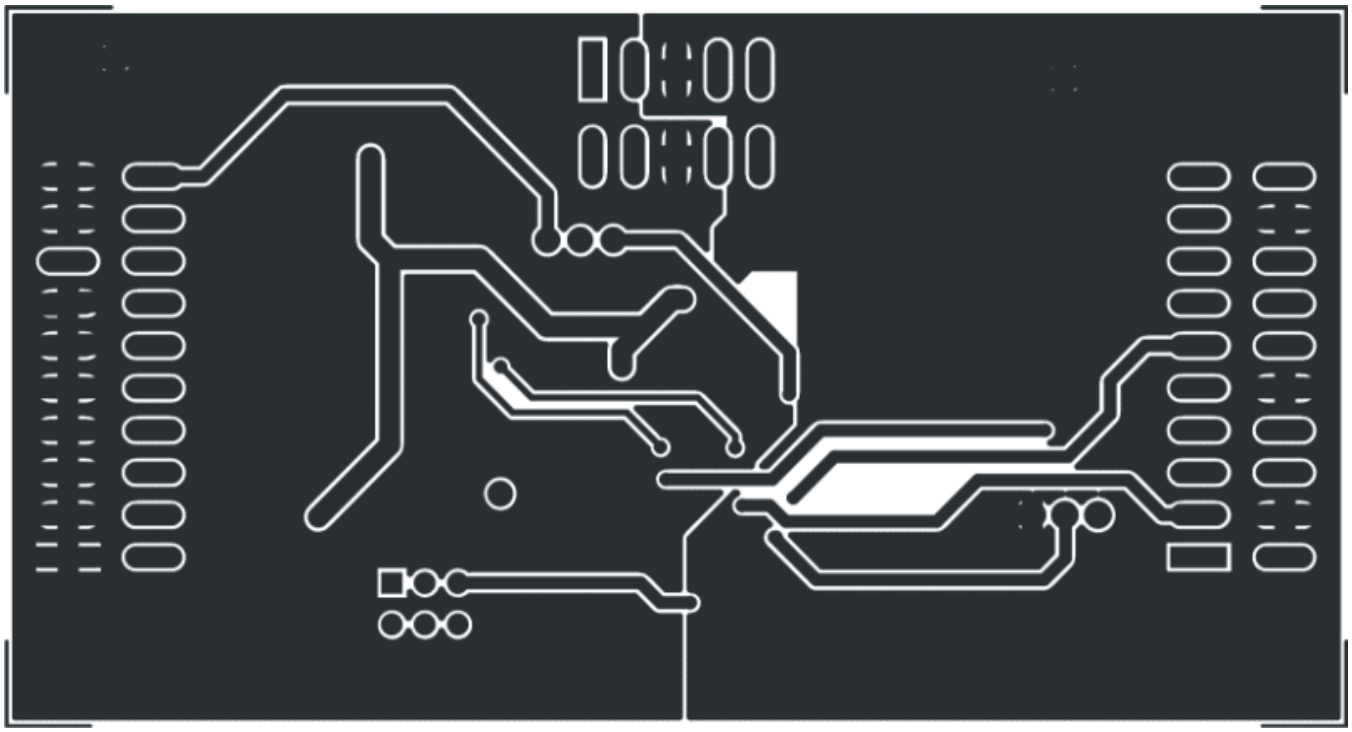


Figure 4. Layer 2 (Bottom Layer)

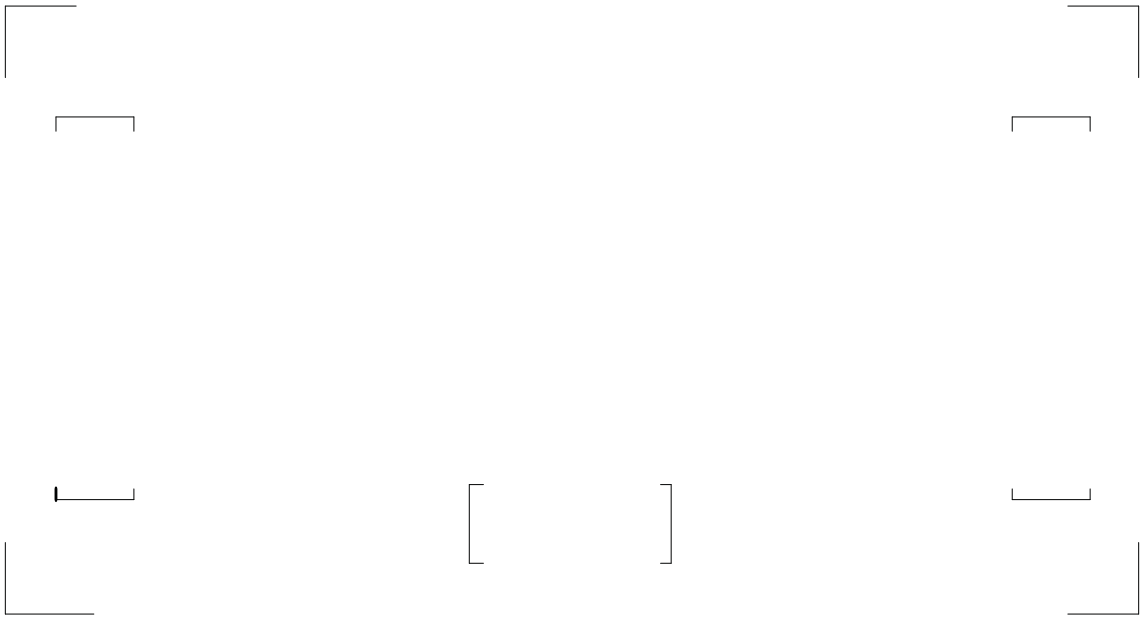


Figure 5. Bottom Silkscreen

2.2 EVM Performance Results

The EVM performance test is performed using a high density DAC bench test board, an Agilent 3458A digital multimeter and a PC running the LabVIEW® software. The EVM board is tested for all codes of the device under test (DUT) and is allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL results.

The results of the DAC8831/32EVM characterization test are shown in Figure 6. Take note that the DAC8831/32 uses the OPA735 for the output buffer.

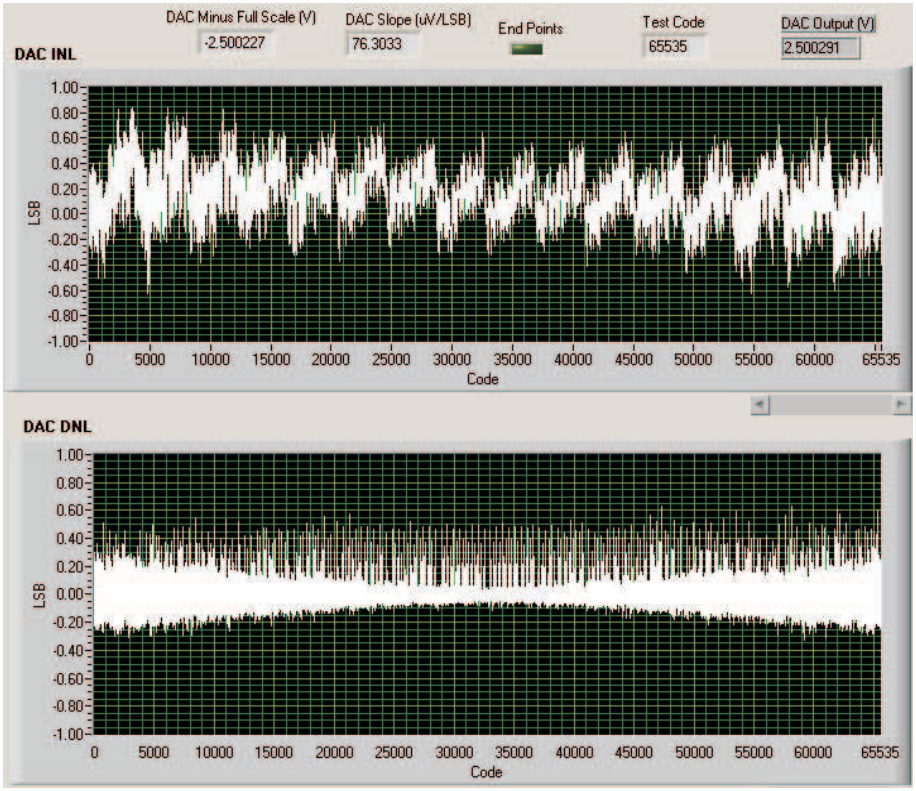


Figure 6. INL and DNL Characterization Plot for the DAC8832

3 EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a host processor.

Refer to the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide for more information about the DAC's serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

3.1 Factory Default Setting

The EVM board is set to its default configuration from factory as described in Table 2 to operate in bipolar ±2.5V output operation. The default jumper settings are shown in Figure 7.

Table 2. DAC8831/32EVM Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	Controls DAC reference source (default is U5 at 2.5VDC)
W3	1-2	Controls LDAC pin (default is DGND)
SW1	RIGHT	Controls analog output voltage (default is ±Vref)
R2	INSTALLED	Powers output buffer, U1 with ±5 V supplies.

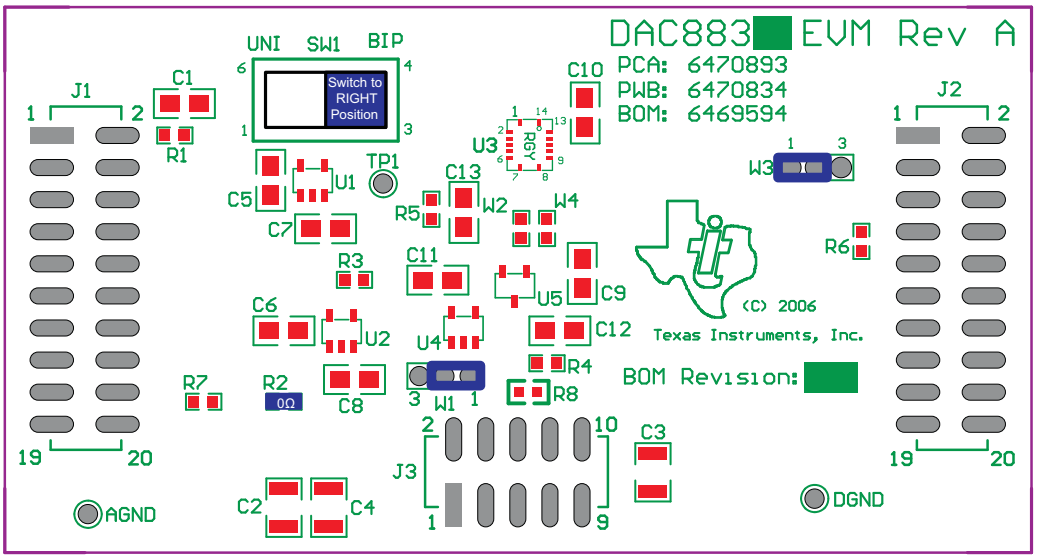


Figure 7. DAC8831/32EVM Default Configuration Setting

3.2 Host Processor Interface

The host processor basically drives the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to any host interface platform that the EVM user chooses to use. The EVM board allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J1 header connector.

To alleviate the tedious task of building customize cables, the DAC8831/32EVM is designed based on the modular EVM form factor from Texas Instruments. This EVM form factor allows direct evaluation of the DAC's performance and operating characteristics in conjunction with the MMB0 Modular EVM Motherboard and the DXP program from Texas Instruments.

This DAC EVM interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP of up to 50MHz clock speed. For more information regarding the serial interface of the particular DAC installed, please refer to the specific DAC data sheet, as listed in Section 1.4 of this user's guide.

3.3 Analog Interface

For maximum flexibility, the DAC8831/32EVM is designed for easy interfacing to multiple analog sources. Table 3 provides the pinout of connector J1. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row header/socket combination at J1. This header/socket provides access to the analog output pins of the DAC through the onboard buffer amplifier. Consult Samtec at www.samtec.com, or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 3. Pinout of J1

Pin Number	Signal	Description
J1-2	Vout	Buffer voltage output – range depends on the position of SW1 (see section 3.3.1)
J1-4	Unused	Pins are unused and should be left open for use with future amplifier and sensor output modules.
J1-6	Unused	
J1-8	Unused	
J1-10	Unused	
J1-12	Unused	
J1-14	Unused	
J1-16	Unused	
J1-18	REF(–)	Unused
J1-20	REF(+)	External reference source input (1.25 V to 5.5 V maximum)
J1-15	Unused	
J1-1–J1-19 (odd)	AGND	Analog ground connections (except J1-15)

3.3.1 EVM Output Voltage

Switch SW1 provides a means to allow unipolar or bipolar output operation of the DAC8831/32EVM. When the slide switch is to the right (screen marked BIP), the output voltage on J1-2 is ±VREF. If the onboard reference is used, this means that the output voltage is –2.5 Vdc to +2.5 Vdc. When the switch is to the left (screen marked UNI), the output from the buffer is 0 V to +2.5 Vdc.

For a wider dynamic output range, the EVM can be configured to use an external reference by moving the shunt at W1 to cover pins 2-3. In this case, an external reference from 1.25V to VDD may be applied to J1-20. For best performance, the external reference must be supplied by a clean dc source. Take note that the DAC output voltage may be limited by the input/output operating rails of the chosen output amplifier.

3.4 Digital Interface Control

The DAC8831EVM is designed for easy interfacing to multiple control platforms. Table 4 provides the pinout of connector J2. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the DAC8831EVM. Consult Samtec at www.samtec.com, or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 4. Pinout of J2

Pin Number	Signal	Description
J2-1	Unused	
J2-3	SCLK	Serial Clock
J2-5	Unused	
J2-7	$\overline{CS}$	Select to the DAC. Tied to the Frame Sync for DSP host systems – STE for SPI™ Host systems
J2-9	Unused	
J2-11	SDI	Serial Data Input
J2-13	Unused	
J2-15	Unused	
J2-17	$\overline{LDAC}$	Load DAC – Active low signal; enables DAC output updates – jumper configurable (see schematic). When LDAC is Low, the DAC latch is simultaneously updated with the content of the input register. Can be controlled by GPIO or tied low via W3.
J2-19	Unused	

3.5 Analog Output

The analog output is applied directly to J1 (top or bottom side) and can be further applied to optional amplifier and signal conditioning modules. The analog output range depends on the configuration of the EVM and the external reference applied at J1-20 or TP2. See Section 3.1 of this user guide and the DAC8831 data sheet (SLAS449) or the DAC8832 data sheet (SBAS380) to determine the maximum analog output range.

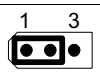
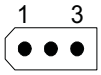
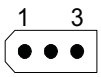
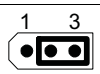
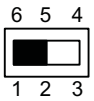
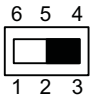
3.6 Load DAC ($\overline{LDAC}$)

Jumper W2 is provided to allow the selection of the signals applied to the DAC8831 or DAC8832 LDAC pin. The factory default condition for the EVM is to place a shunt jumper between pins 1-2 of W3. This ties the $\overline{LDAC}$ pin directly to ground for simultaneous updates of the DAC output buffer. When the shunt is moved to pins 2-3, an external $\overline{LDAC}$ signal may be applied to J2-17 to allow timed updates of the DAC output buffer.

3.7 Jumper and Switch Setting

Table 5 shows the function of each specific jumper setting of the EVM.

Table 5. Jumper Setting Function

Reference	Jumper Setting	Function
W1		Routes the 2.5V reference from U5 through buffer U4 for DAC VREF pin.
		Disconnect the onboard (U5) and external (via J1-20) references and use desired source of reference applied directly into W1-2.
		Routes the external reference source from J1-20 through buffer U4 for DAC V_{REF} pin.
W3		$\overline{\text{LDAC}}$ pin is tied directly to ground. Puts the DAC into transparent mode.
		$\overline{\text{LDAC}}$ pin is not connected.
		$\overline{\text{LDAC}}$ pin is tied directly to J2-17. Allows the host controller to update the DAC output simultaneously.
SW1		DAC is in unipolar mode of operation.
		DAC is in bipolar mode of operation.
Legend:		Indicates the corresponding pins that are shorted or closed.

3.8 Schematic

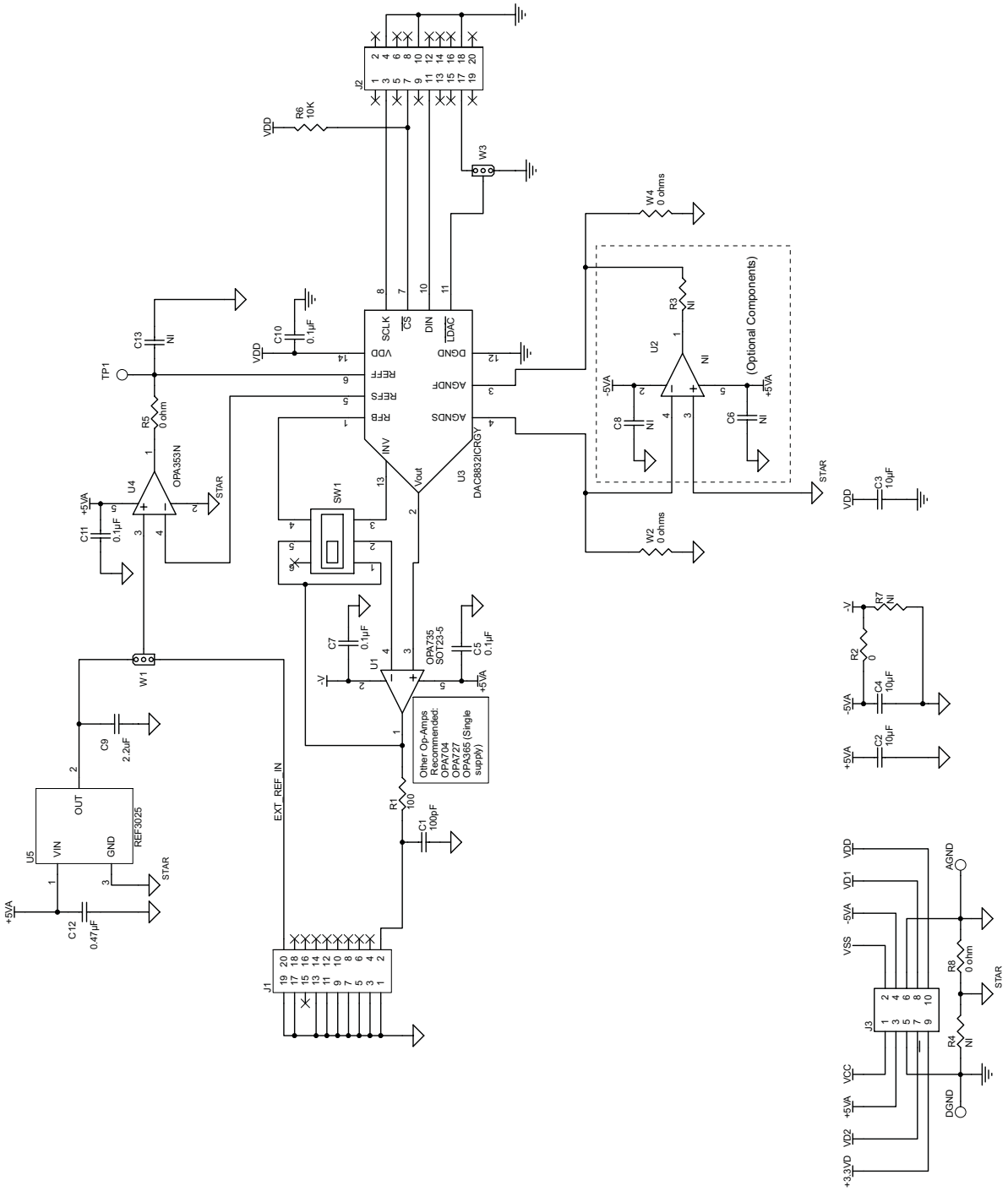


Figure 8. DAC8831/32EVM Schematic

4 Using the DAC8832EVM with DXP

The DAC8832EVM is compatible with the DAC eXerciser Program (DXP) from Texas Instruments. DXP is a tool that can generate the necessary control signals required to output various signals and waveforms from the device installed on the DAC8832EVM. The DAC8832EVM-PDK kit combines the DAC8832EVM board with the DSP-based modular motherboard MMB0. The kit includes the DXP software for evaluation using any available USB port on a Microsoft® Windows® XP-based computer.

DXP is a program for controlling the digital input signals such as the clock, $\overline{CS}$, and SDI. Wave tables are built into the DSP software to allow sine, ramp, triangle, and square wave signals to be generated by the DAC8832. Straight dc outputs can also be obtained.

The DAC8832EVM-PDK uses the DSP-based MMB0 to control the DAC8832EVM using the DXP software For complete information about installing and configuring DXP, see the DXP User's Guide, available for download from the TI web site. This section covers the specific operation of the DAC8832EVM-PDK.

4.1 Hardware

The hardware consists of two primary components: the DAC8832EVM itself and a modular motherboard called the MMB0. The MMB0 board houses a TMS320VC5507 DSP that controls the serial interface to the device loaded on the EVM board.

The hardware must be configured such that the DAC8832EVM is plugged onto the MMB0 aligning female connectors J4, J2 and J6 (on the bottom side of the DAC8832VM) with male connectors J7, J4 and J5 on the MMB0. The assembled hardware is shown in Figure 9.

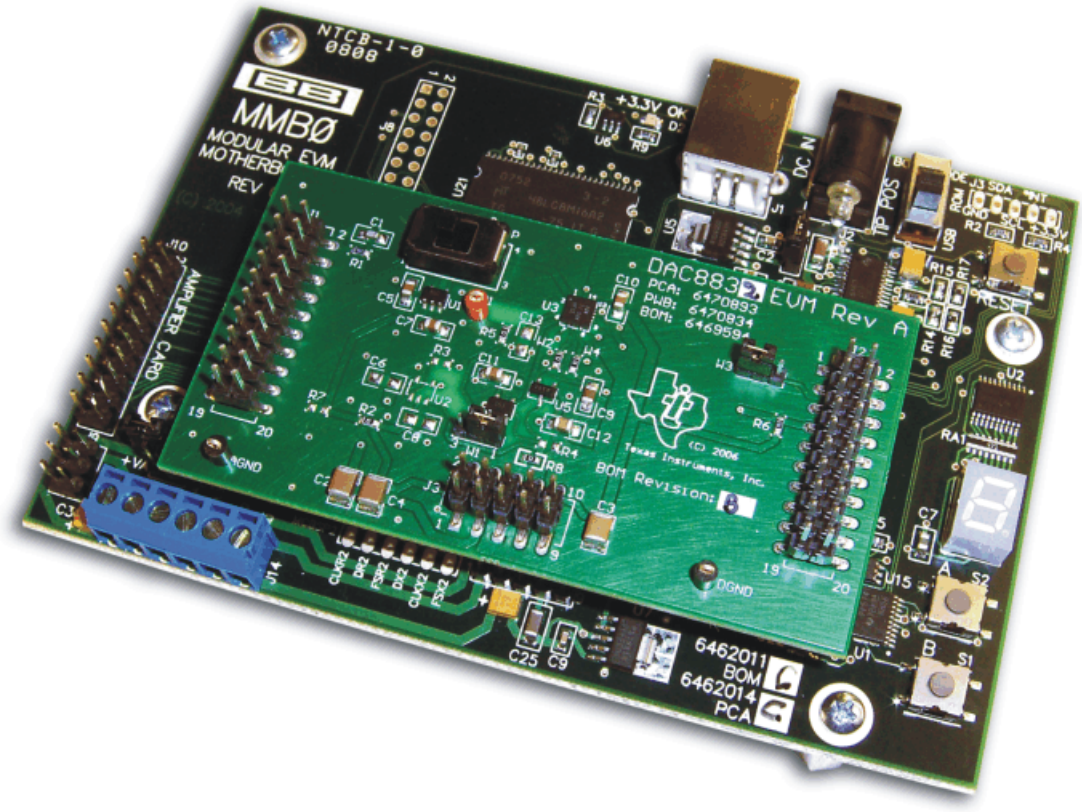


Figure 9. MMB0 with DAC8832EVM Installed

CAUTION

Use caution when assembling the boards. It is possible to misalign the connectors and damage both the EVM and the motherboard.

CAUTION

DO NOT connect the MMB0 to your PC before installing the DXP software as described in the DXP User's Guide. Installing the software first ensures that the necessary drivers are properly loaded to run the hardware.

4.2 MMB0 Power Supplies

Several power connections are required for the hardware to work properly. For the MMB0, the supplied 6-V ac/dc converter is all that is necessary. Be sure that J12 on the MMB0 board is closed before connecting the ac/dc adapter to the *DC In* connector of the MMB0. This supply provides all power to the digital portion of the DAC8832EVM as well as all necessary power for the DSP. Clean, well-regulated analog power for the DAC8832EVM should be supplied externally via J14, a six-position screw terminal mounted in the lower left corner of the MMB0 board.

CAUTION

When using external power supplies applied to J14 on the MMB0, please ensure all shorting blocks from J13 are completely removed. Permanent damage to the MMB0 may occur otherwise.

From left to right, the J14 screw terminal connections are –VA, +VA, +5VA, –5VA, +5VD, and GND. The 5V from the ac/dc adapter can be connected to the +VA or the +5VA by installing a jumper across JP13A or JP13B. If the jumpers are not installed, the analog V_{SS}, V_{CC}, +5VA, and –5VA may be applied directly to the –VA, +VA, +5VA, and –5VA screw terminals at J14 on the MMB0 (referenced to the GND terminal).The DAC8832 board power requirements are described in Section 1.2 of this manual.

4.3 Software: Running DXP

Install DXP on a laptop or personal computer running Windows XP as shown in the detailed instructions in the DXP User's Guide (TI document SBAU146). Run the DXP program by clicking on the DXP icon on your desktop, or by browsing to your installation directory.

Before you can generate signals with DXP, a DAC EVM configuration file must be loaded. To load a configuration file, select the desired DAC from the configuration list under the *DAC* menu, as Figure 10 illustrates. Choose the DAC configuration file for the device installed on the EVM.

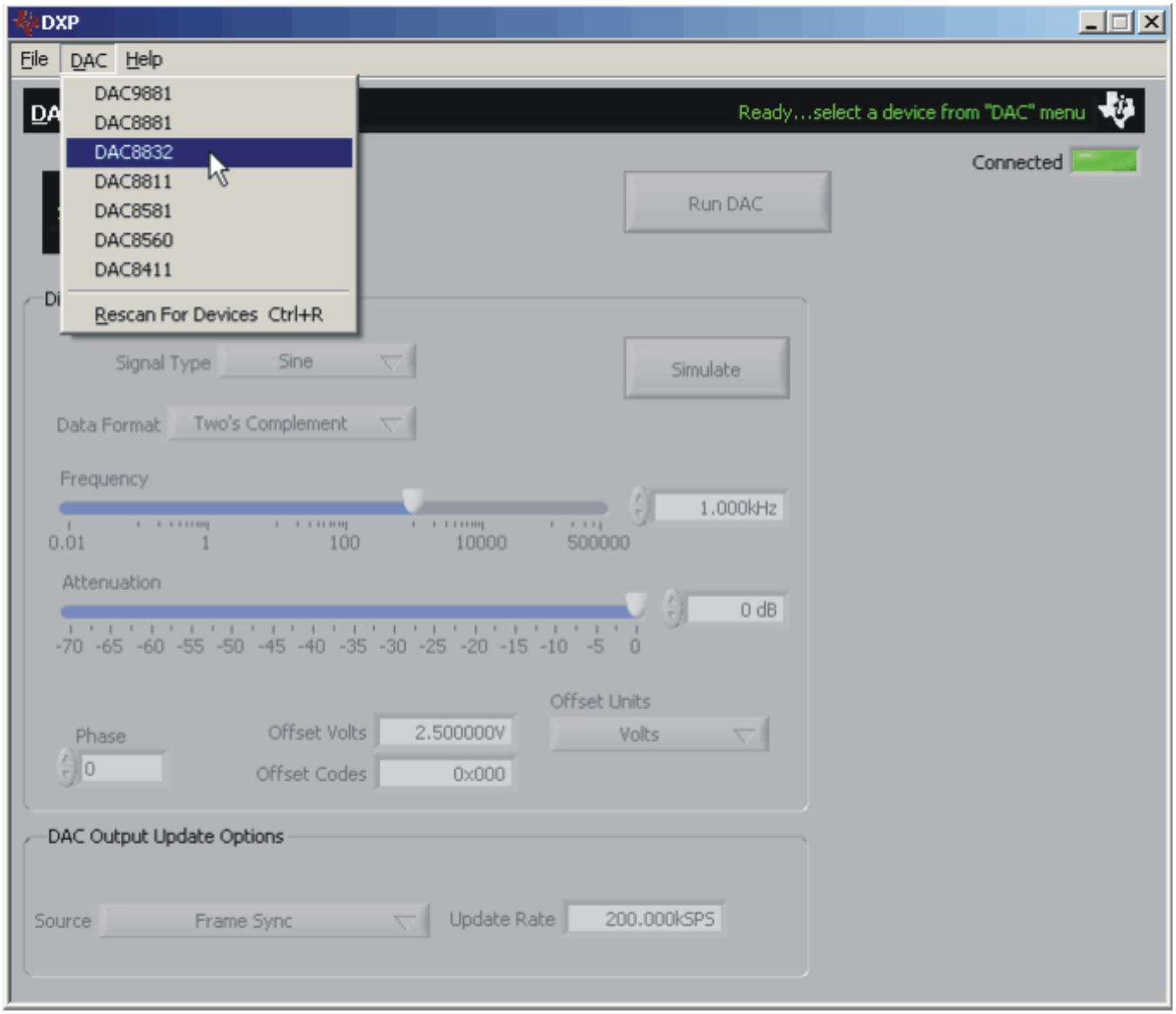


Figure 10. Loading a DAC8832EVM Configuration

The DXP software defaults to output a 1-kHz sine wave from the DAC. Other waveform options include square, sawtooth, triangle, and dc output options, as described in the DXP User's Guide. The frequency and amplitude of the output waveform are controlled by sliders on the DXP software interface. The DAC update rate can also be modified, as shown in Figure 11.

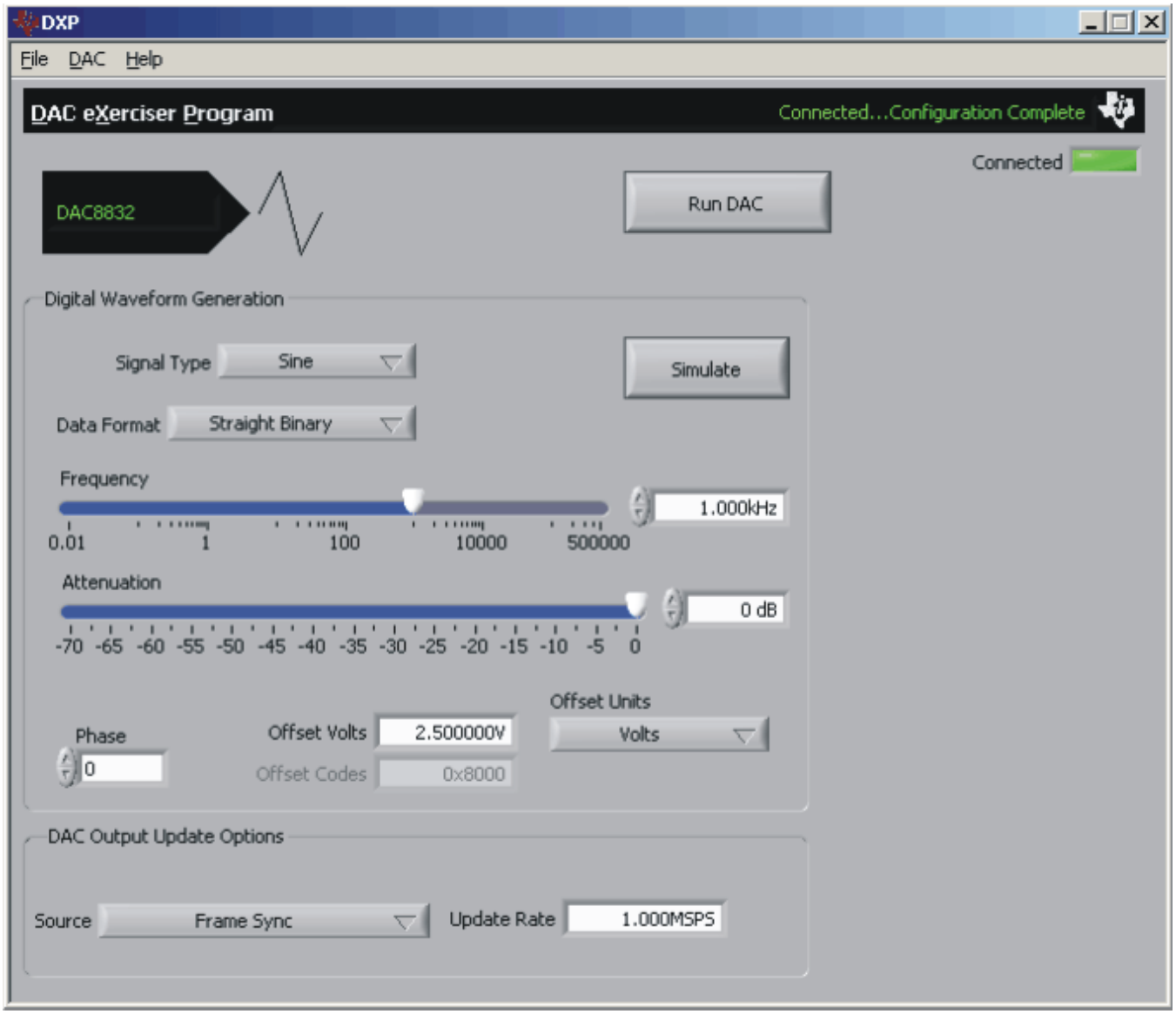


Figure 11. DAC8832EVM: Frequency/Amplitude and Update Rate Adjustments

4.4 DAC Output Update Options

The DXP software also allows the user to choose several DAC output update options, as Figure 12 shows.

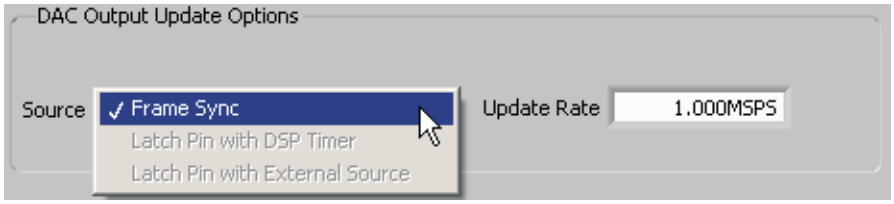


Figure 12. DAC Output Update Options

Table 6 lists the details of these options.

Table 6. Output Update Features

Options	Detailed Description
Frame Sync	The DXP software defaults to Frame Sync. The Frame Sync output of the MMB0 connects to the $\overline{CS}$ input of the DAC8832. In this mode, the $\overline{LDAC}$ pin is held low and the DAC latch is transparent. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated via SDI. Place a shunt jumper on W3 covering pins 1-2 (default) to use this option.
Latch with DSP Timer	Jumper W3 on the EVM controls LDAC selection. In this configuration, a timer function on the MMB0 applies a pulse to the $\overline{LDAC}$ pin and the output of the DAC8832 is updated synchronously with the falling edge of the applied pulse. Place the shunt jumper on W3 pins 2-3 to use this feature.
Latch with External Timer	N/A
Update Rate	User Input - enter the desired DAC update rate; 1MSPS is the default

5 Bill of Materials

Table 7. Parts Lists[(1)]

Item #	QTY	Designator	Manufacturer	Part Number	Description
1	1	C1	TDK	C1608C0G1H101J	100 pF, 0603, C0G, 50V, 5% Tol, Multilayer Ceramic Capacitor
2	3	C2 C3 C4	TDK	C3216Y5V1C106Z	10 µF, 1206, Y5V, 10V, 10% Tol, Multilayer Ceramic Capacitor
3	4	C5 C7 C10 C11	TDK	C2012X7R1E104K	0.1 µF, 0805, X7R, 50V, 10% Tol, Multilayer Ceramic Capacitor
4	3	C6 C8 C13	TDK	C2012X7R1E104K	Not Installed
5	1	C9	TDK	C2012X5R1A225M	2.2 µF, 0805, Y5V, 10V, 10% Tol, Multilayer Ceramic Capacitor SMD
6	1	C15	TDK	C2012X7R1E474M	0.47 µF, 0805, Ceramic, Y5V, 10V, 10% Tol, Multilayer Ceramic Capacitor
7	1	J1 J2 (top side)	Samtec	TSM-110-01-T-DV-P	10 Pin, Dual Row, SMT Header (20 Pos.)
8	1	J1B J2B (bottom side)	Samtec	SSW-110-22-F-D-VS-K	10 Pin, Dual Row, SMT Socket (20 Pos.)
9	1	J3 (top side)	Samtec	TSM-105-01-T-DV-P	5 Pin, Dual Row, SMT Header (10 Pos.)
10	2	J3B (bottom side)	Samtec	SSW-105-22-F-D-VS-K	5 Pin, Dual Row, SMT socket (10 Pos.)
11	1	R1	Yageo America	9C06031A1000JLHFT	100 Ω, 0603, 5%, 0.1 W resistor
12	1	R2 W2 W4	Yageo America	9C06031A0R00JLHFT	0 Ω, 0805, 5%, 0.1 W resistor
13	1	R3 R4 R7			Not Installed
14	2	R5	Yageo America	9C06031A33R0JLHFT	33 Ω, 0603, 5%, 0.1 W resistor
15	2	R6	Yageo America	9C06031A1002JLHFT	10 kΩ, 0603, 5%, 0.1 W resistor
16	1	SW1	E Switch	EG2209	DPDT Slide Switch
17	1	TP2	Keystone	5001	Red Test Point Loop
18	5	DGND AGND	Keystone	5000	Black Test Point Loop
19	2	U1	Texas Instruments	OPA735AIDBVT	OPA735
20	1	U2	Texas Instruments	OPA735AIDBVT	Not Installed – Optional Component
21	3	U3	Texas Instruments	DAC8831ICRGY	16-Bit, Unbuffered Voltage Output, Reset to Zero-Scale DAC
				DAC8832ICRGY	16-Bit, Unbuffered Voltage Output, Reset to Mid-Scale DAC
22	3	U4	Texas Instruments	OPA353NA	OPA353
23	1	U5	Texas Instruments	REF3025AIDBZT	REF3025
24	1	W1 W3	Samtec	TSW-103-07-L-S	3 Pin, Single Row, TH Header
NOTE:					

(1) P2, P4, and P6 parts are not shown in the schematic diagram. All the ***P*** designated parts are installed on the bottom side of the PCB opposite the ***J*** designated counterpart. For example, J2 is installed on the topside while P2 is installed on the bottom side opposite of J2. The following parts are not installed: J1, J3, R1, R2, and R3 .

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of Table 1 (±5 VDC) and the output voltage range of ±5 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265