

# NTHC5513

## MOSFET – Power, Complementary ChipFET 20 V, +3.9 A / -3.0 A

### Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Featuring Complementary Pair
- ChipFET Package Provides Great Thermal Characteristics Similar to Larger Packages
- Low  $R_{DS(on)}$  in a ChipFET Package for High Efficiency Performance
- Low Profile (< 1.10 mm) Allows Placement in Extremely Thin Environments Such as Portable Electronics
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Load Switch Applications Requiring Level Shift
- DC-DC Conversion Circuits
- Drive Small Brushless DC Motors
- Designed for Power Management Applications in Portable, Battery Powered Products

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	20	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 12$	V	
Continuous Drain Current (Note 1)	N-Ch Steady State	$T_A = 25^\circ\text{C}$	$I_D$	2.9	A
			$T_A = 85^\circ\text{C}$	2.1	
		$t \leq 5$	$T_A = 25^\circ\text{C}$	3.9	
	P-Ch Steady State	$T_A = 25^\circ\text{C}$	$I_D$	-2.2	
			$T_A = 85^\circ\text{C}$	-1.6	
		$t \leq 5$	$T_A = 25^\circ\text{C}$	-3.0	
Pulsed Drain Current (Note 1)	N-Ch	$t = 10 \mu\text{s}$	$I_{DM}$	12	A
	P-Ch	$t = 10 \mu\text{s}$		-9.0	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	1.1	W
		$T_A = 25^\circ\text{C}$		2.1	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

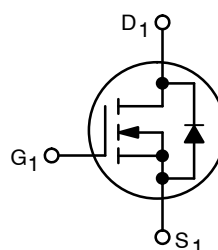
1. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



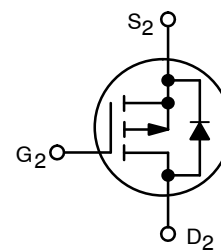
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[www.onsemi.com](http://www.onsemi.com)

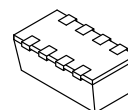
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
N-Channel 20 V	60 m $\Omega$ @ 4.5 V	3.9 A
	80 m $\Omega$ @ 2.5 V	
P-Channel -20 V	130 m $\Omega$ @ -4.5 V	-3.0 A
	200 m $\Omega$ @ -2.5 V	



N-Channel MOSFET

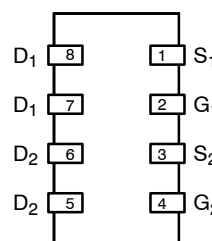


P-Channel MOSFET

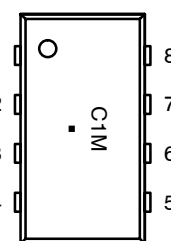


ChipFET  
CASE 1206A  
STYLE 2

### PIN CONNECTIONS



### MARKING DIAGRAM



C1 = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTHC5513T1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHC5513

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Max	Unit
Junction-to-Ambient (Note 1)	Steady State	$R_{\theta JA}$	110	°C/W
	$t \leq 5$		60	

2. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS (Note 3)

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0\text{ V}$	$I_D = 250\ \mu\text{A}$	20		V
		P		$I_D = -250\ \mu\text{A}$	-20		
Zero Gate Voltage Drain Current	$I_{DSS}$	N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$			1.0	$\mu\text{A}$
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-1.0	
		N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}, T_J = 85^\circ\text{C}$			5	
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}, T_J = 85^\circ\text{C}$			-5	
Gate-to-Source Leakage Current	$I_{GSS}$		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250\ \mu\text{A}$	0.6		1.2	V
		P		$I_D = -250\ \mu\text{A}$	-0.6		-1.2	
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$			0.058	0.080	$\Omega$
		P	$V_{GS} = -4.5\text{ V}, I_D = -2.2\text{ A}$			0.130	0.155	
		N	$V_{GS} = 2.5\text{ V}, I_D = 2.3\text{ A}$			0.077	0.115	
		P	$V_{GS} = -2.5\text{ V}, I_D = -1.7\text{ A}$			0.200	0.240	
Forward Transconductance	$g_{FS}$	N	$V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$			6.0		S
		P	$V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$			6.0		

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	N	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}$		180		pF		
		P		$V_{DS} = -10\text{ V}$		185				
Output Capacitance	$C_{OSS}$	N		$V_{DS} = 10\text{ V}$		80				
		P		$V_{DS} = -10\text{ V}$		95				
Reverse Transfer Capacitance	$C_{RSS}$	N		$V_{DS} = 10\text{ V}$		25				
		P		$V_{DS} = -10\text{ V}$		30				
Total Gate Charge	$Q_{G(TOT)}$	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$			2.6		4.0	nC
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$			3.0		6.0	
Gate-to-Source Gate Charge	$Q_{GS}$	N	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$			0.6				
		P	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$			0.5				
Gate-to-Drain "Miller" Charge	$Q_{GD}$	N	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$			0.7				
		P	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$			0.9				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width  $\leq 250\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 4)							
Turn-On Delay Time	t <sub>d(ON)</sub>	N	V <sub>DD</sub> = 16 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.9 A, R <sub>G</sub> = 2.5 Ω		5.0	10	ns
Rise Time	t <sub>r</sub>				9.0	18	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				10	20	
Fall Time	t <sub>f</sub>				3.0	6.0	
Turn-On Delay Time	t <sub>d(ON)</sub>	P	V <sub>DD</sub> = -16 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.2 A, R <sub>G</sub> = 2.5 Ω		7.0	12	
Rise Time	t <sub>r</sub>				13	25	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				33	50	
Fall Time	t <sub>f</sub>				27	40	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 5)	V <sub>SD</sub>	N	V <sub>GS</sub> = 0 V	I <sub>S</sub> = 2.6 A		0.8	1.15	V
		P		I <sub>S</sub> = -2.1 A		-0.8	-1.15	
Reverse Recovery Time (Note 4)	t <sub>RR</sub>	N	V <sub>GS</sub> = 0 V, dI <sub>S</sub> / dt = 100 A/μs	I <sub>S</sub> = 1.5 A		12.5		ns
		P		I <sub>S</sub> = -1.5 A		32		
Charge Time	t <sub>a</sub>	N		I <sub>S</sub> = 1.5 A		9.0		
		P		I <sub>S</sub> = -1.5 A		10		
Discharge Time	t <sub>b</sub>	N		I <sub>S</sub> = 1.5 A		3.5		
		P		I <sub>S</sub> = -1.5 A		22		
Reverse Recovery Charge	Q <sub>RR</sub>	N		I <sub>S</sub> = 1.5 A		6.0		nC
		P		I <sub>S</sub> = -1.5 A		15		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.
5. Pulse Test: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

TYPICAL N-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

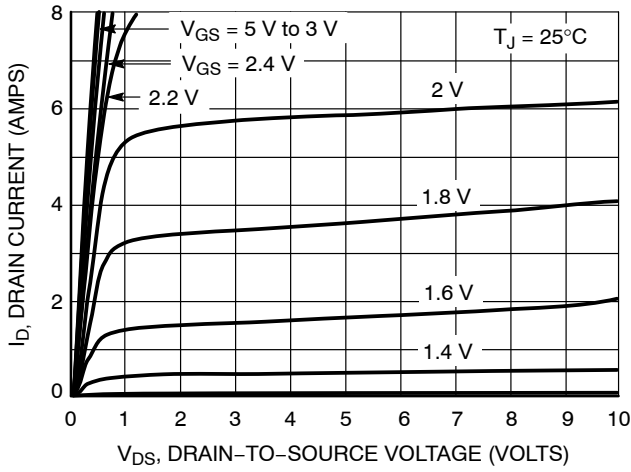


Figure 1. On-Region Characteristics

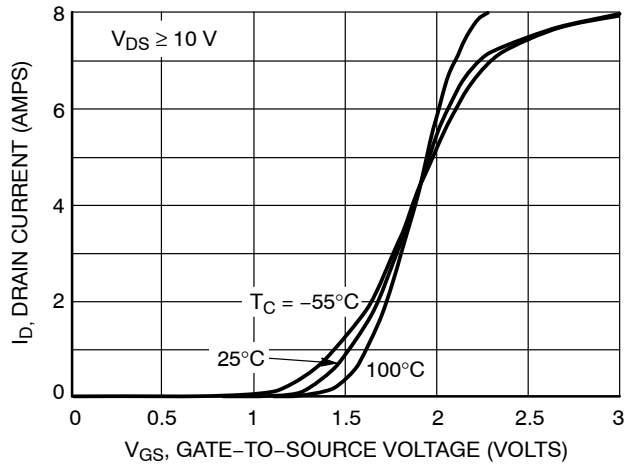


Figure 2. Transfer Characteristics

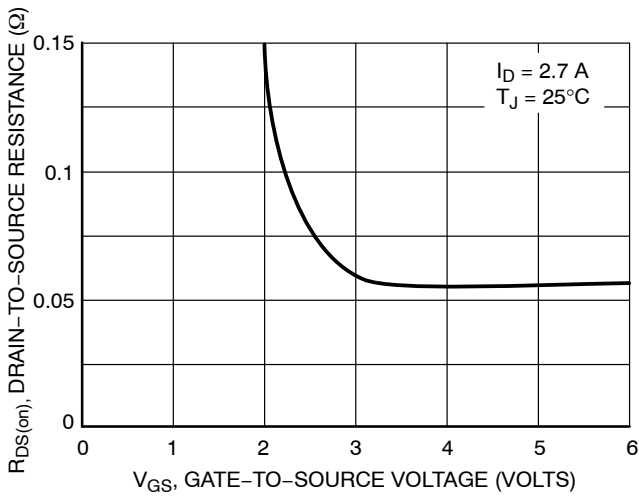


Figure 3. On-Resistance vs. Gate-to-Source Voltage

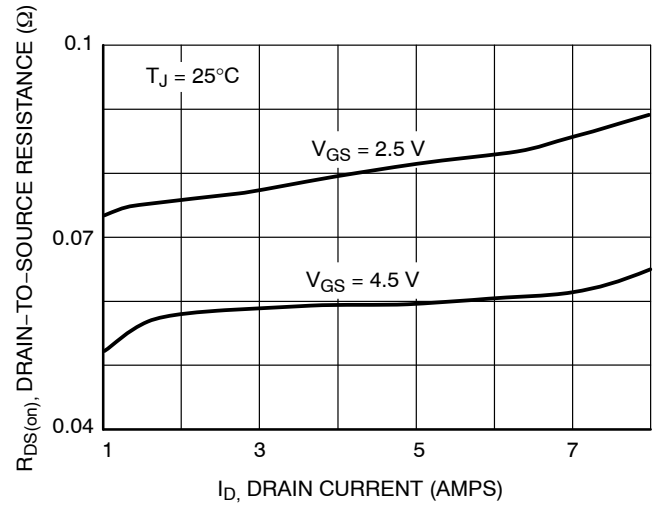


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

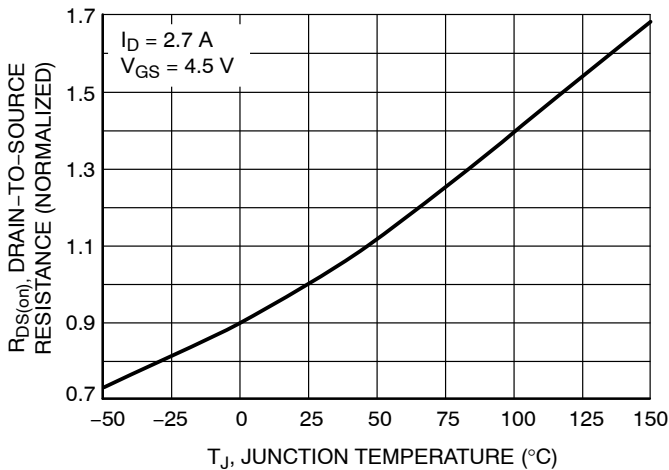


Figure 5. On-Resistance Variation with Temperature

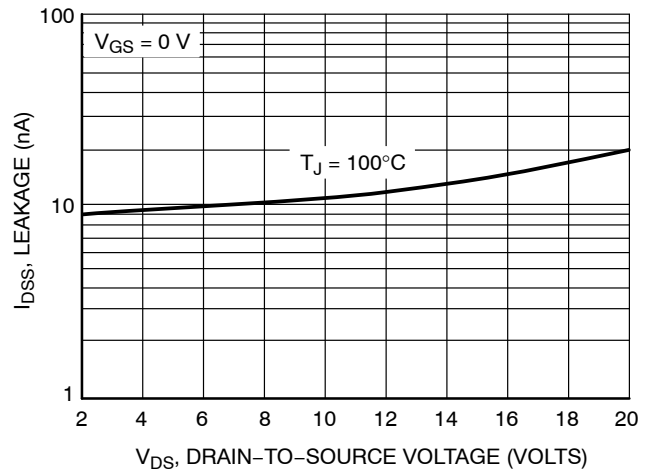


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

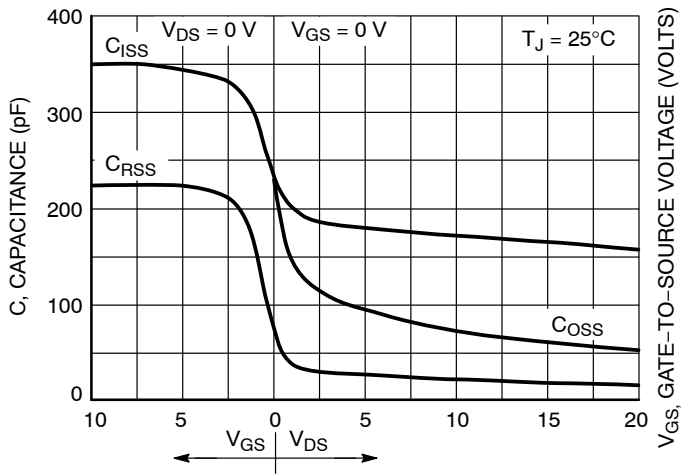


Figure 7. Capacitance Variation

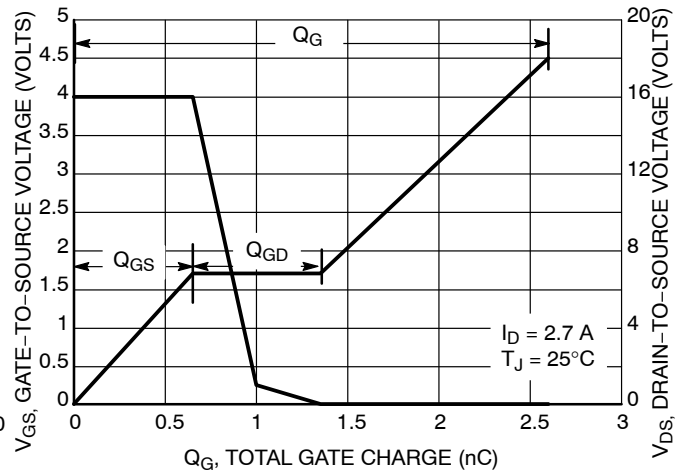


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

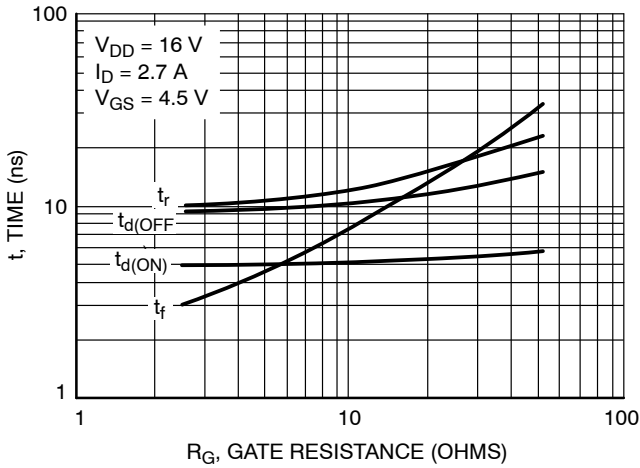


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

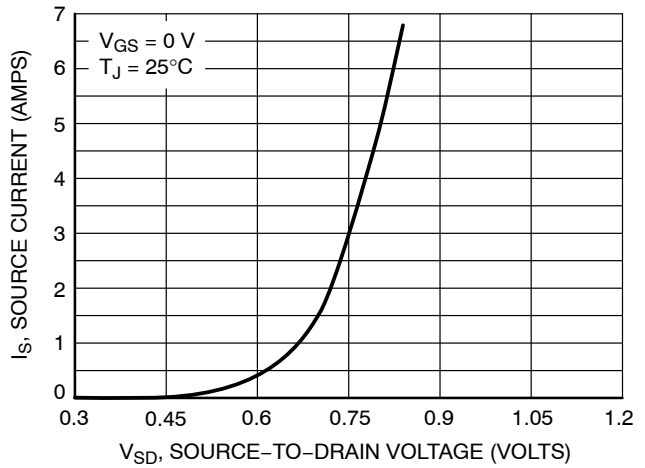


Figure 10. Diode Forward Voltage vs. Current

TYPICAL P-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

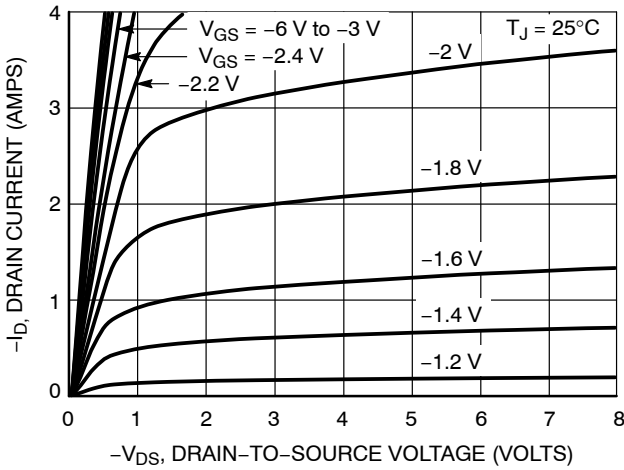


Figure 11. On-Region Characteristics

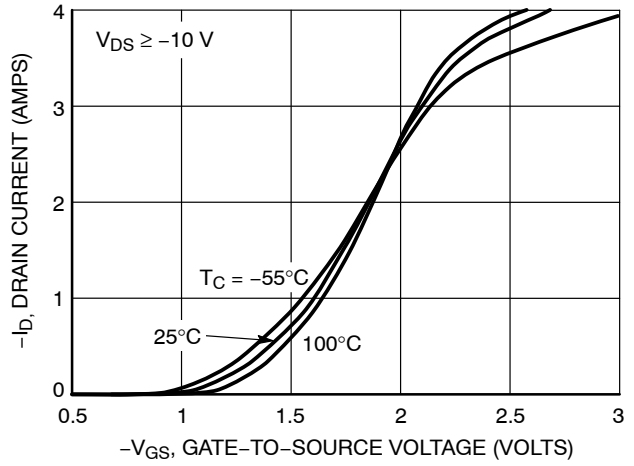


Figure 12. Transfer Characteristics

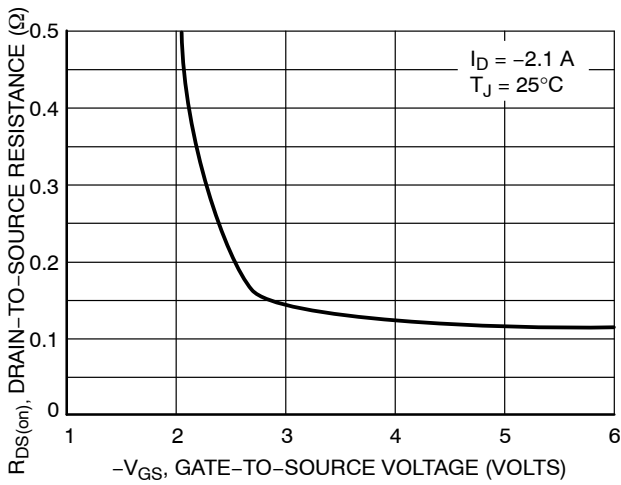


Figure 13. On-Resistance vs. Gate-to-Source Voltage

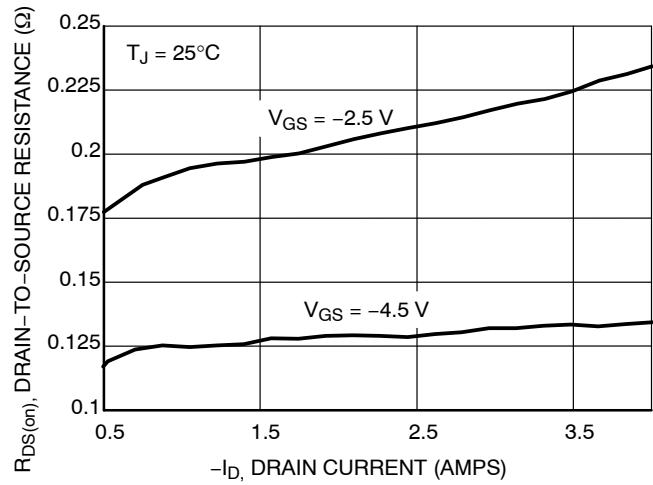


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

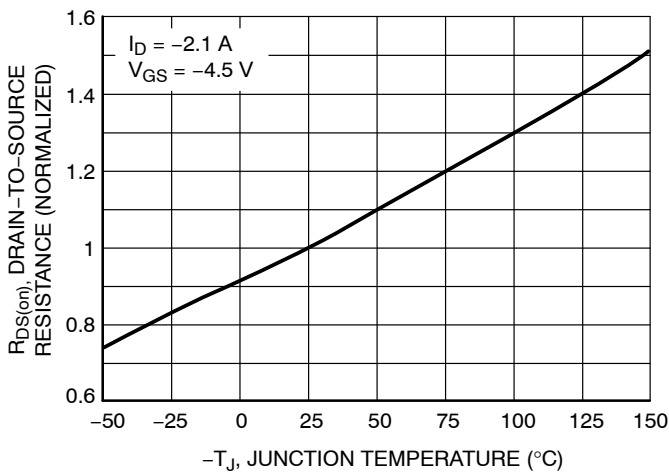


Figure 15. On-Resistance Variation with Temperature

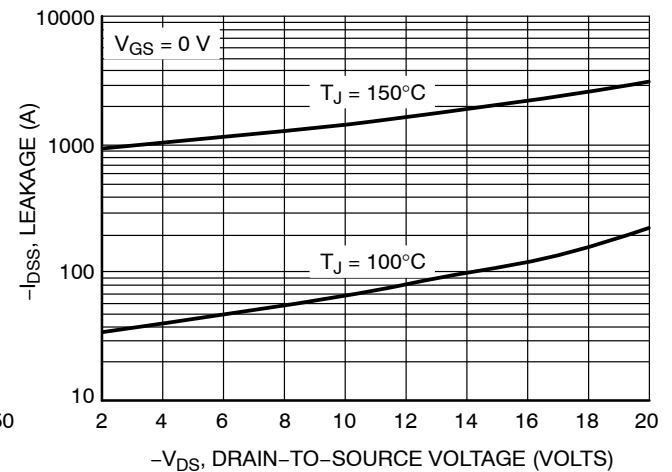
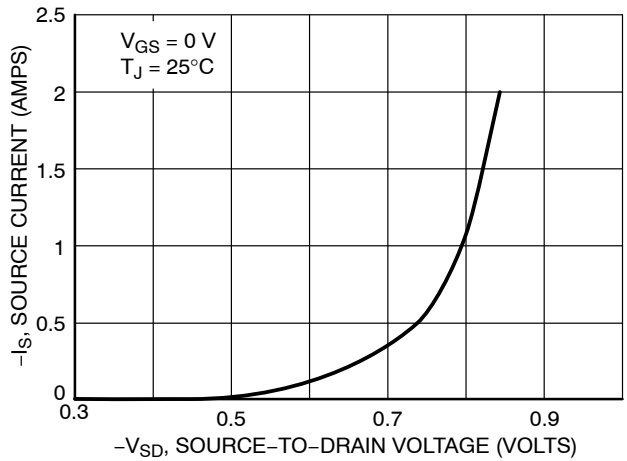
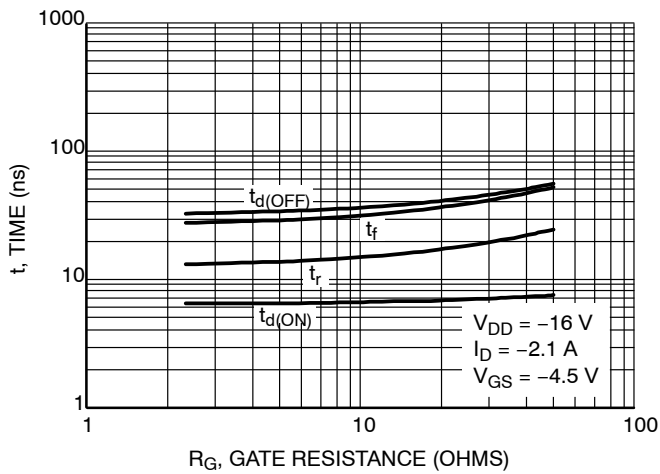
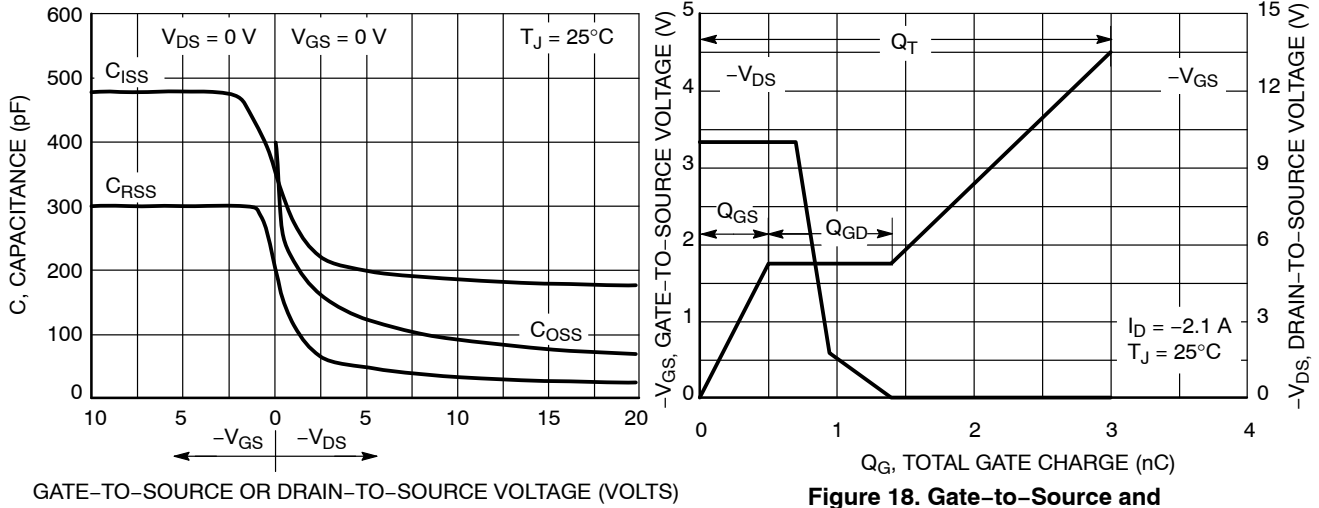


Figure 16. Drain-to-Source Leakage Current vs. Voltage

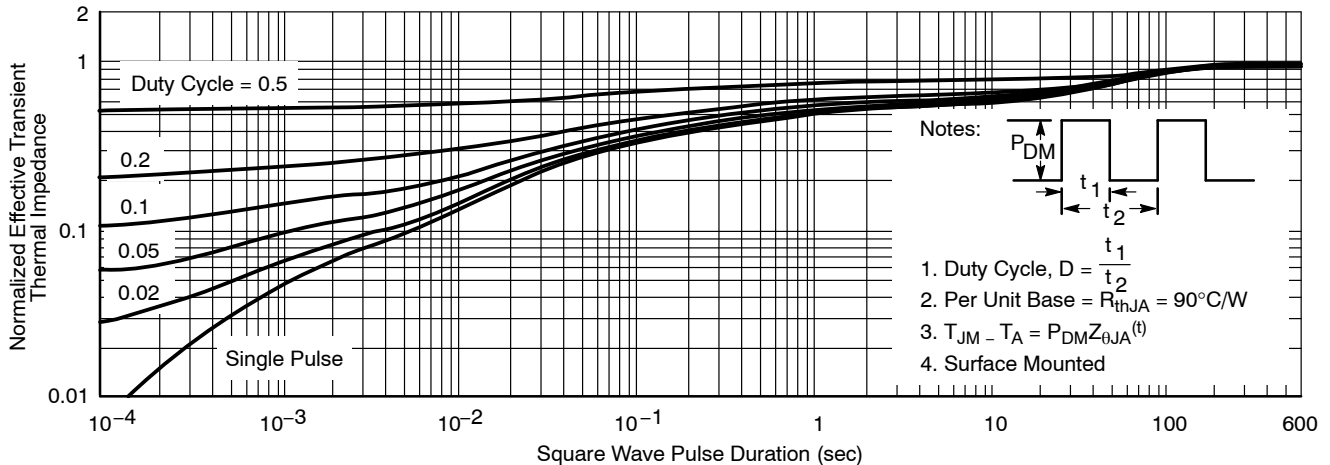
TYPICAL P-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)



TYPICAL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)



# NTHC5513

## SOLDERING FOOTPRINT\*

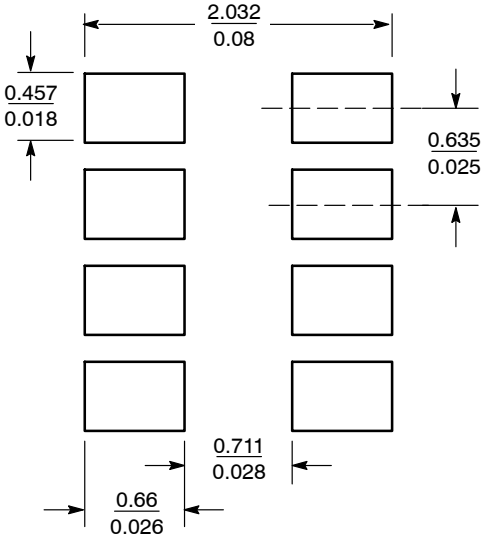


Figure 22. Basic

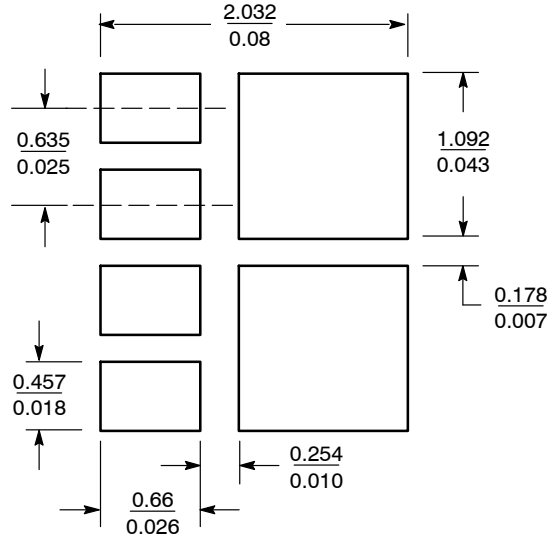


Figure 23. Style 2

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 22. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 23 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

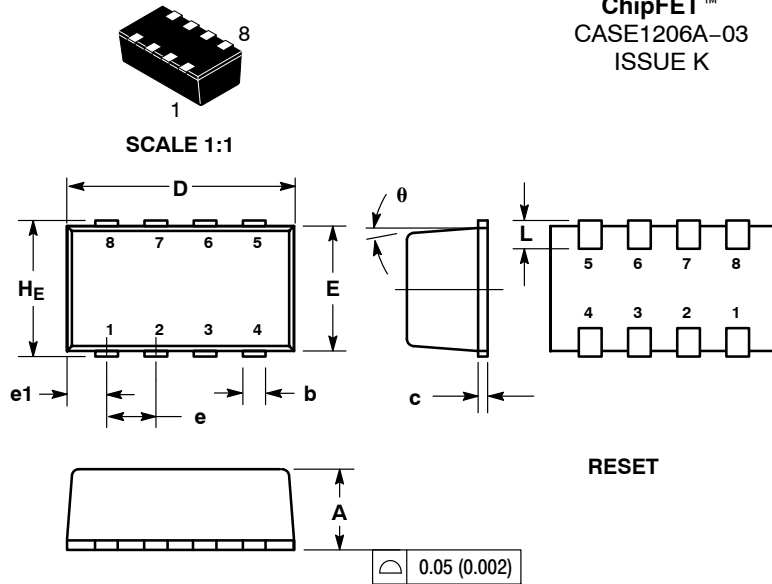


### ChipFET™

#### CASE1206A-03

#### ISSUE K

DATE 19 MAY 2009



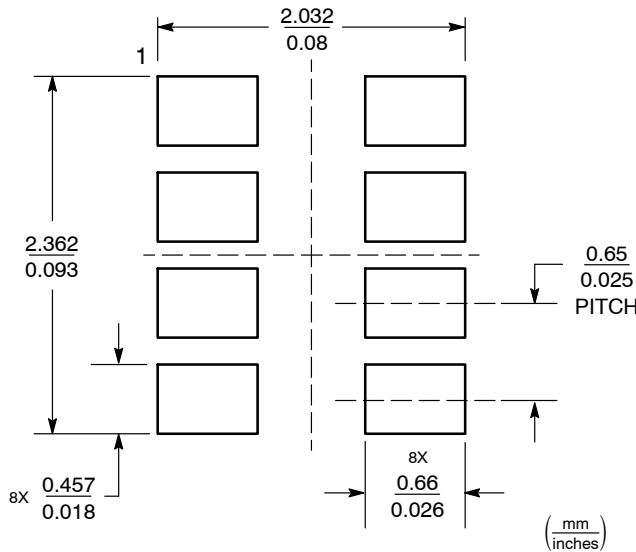
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

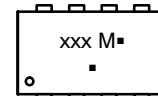
- |   |   |   |  |   |   |
|---|---|---|--|---|---|
| <b>STYLE 1:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. GATE<br>5. SOURCE<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN | <b>STYLE 2:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1 | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE | <b>STYLE 4:</b><br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. COLLECTOR<br>4. BASE<br>5. EMITTER<br>6. COLLECTOR<br>7. COLLECTOR<br>8. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. DRAIN<br>4. DRAIN<br>5. SOURCE<br>6. GATE<br>7. CATHODE<br>8. CATHODE | <b>STYLE 6:</b><br>PIN 1. ANODE<br>2. DRAIN<br>3. DRAIN<br>4. GATE<br>5. SOURCE<br>6. DRAIN<br>7. DRAIN<br>8. CATHODE / DRAIN |
|---|---|---|--|---|---|

### SOLDERING FOOTPRINT



### Basic Style

### GENERIC MARKING DIAGRAM\*



- xxx = Specific Device Code
  - M = Month Code
  - = Pb-Free Package
- (Note: Microdot may be in either location)

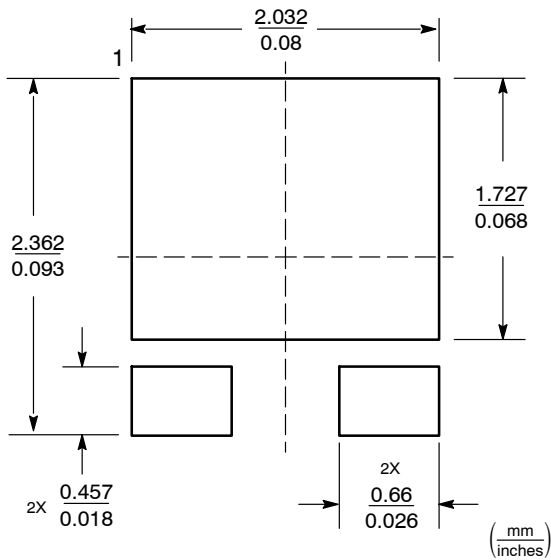
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

### OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

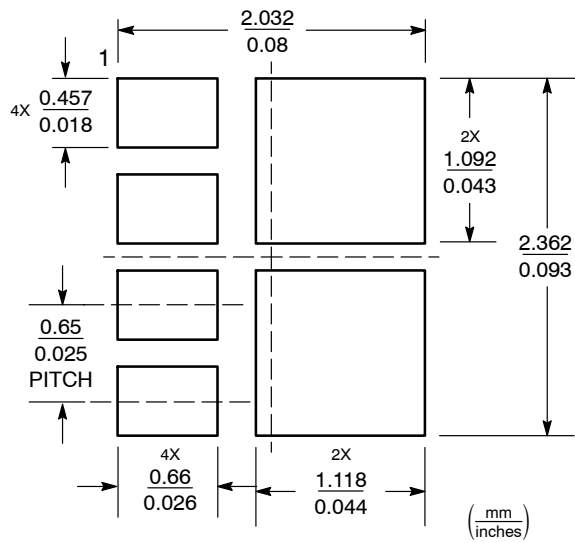
<b>DOCUMENT NUMBER:</b>	<b>98AON03078D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>ChipFET</b>	<b>PAGE 1 OF 2</b>

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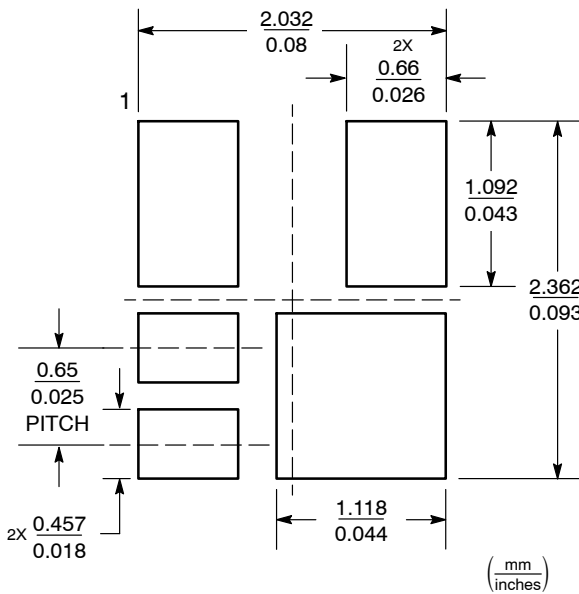
ADDITIONAL SOLDERING FOOTPRINTS\*



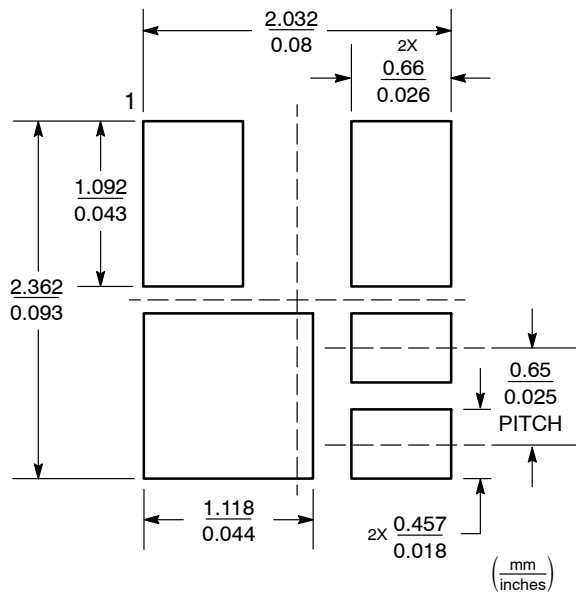
Styles 1 and 4



Style 2



Style 3



Style 5

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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