

# NTMD6N02R2

## MOSFET – Power, Dual, N-Channel Enhancement Mode, SO-8

6.0 A, 20 V



ON Semiconductor®

<http://onsemi.com>

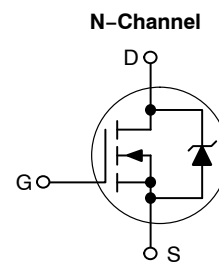
### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SOIC-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SOIC-8 Mounting Information Provided
- Pb-Free Package is Available

### Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery-Powered Products, for example, Computers, Printers, Cellular and Cordless Telephones and PCMCIA Cards

$V_{DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
20 V	35 m $\Omega$ @ $V_{GS} = 4.5$ V	6.0 A



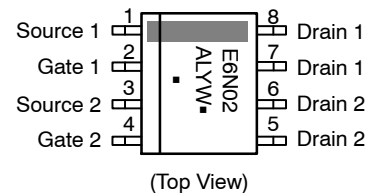
SOIC-8  
CASE 751  
STYLE 11

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	20	V
Drain-to-Gate Voltage ( $R_{GS} = 1.0$ M $\Omega$ )	$V_{DGR}$	20	V
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 12$	V
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	2.0	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	6.5	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	5.5	A
Pulsed Drain Current (Note 4)	$I_{DM}$	50	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	102	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.22	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	5.07	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	4.07	A
Pulsed Drain Current (Note 4)	$I_{DM}$	40	A
Thermal Resistance Junction-to-Ambient (Note 3)	$R_{\theta JA}$	172	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	0.73	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	3.92	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	3.14	A
Pulsed Drain Current (Note 4)	$I_{DM}$	30	A

1. Mounted onto a 2 in square FR-4 Board (1 in sq. 2 oz. Cu 0.06 in thick single sided),  $t < 10$  seconds.
2. Mounted onto a 2 in square FR-4 Board (1 in sq. 2 oz. Cu 0.06 in thick single sided),  $t =$  steady state.
3. Minimum FR-4 or G-10 PCB,  $t =$  steady state.
4. Pulse Test: Pulse Width = 10  $\mu\text{s}$ , Duty Cycle = 2%.

### MARKING DIAGRAM & PIN ASSIGNMENT



E6N02 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMD6N02R2	SOIC-8	2500/Tape & Reel
NTMD6N02R2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMD6N02R2

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 20\text{ Vdc}$ , $V_{GS} = 5.0\text{ Vdc}$ , Peak $I_L = 6.0\text{ Apk}$ , $L = 20\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	360	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	$T_L$	260	$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\ \mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	20 –	– 19.2	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$I_{DSS}$	– –	– –	1.0 10	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = +12\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	100	nAdc
Gate-Body Leakage Current ( $V_{GS} = -12\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	-100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{Adc}$ ) Temperature Coefficient (Negative)	$V_{GS(th)}$	0.6 –	0.9 -3.0	1.2 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-State Resistance ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ ) ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 4.0\text{ Adc}$ ) ( $V_{GS} = 2.7\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ ) ( $V_{GS} = 2.5\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )	$R_{DS(on)}$	– – – –	0.028 0.028 0.033 0.035	0.035 0.043 0.048 0.049	$\Omega$
Forward Transconductance ( $V_{DS} = 12\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )	$g_{FS}$	–	10	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 16\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	–	785	1100	pF
Output Capacitance		$C_{oss}$	–	260	450	
Reverse Transfer Capacitance		$C_{rss}$	–	75	180	

### SWITCHING CHARACTERISTICS (Notes 6 and 7)

Turn-On Delay Time	$(V_{DD} = 16\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	–	12	20	ns
Rise Time		$t_r$	–	50	90	
Turn-Off Delay Time		$t_{d(off)}$	–	45	75	
Fall Time		$t_f$	–	80	130	
Turn-On Delay Time	$(V_{DD} = 16\text{ Vdc}$ , $I_D = 4.0\text{ Adc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	–	11	18	ns
Rise Time		$t_r$	–	35	65	
Turn-Off Delay Time		$t_{d(off)}$	–	45	75	
Fall Time		$t_f$	–	60	110	
Total Gate Charge	$(V_{DS} = 16\text{ Vdc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ )	$Q_{tot}$	–	12	20	nC
Gate-Source Charge		$Q_{gs}$	–	1.5	–	
Gate-Drain Charge		$Q_{gd}$	–	4.0	–	

5. Handling precautions to protect against electrostatic discharge is mandatory

6. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

# NTMD6N02R2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (continued) (Note 8)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>BODY-DRAIN DIODE RATINGS (Note 9)</b>						
Diode Forward On-Voltage	$V_{SD}$	-	$(I_S = 4.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$	0.83	Vdc	
			$(I_S = 6.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$	0.88		
			$(I_S = 6.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^\circ\text{C})$	0.75		
Reverse Recovery Time	$t_{rr}$	-	$(I_S = 6.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, dI_S/dt = 100 \text{ A}/\mu\text{s})$	30	ns	
				$t_a$		15
				$t_b$		15
Reverse Recovery Stored Charge	$Q_{RR}$	-	0.02	-	$\mu\text{C}$	

8. Handling precautions to protect against electrostatic discharge is mandatory.

9. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.

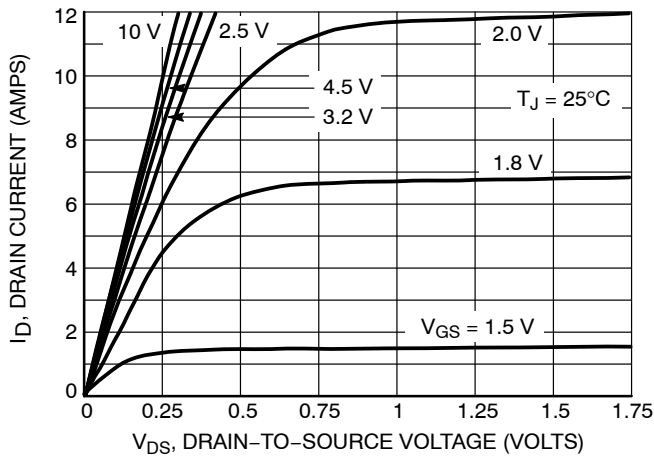


Figure 1. On-Region Characteristics

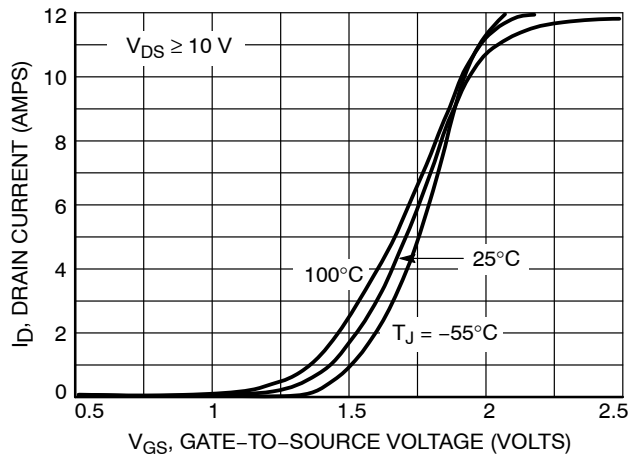


Figure 2. Transfer Characteristics

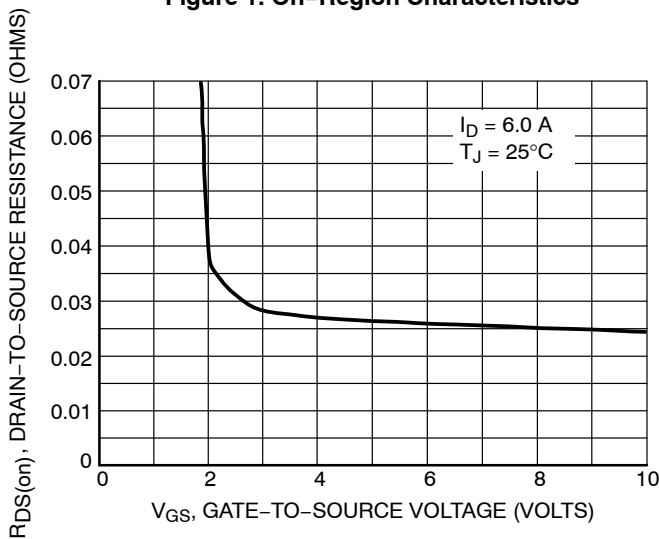


Figure 3. On-Resistance versus Gate-to-Source Voltage

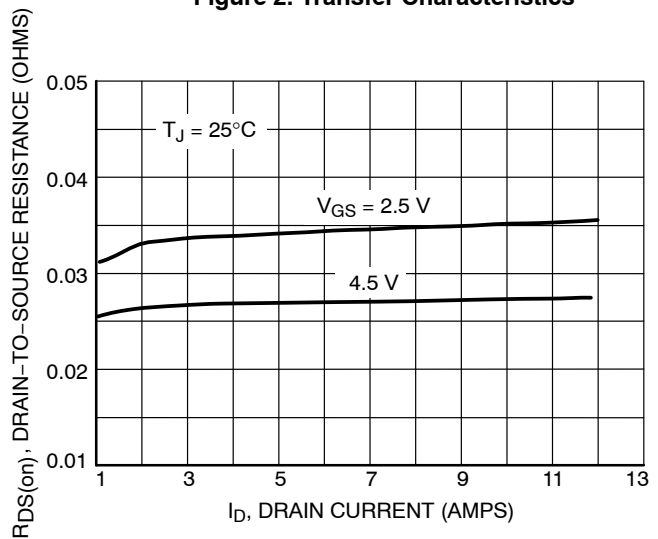
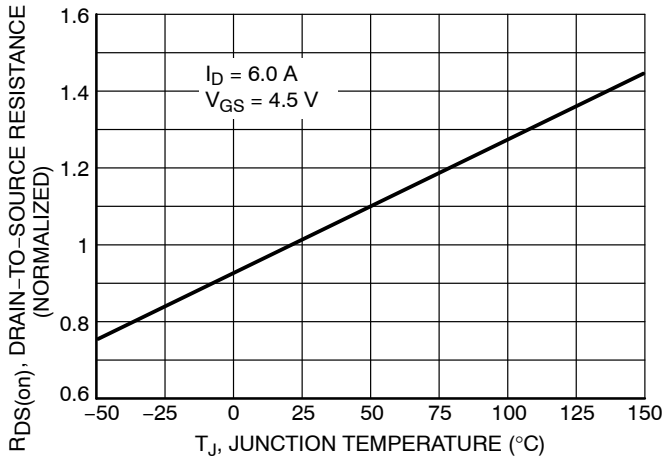
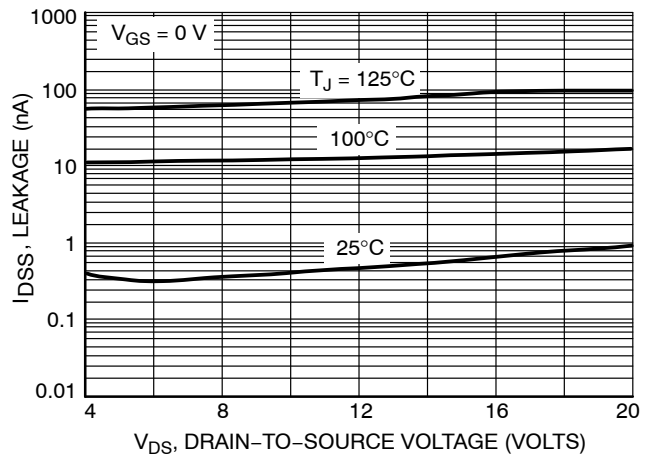


Figure 4. On-Resistance versus Drain Current and Gate Voltage

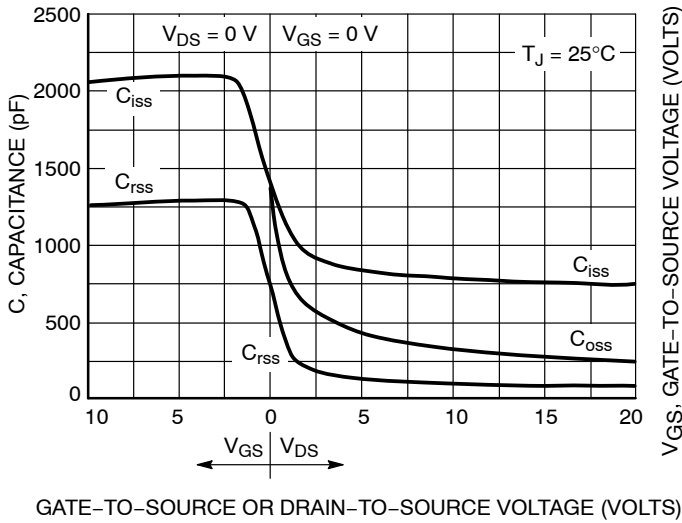
# NTMD6N02R2



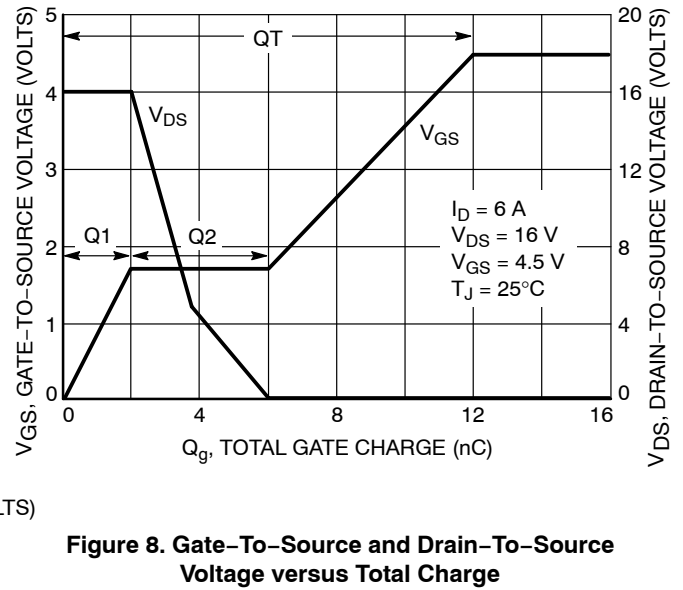
**Figure 5. On-Resistance Variation with Temperature**



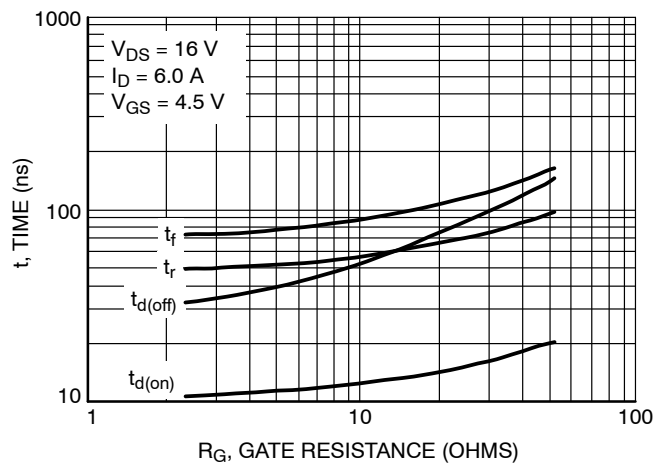
**Figure 6. Drain-To-Source Leakage Current versus Voltage**



**Figure 7. Capacitance Variation**



**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

# NTMD6N02R2

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

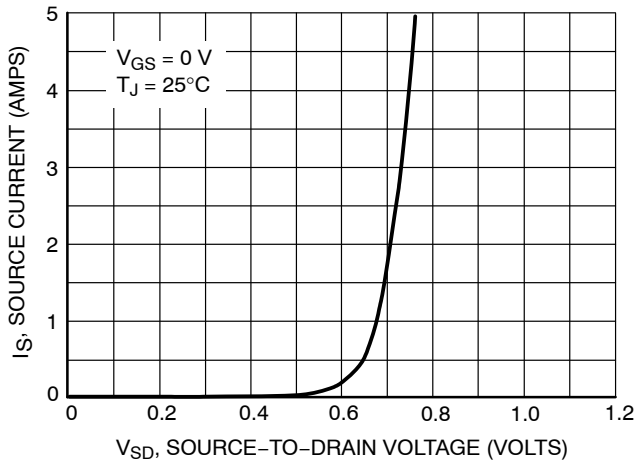


Figure 10. Diode Forward Voltage versus Current

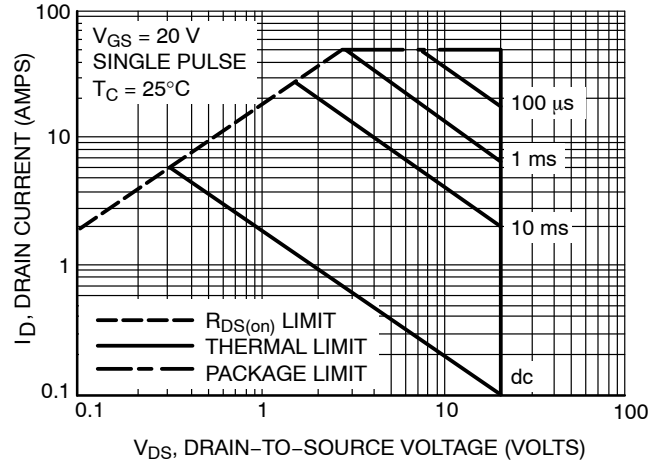


Figure 11. Maximum Rated Forward Biased Safe Operating Area

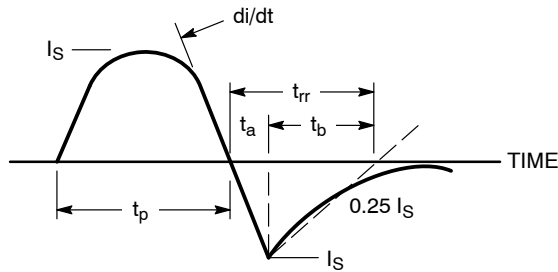


Figure 12. Diode Reverse Recovery Waveform

## TYPICAL ELECTRICAL CHARACTERISTICS

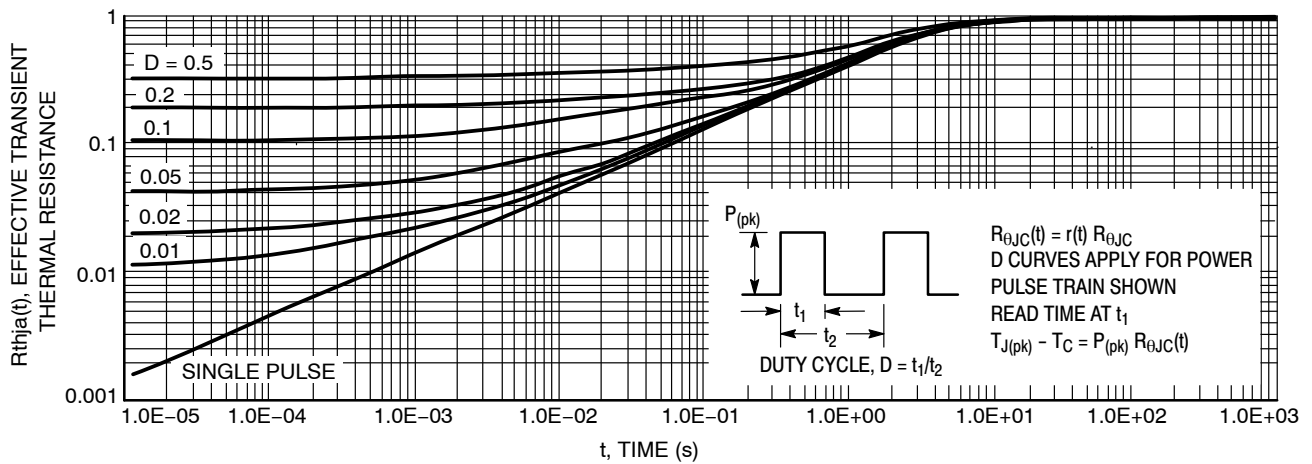


Figure 13. Thermal Response

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

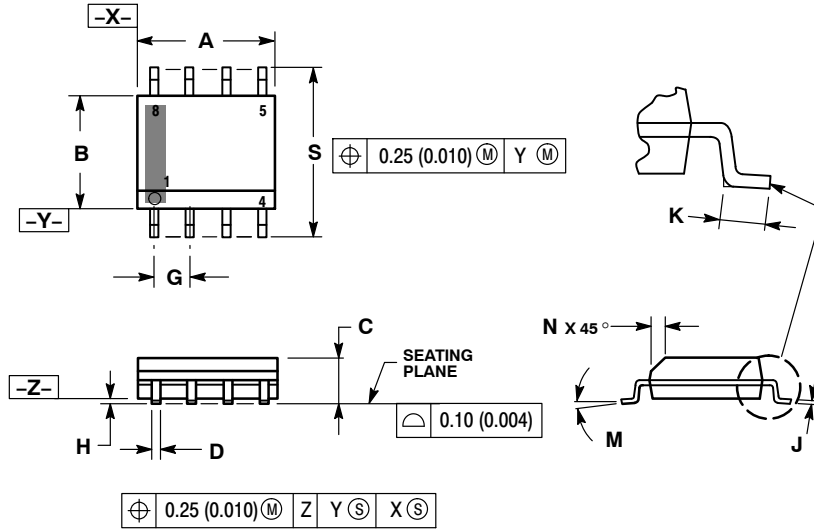
ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

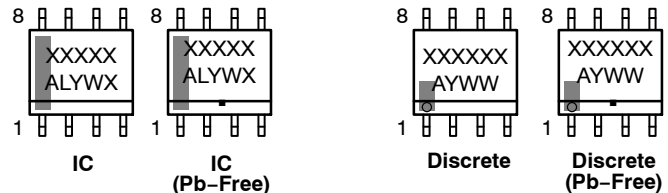
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2


ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p><b>STYLE 2:</b><br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p><b>STYLE 6:</b><br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p><b>STYLE 7:</b><br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p><b>STYLE 11:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p><b>STYLE 14:</b><br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p><b>STYLE 18:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p><b>STYLE 19:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p><b>STYLE 26:</b><br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p><b>STYLE 27:</b><br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p><b>STYLE 28:</b><br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p><b>STYLE 29:</b><br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |   |   |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative