

# NTTFS4824N

## MOSFET – Power, Single, N-Channel, $\mu$ 8FL 30 V, 69 A

### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- DC-DC Converters
- Low Side Switching

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	14.9	A
		$T_A = 85^\circ\text{C}$	10.8	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	2.2	W	
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	20.6	A
		$T_A = 85^\circ\text{C}$	14.9	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	$P_D$	4.1	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_C = 25^\circ\text{C}$	8.3	A
		$T_C = 85^\circ\text{C}$	6.0	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	0.66	W	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	69	A
		$T_C = 85^\circ\text{C}$	50	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	46.3	W	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	207	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	46.3	A	
Drain to Source dV/dt	dV/dt	6.0	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 38$ A <sub>pk</sub> , $L = 0.1$ mH, $R_G = 25 \Omega$ )	$E_{AS}$	72	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

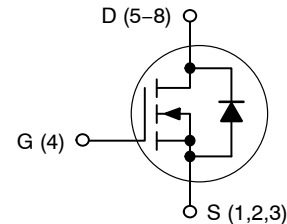


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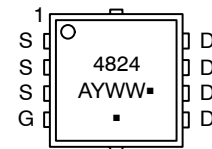
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	5.0 m $\Omega$ @ 10 V	69 A
	7.5 m $\Omega$ @ 4.5 V	

### N-Channel MOSFET



**WDFN8**  
( $\mu$ 8FL)  
CASE 511AB  
FLAT LEAD

### MARKING DIAGRAM



4824 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTTFS4824NTAG	WDFN8 (Pb-Free)	1500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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2. Surface-mounted on FR4 board using the minimum recommended pad size.

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.7	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	57.7	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	187.8	
Junction-to-Ambient – ( $t \leq 10$ s) (Note 3)	$R_{\theta JA}$	30.3	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu\text{A}$	30			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$			1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$			10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V				$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250$ $\mu\text{A}$	1.5	1.9	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V to 11.5 V	$I_D = 20$ A		3.7	5.0	m $\Omega$
			$I_D = 10$ A		3.6		
		$V_{GS} = 4.5$ V	$I_D = 20$ A		5.8	7.5	
			$I_D = 10$ A		5.7		
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5$ V, $I_D = 20$ A		53		S	

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = 12$ V		1750	2363	pF
Output Capacitance	$C_{oss}$			350	473	
Reverse Transfer Capacitance	$C_{rss}$			170	255	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V, $I_D = 20$ A		12.6	18	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.7		
Gate-to-Source Charge	$Q_{GS}$			4.7		
Gate-to-Drain Charge	$Q_{GD}$			4.8		
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 11.5$ V, $V_{DS} = 15$ V, $I_D = 20$ A		29	

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V, $I_D = 15$ A, $R_G = 3.0$ $\Omega$		13		ns
Rise Time	$t_r$			38		
Turn-Off Delay Time	$t_{d(off)}$			18		
Fall Time	$t_f$			5.5		

5. Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

# NTTFS4824N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.0		ns
Rise Time	$t_r$			21		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall Time	$t_f$			4.4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 20\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
			$T_J = 125^\circ\text{C}$		0.7		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V},$ $dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 20\text{ A}$		22		ns	
Charge Time	$t_a$			10.5			
Discharge Time	$t_b$			11.5			
Reverse Recovery Charge	$Q_{RR}$			10		nC	

### PACKAGE PARASITIC VALUES

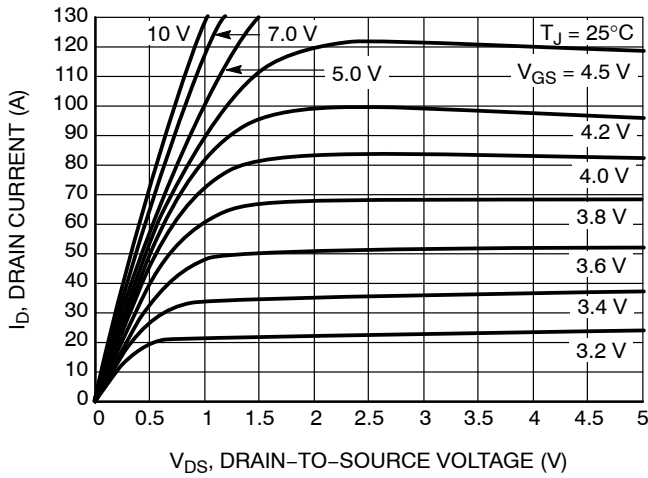
Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.38		nH
Drain Inductance	$L_D$			0.054		
Gate Inductance	$L_G$			1.3		
Gate Resistance	$R_G$			0.9	2.0	$\Omega$

5. Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .

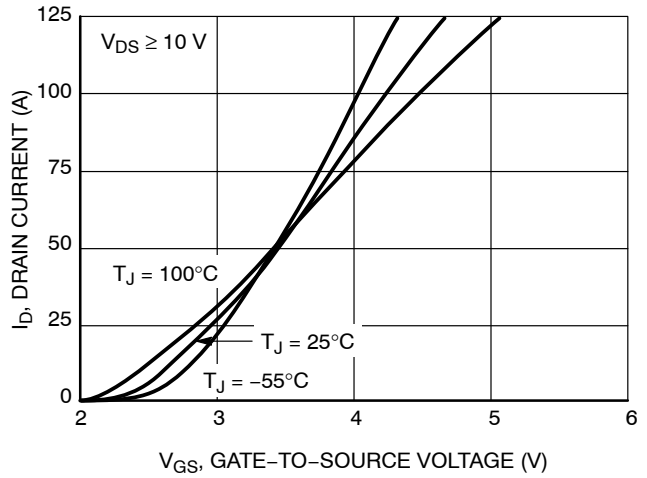
6. Switching characteristics are independent of operating junction temperatures.

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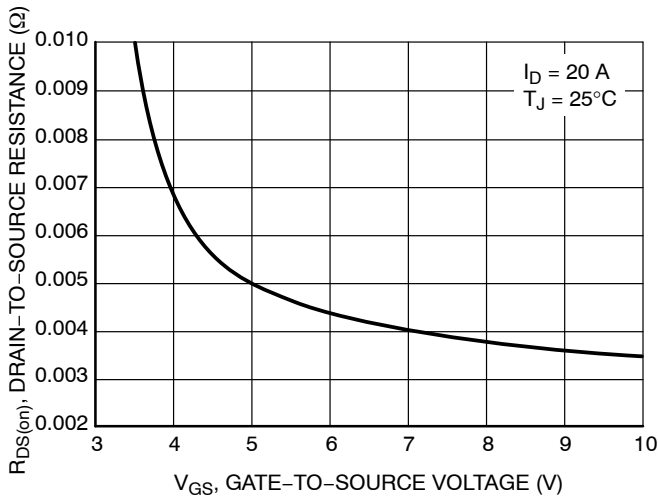
## TYPICAL CHARACTERISTICS



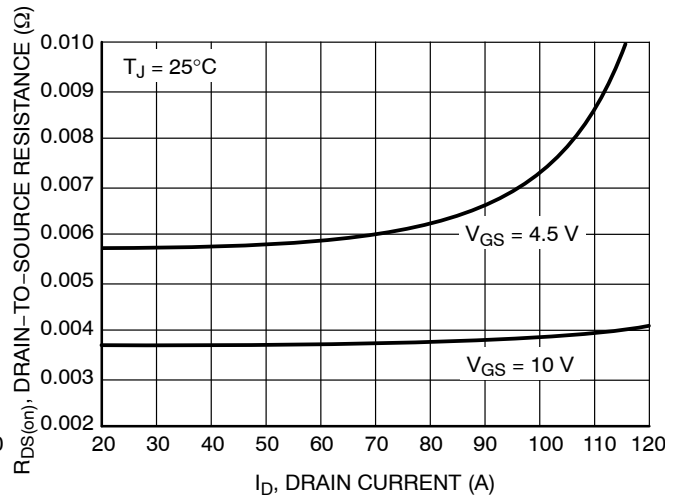
**Figure 1. On-Region Characteristics**



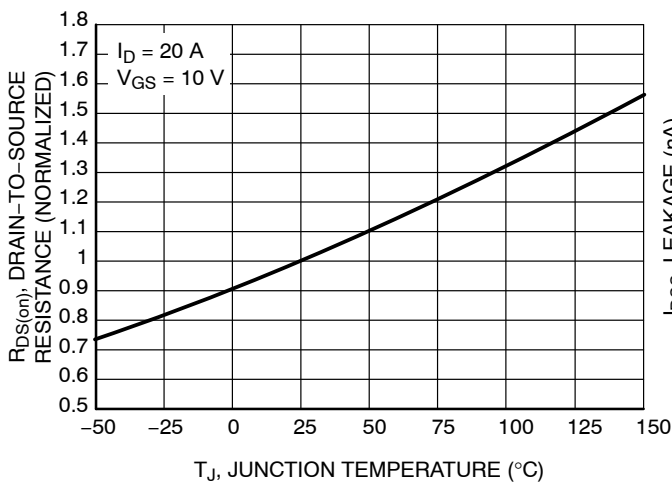
**Figure 2. Transfer Characteristics**



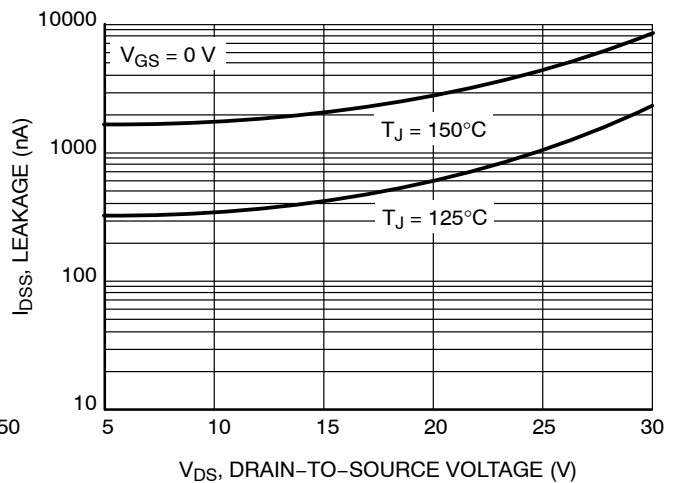
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

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## TYPICAL CHARACTERISTICS

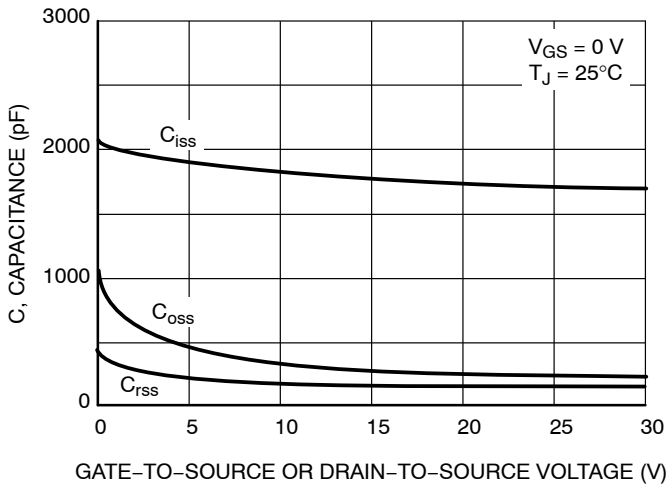


Figure 7. Capacitance Variation

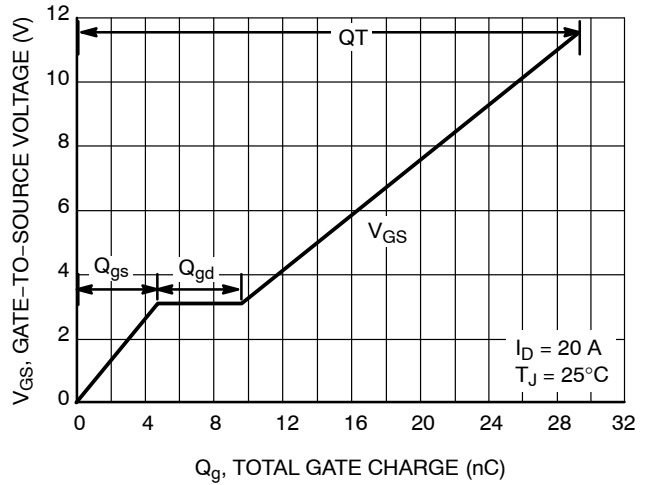


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

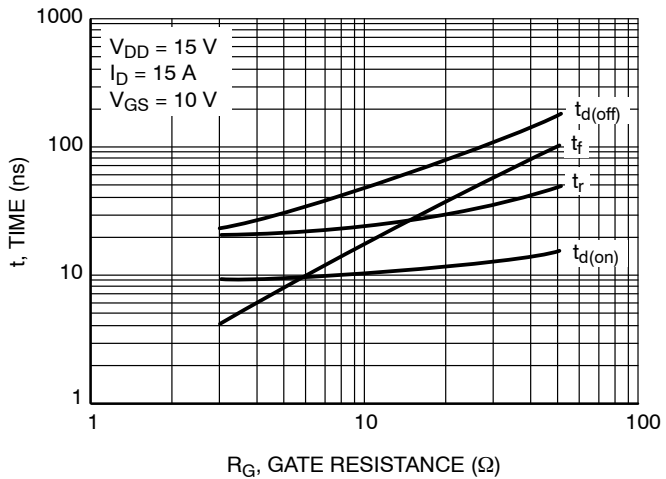


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

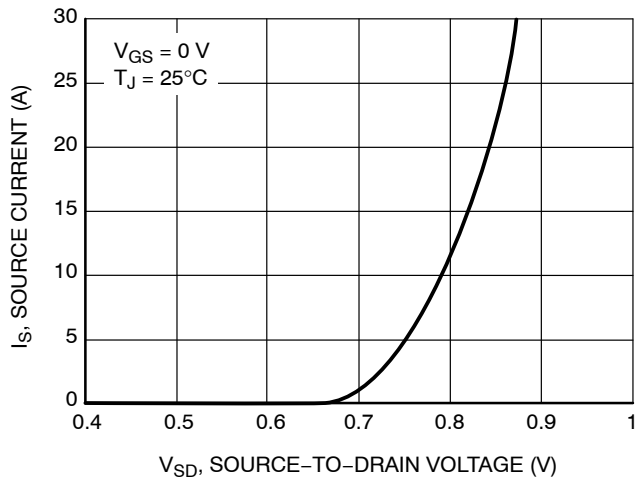


Figure 10. Diode Forward Voltage vs. Current

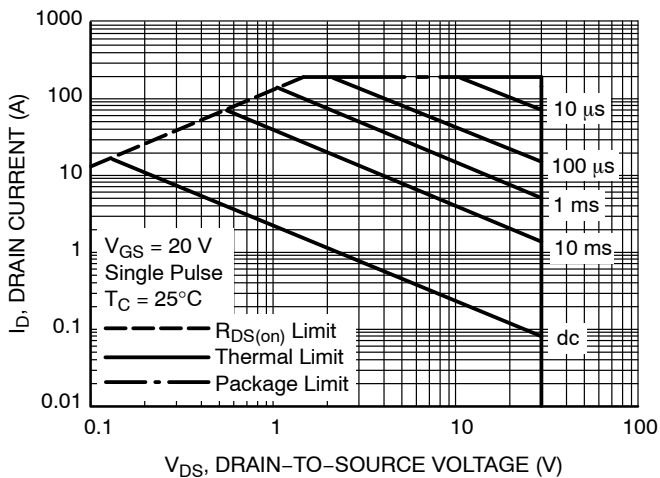


Figure 11. Maximum Rated Forward Biased Safe Operating Area

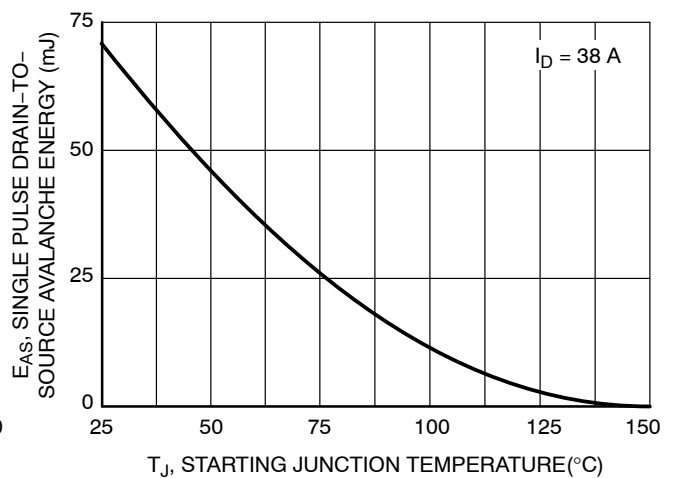


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

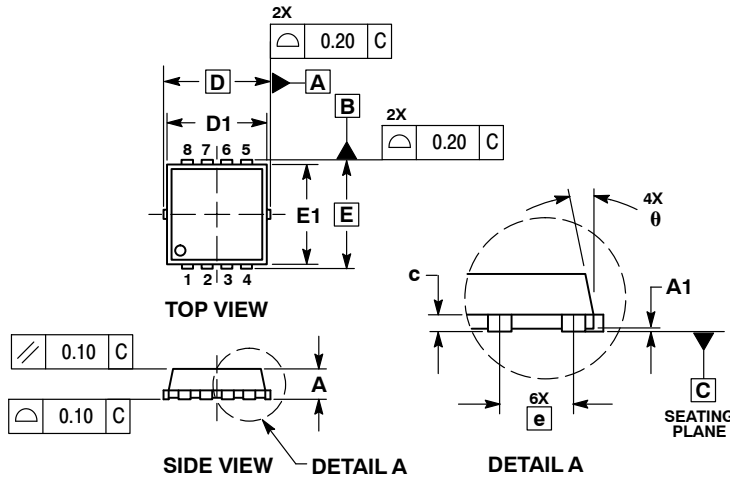
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SCALE 2:1

### WDFN8 3.3x3.3, 0.65P CASE 511AB ISSUE D

DATE 23 APR 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°

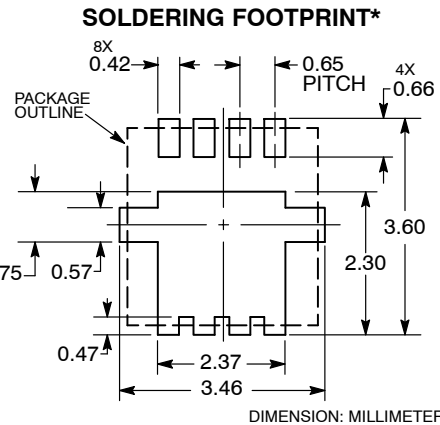


#### GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>WDFN8 3.3X3.3, 0.65P</b>	<b>PAGE 1 OF 1</b>

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