

# NTNS3A91PZ

## MOSFET – Single, P-Channel, Small Signal, XLLGA3, 0.62 x 0.62 x 0.4 mm -20 V, -223 mA



ON Semiconductor®

<http://onsemi.com>

### Features

- Single P-Channel MOSFET
- Ultra Small and Thin Package (0.62 x 0.62 x 0.4 mm)
- Low  $R_{DS(on)}$  Solution in 0.62 x 0.62 mm Package
- 1.5 V Gate Voltage Rating
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Small Signal Load Switch
- Analog Switch
- High Speed Interfacing
- Optimized for Power Management in Ultra Portable Products

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		$V_{DSS}$	-20	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 8.0$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	-223	mA
				$T_A = 85^\circ\text{C}$	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	-240		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	121	mW
				$t \leq 5$ s	
Pulsed Drain Current		$t_p = 10 \mu\text{s}$	$I_{DM}$	-669	mA
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150		$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	-121		mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260		$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

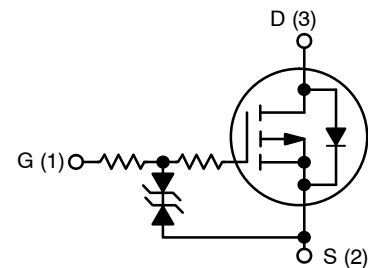
### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	1035	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5$ s (Note 1)	$R_{\theta JA}$	895	

1. Surface Mounted on FR4 Board using the minimum recommended pad size, (or 2 mm<sup>2</sup>), 1 oz Cu.

MOSFET		
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-20 V	1.6 $\Omega$ @ -4.5 V	-223 mA
	2.4 $\Omega$ @ -2.5 V	
	3.3 $\Omega$ @ -1.8 V	
	4.5 $\Omega$ @ -1.5 V	

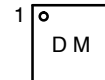
### P-Channel MOSFET



### MARKING DIAGRAM



XLLGA3  
CASE 713AB



D = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTNS3A91PZT5G	XLLGA3 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTNS3A91PZ

2. Pulse Test: pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250 \mu\text{A}$ , ref to $25^\circ\text{C}$		11		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0 \text{ V}, V_{DS} = -20 \text{ V}$			-1.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8.0 \text{ V}$			$\pm 2.0$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.1		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -100 \text{ mA}$		1.1	1.6	$\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -50 \text{ mA}$		1.5	2.4	
		$V_{GS} = -1.8 \text{ V}, I_D = -20 \text{ mA}$		2.0	3.3	
		$V_{GS} = -1.5 \text{ V}, I_D = -10 \text{ mA}$		2.5	4.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5 \text{ V}, I_D = -100 \text{ mA}$		0.41		S
Source-Drain Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_S = -10 \text{ mA}$		-0.6	-1.0	V

### CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0 \text{ V}, f = 10 \text{ kHz}, V_{DS} = -15 \text{ V}$		41		pF
Output Capacitance	$C_{OSS}$			4.6		
Reverse Transfer Capacitance	$C_{RSS}$			4.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5 \text{ V}, V_{DS} = -15 \text{ V}, I_D = -200 \text{ mA}$		1.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	$Q_{GS}$			0.2		
Gate-to-Drain Charge	$Q_{GD}$			0.23		

### SWITCHING CHARACTERISTICS, $V_{GS} = 4.5 \text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5 \text{ V}, V_{DD} = -15 \text{ V}, I_D = -200 \text{ mA}, R_G = 2 \Omega$		41		ns
Rise Time	$t_r$			97		
Turn-Off Delay Time	$t_{d(OFF)}$			571		
Fall Time	$t_f$			286		

3. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL CHARACTERISTICS

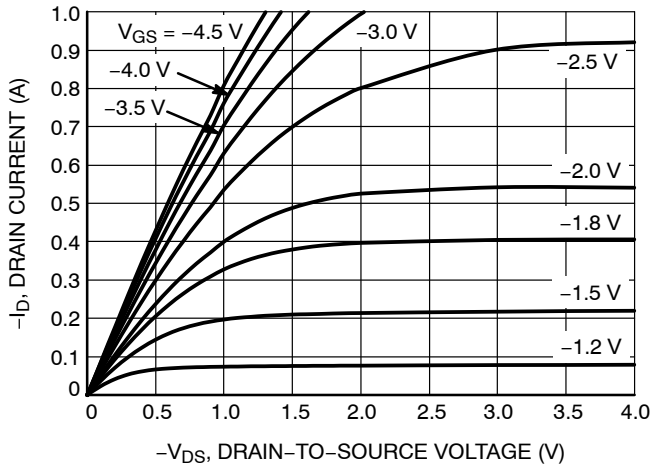


Figure 1. On-Region Characteristics

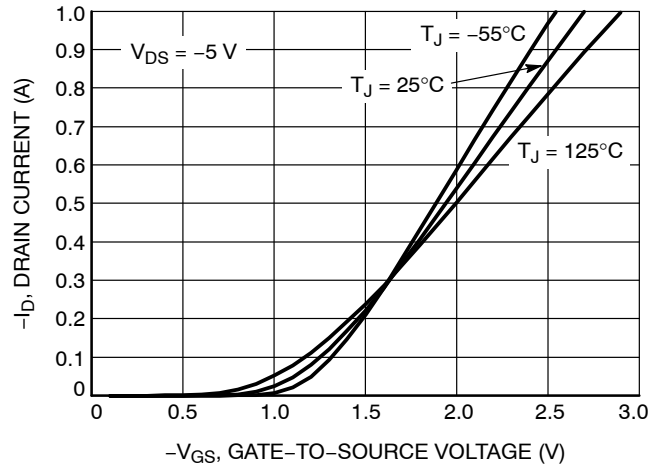


Figure 2. Transfer Characteristics

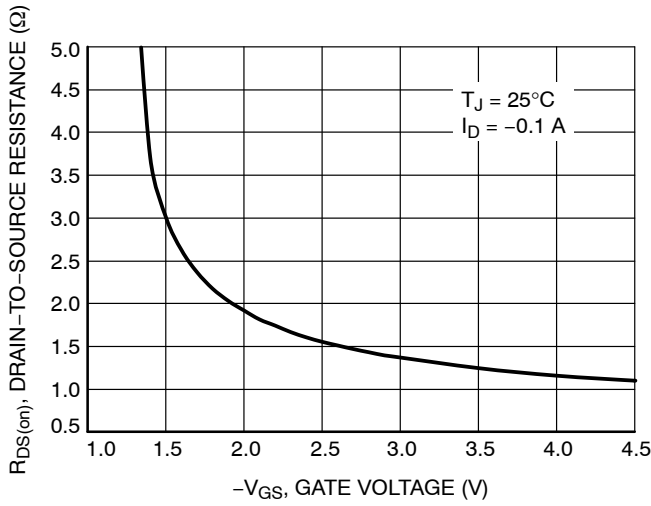


Figure 3. On-Resistance vs. Gate-to-Source Voltage

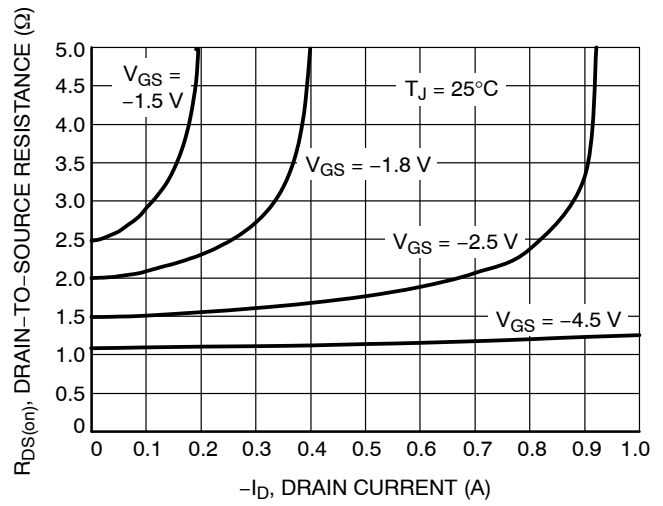


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

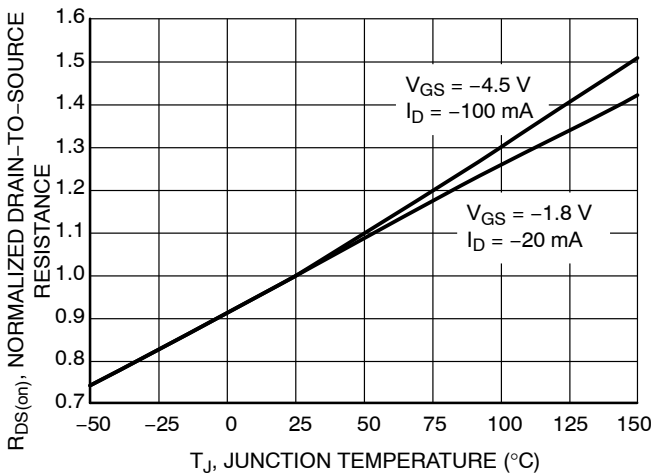


Figure 5. On Resistance Variation with Temperature

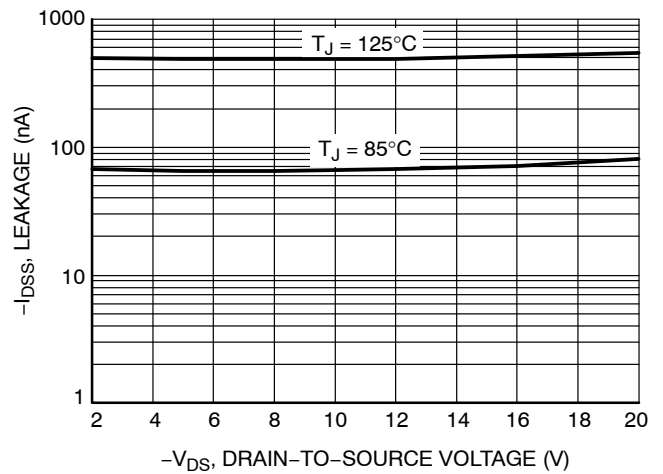


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

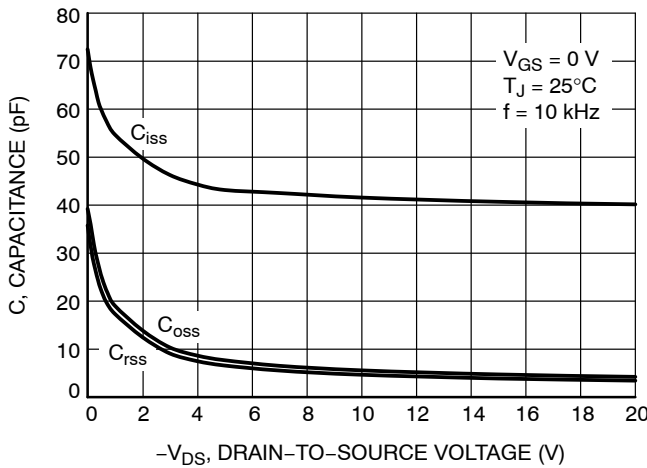


Figure 7. Capacitance Variation

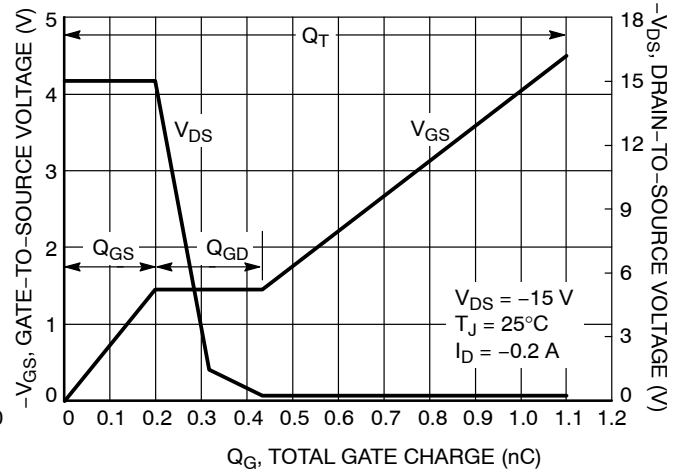


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

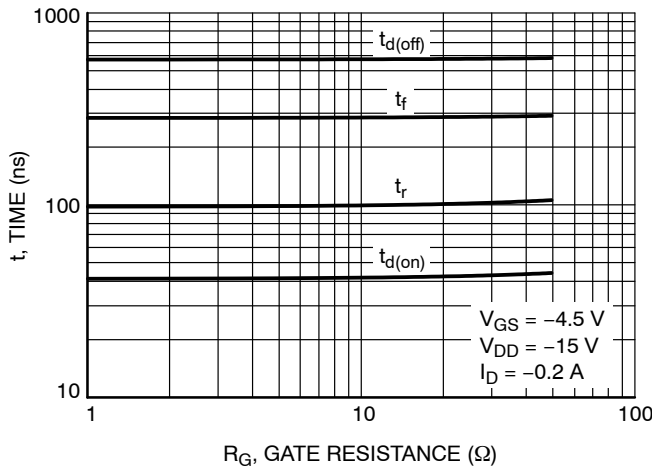


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

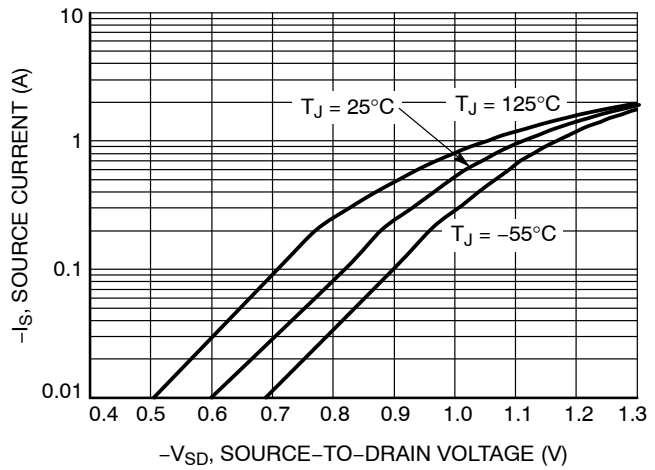


Figure 10. Diode Forward Voltage vs. Current

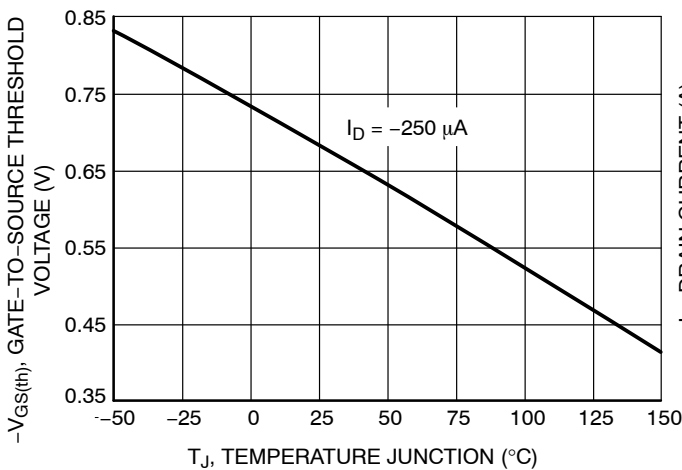


Figure 11. Threshold Voltage

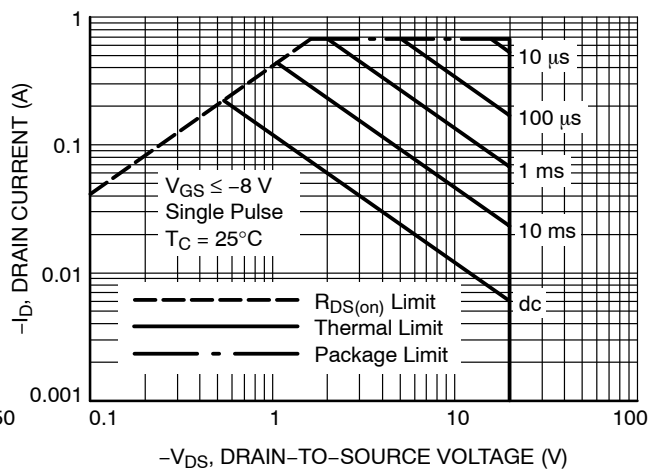


Figure 12. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL CHARACTERISTICS

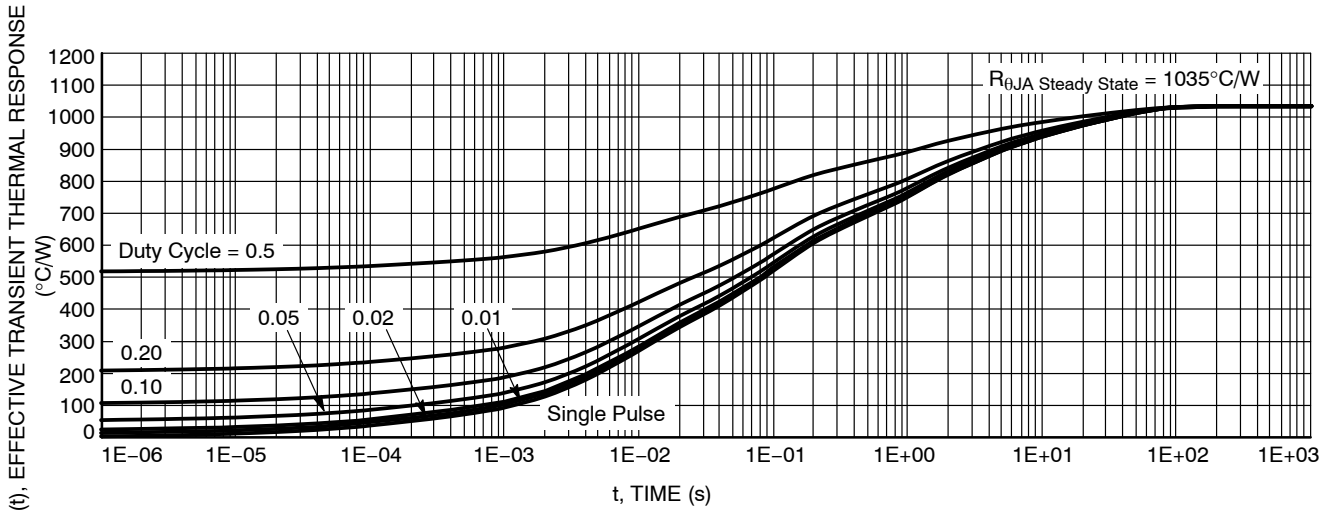
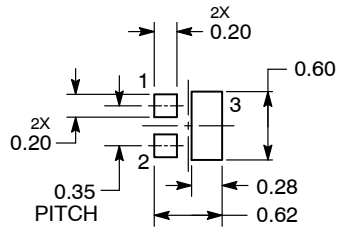


Figure 13. FET Thermal Response

### MINIMUM RECOMMENDED SOLDER FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*Dependent upon end user capabilities, this footprint could be used as a minimum.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

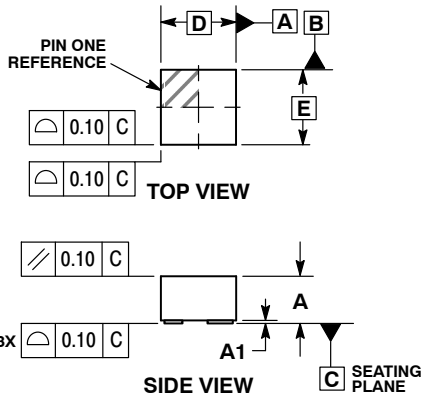
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SCALE 8:1

**XLLGA3, 0.62x0.62, 0.35P**  
**CASE 713AB**  
**ISSUE O**

DATE 25 SEP 2012



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

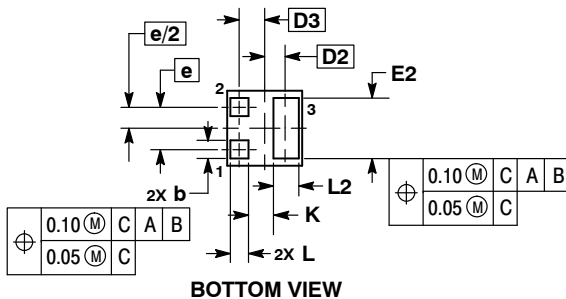
MILLIMETERS		
DIM	MIN	MAX
A	0.340	0.440
A1	0.000	0.030
b	0.100	0.200
D	0.620 BSC	
D2	0.175 BSC	
D3	0.205 BSC	
E	0.620 BSC	
E2	0.400	0.600
e	0.350 BSC	
K	0.200 REF	
L	0.090	0.210
L2	0.110	0.310

**GENERIC MARKING DIAGRAM\***

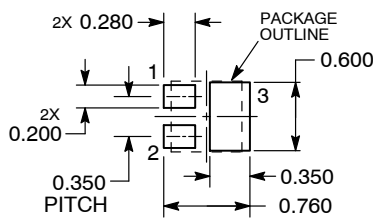


- X = Specific Device Code
- M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.



**RECOMMENDED SOLDER FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>XLLGA3, 0.62X0.62, 0.35P</b>	<b>PAGE 1 OF 1</b>

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