

NTHS4501N

Power MOSFET

30 V, 6.7 A, Single N-Channel, ChipFET™ Package

Features

- Planar Technology Device Offers Low $R_{DS(on)}$ and Fast Switching Speed in a ChipFET Package
- Leadless ChipFET Package has 40% Smaller Footprint than TSOP-6. Ideal Device for Applications Where Board Space is at a Premium.
- ChipFET Package Exhibits Excellent Thermal Capabilities Where Heat Transfer is Required.
- Pb-Free Package is Available

Applications

- Buck and Boost Converters
- Optimized for Battery and Load Management Applications in Portable Equipment such as Notebook Computers, MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistants and Other Portable Applications
- Charge Control in Battery Chargers

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | | Symbol | Value | Unit |
|---|------------------------|--------------------------|------------|------------------|
| Drain-to-Source Voltage | | V_{DSS} | 30 | V |
| Gate-to-Source Voltage | | V_{GS} | ± 20 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A = 25^\circ\text{C}$ | 4.9 | A |
| | | $T_A = 85^\circ\text{C}$ | 3.5 | |
| | $t \leq 5 \text{ s}$ | $T_A = 25^\circ\text{C}$ | 6.7 | |
| Power Dissipation (Note 1) | Steady State | $T_A = 25^\circ\text{C}$ | 1.3 | W |
| | | $T_A = 85^\circ\text{C}$ | 0.7 | |
| | $t \leq 5 \text{ s}$ | $T_A = 25^\circ\text{C}$ | 2.5 | |
| Pulsed Drain Current | $t_p = 10 \mu\text{s}$ | I_{DM} | 20 | A |
| Operating Junction and Storage Temperature | | T_J, T_{STG} | -55 to 150 | $^\circ\text{C}$ |
| Source Current (Body Diode) | | I_S | 1.1 | A |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | T_L | 260 | $^\circ\text{C}$ |

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|-----------------|-----|---------------------------|
| Junction-to-Ambient - Steady State (Note 1) | $R_{\theta JA}$ | 95 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Foot (Drain) Steady State (Note 1) | $R_{\theta JF}$ | 20 | |
| Junction-to-Ambient - $t \leq 5 \text{ s}$ (Note 1) | $R_{\theta JA}$ | 50 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

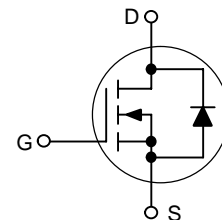
1. Surface Mounted on FR4 Board using 1 in sq. pad size (Cu area = 1.127 in sq [1 oz] including traces).



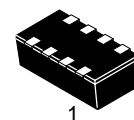
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| $V_{(BR)DSS}$ | $R_{DS(on)}$ Typ | I_D Max |
|---------------|-----------------------|-----------|
| 30 V | 30 m Ω @ 10 V | 6.7 A |
| | 40 m Ω @ 4.5 V | |

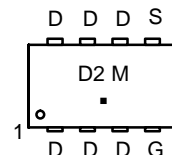


N-Channel MOSFET



ChipFET
CASE 1206A
STYLE 1

MARKING DIAGRAM AND PIN ASSIGNMENT



- D2 = Specific Device Code
- M = Month Code
- = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-------------------|------------------|
| NTHS4501NT1 | ChipFET | 3000/Tape & Reel |
| NTHS4501NT1G | ChipFET (Pb-Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTHS4501N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|--------------------------------------|--|------------------------|-----|-----|-------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 30 | 31 | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 30 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 24 V | T _J = 25°C | | 1.0 | μA |
| | | | T _J = 125°C | | 10 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 2)

| | | | | | | |
|--|-------------------------------------|---|-----|-----|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 250 μA | 1.0 | 1.6 | 2.0 | V |
| Negative Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | 4.0 | | mV/°C |
| Drain-to-Source On-Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 4.9 A | | 30 | 38 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 3.9 A | | 40 | 50 | |
| Forward Transconductance | g _{FS} | V _{DS} = 10 V, I _D = 4.9 A | | 15 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|---|--|-----|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V | | 462 | | pF |
| Output Capacitance | C _{OSS} | | | 137 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 32 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 15 V, I _D = 4.9 A | | 9.1 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 0.7 | | |
| Gate-to-Source Charge | Q _{GS} | | | 1.3 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 1.8 | | |

SWITCHING CHARACTERISTICS (Note 3)

| | | | | | | |
|---------------------|---------------------|---|--|-----|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 10 V, V _{DS} = 15 V, I _D = 1.0 A, R _G = 6.0 Ω | | 4.0 | | ns |
| Rise Time | t _r | | | 11 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 17 | | |
| Fall Time | t _f | | | 7.5 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|-------------------------|-----------------|---|-----------------------|------|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 1.1 A | T _J = 25°C | 0.75 | 1.2 | V |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, I _S = 1.1 A, dI _S /dt = 90 A/μs | | 19.1 | | ns |
| Charge Time | t _a | | | 11.9 | | |
| Discharge Time | t _b | | | 7.3 | | |
| Reverse Recovery Charge | Q _{RR} | | | 13 | | nC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

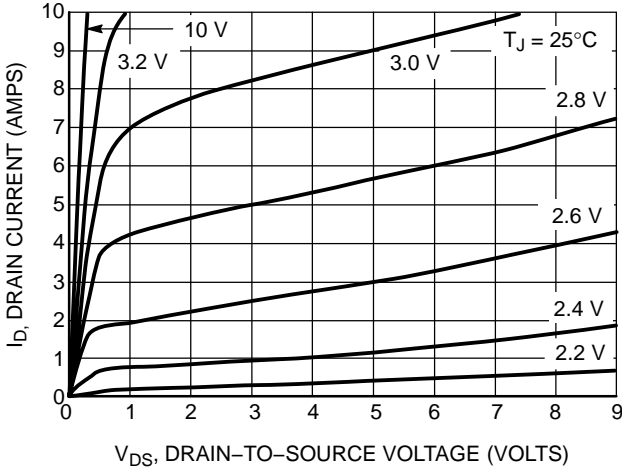


Figure 1. On-Region Characteristics

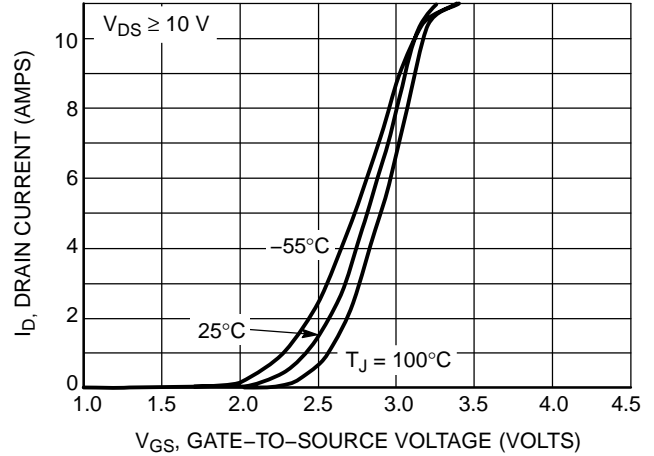


Figure 2. Transfer Characteristics

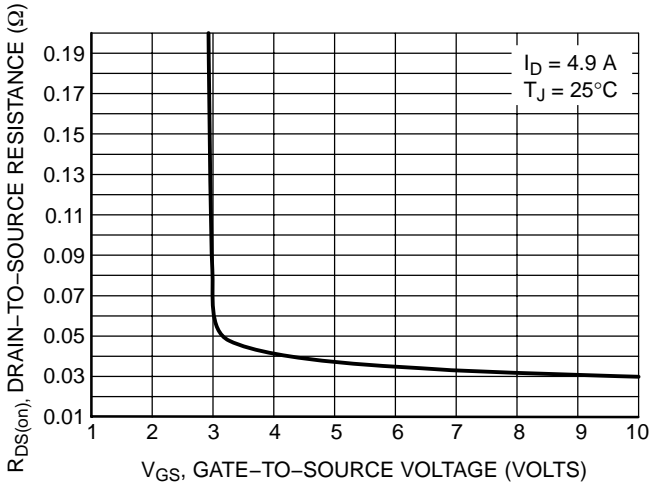


Figure 3. On-Resistance vs. Gate-to-Source Voltage

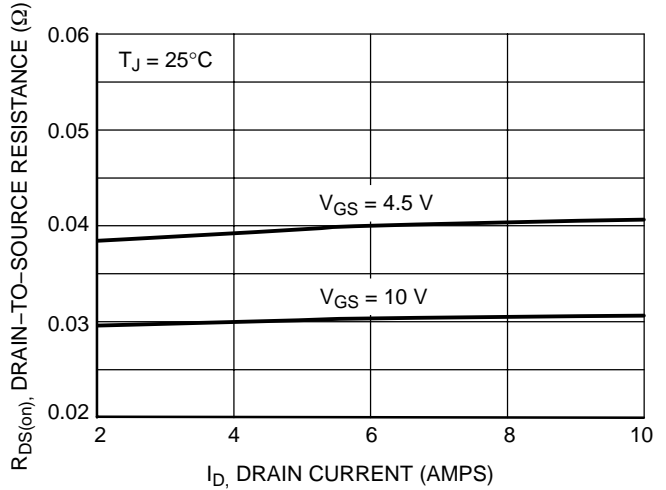


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

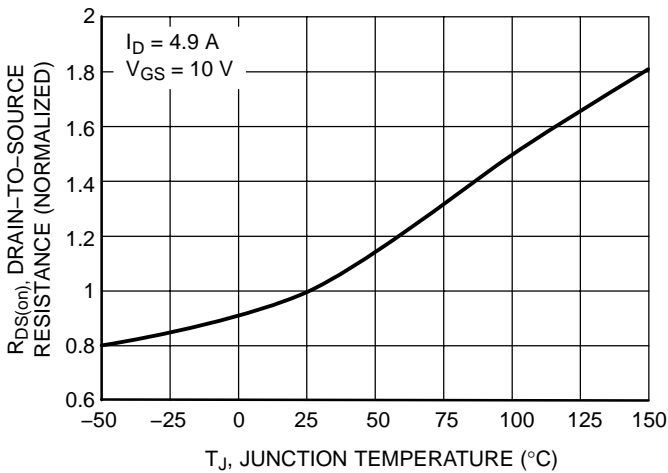


Figure 5. On-Resistance Variation with Temperature

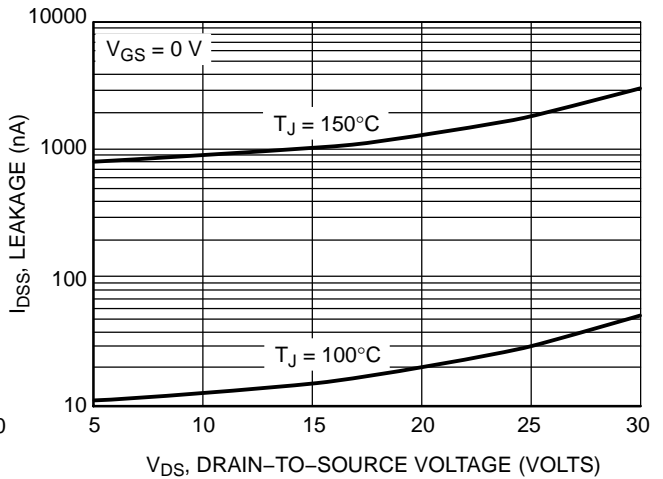


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

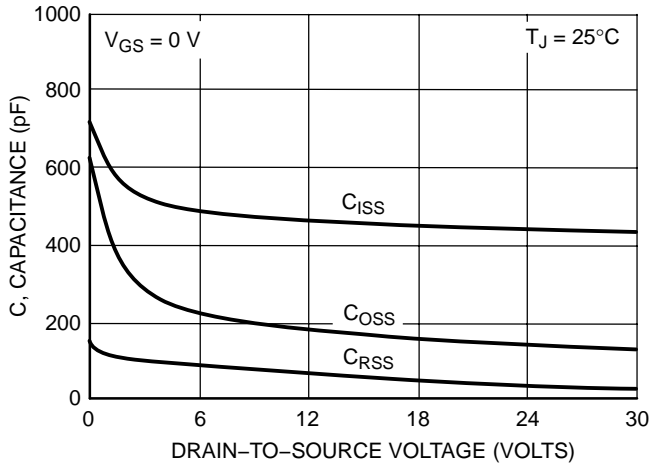


Figure 7. Capacitance Variation

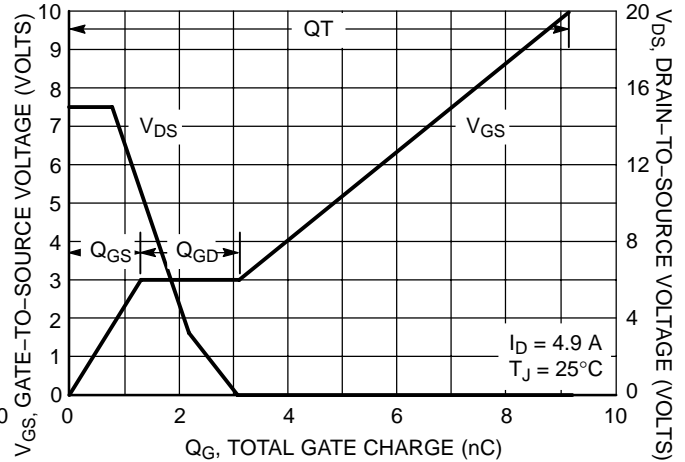


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

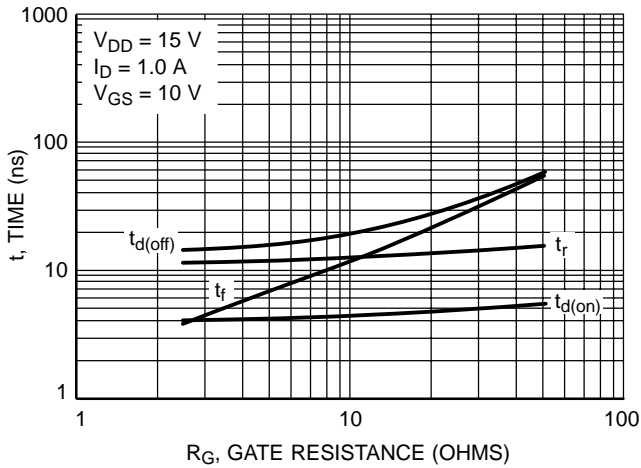


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

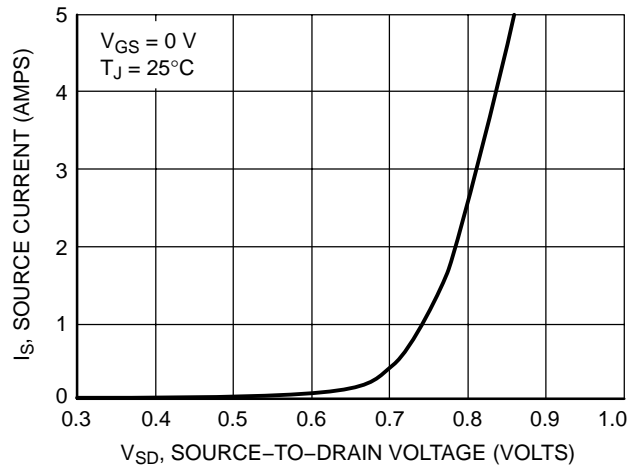


Figure 10. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE

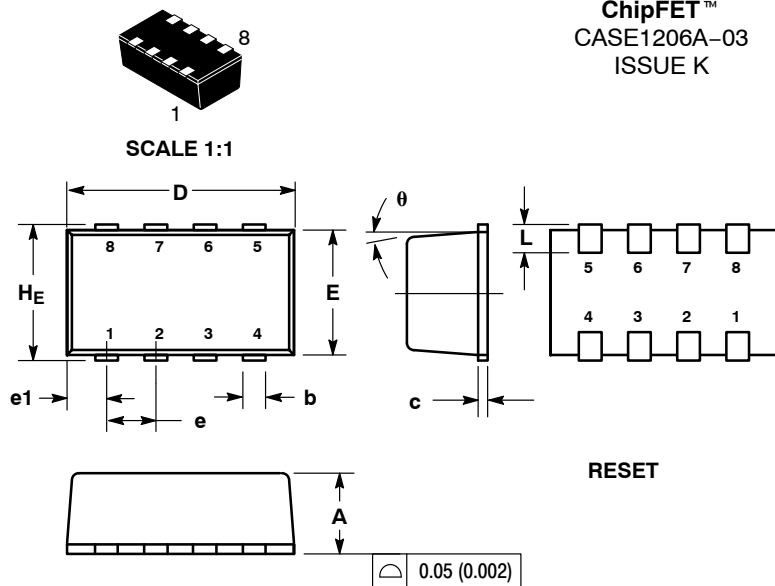
PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™ CASE1206A-03 ISSUE K

DATE 19 MAY 2009

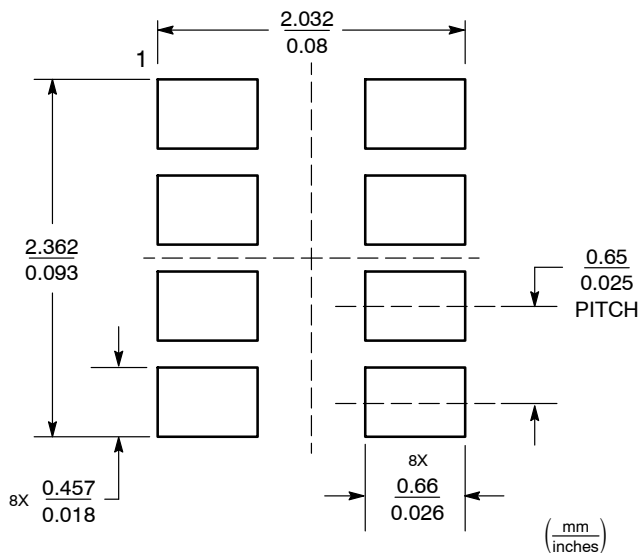


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
 4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
 5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
 6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.00 | 1.05 | 1.10 | 0.039 | 0.041 | 0.043 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 2.95 | 3.05 | 3.10 | 0.116 | 0.120 | 0.122 |
| E | 1.55 | 1.65 | 1.70 | 0.061 | 0.065 | 0.067 |
| e | 0.65 BSC | | | 0.025 BSC | | |
| e1 | 0.55 BSC | | | 0.022 BSC | | |
| L | 0.28 | 0.35 | 0.42 | 0.011 | 0.014 | 0.017 |
| HE | 1.80 | 1.90 | 2.00 | 0.071 | 0.075 | 0.079 |
| θ | 5° NOM | | | 5° NOM | | |

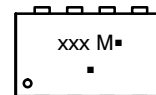
- | | | | | | |
|---|---|---|--|---|---|
| <p>STYLE 1: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 2: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 3: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. COLLECTOR 4. BASE 5. EMITTER 6. COLLECTOR 7. COLLECTOR 8. COLLECTOR</p> | <p>STYLE 5: PIN 1. ANODE 2. ANODE 3. DRAIN 4. DRAIN 5. SOURCE 6. GATE 7. CATHODE 8. CATHODE</p> | <p>STYLE 6: PIN 1. ANODE 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. CATHODE / DRAIN</p> |
|---|---|---|--|---|---|

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
 - M = Month Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

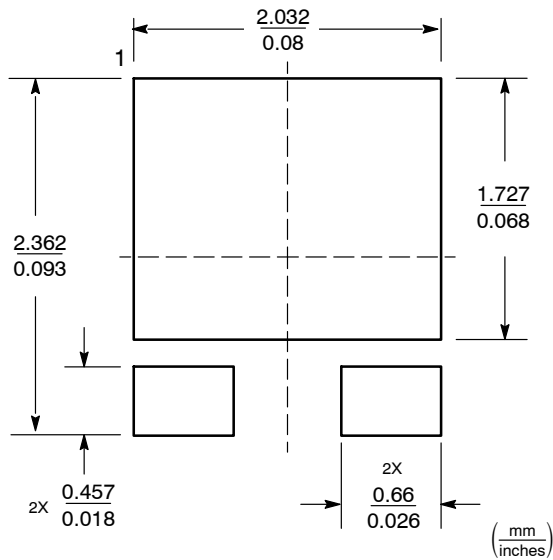
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

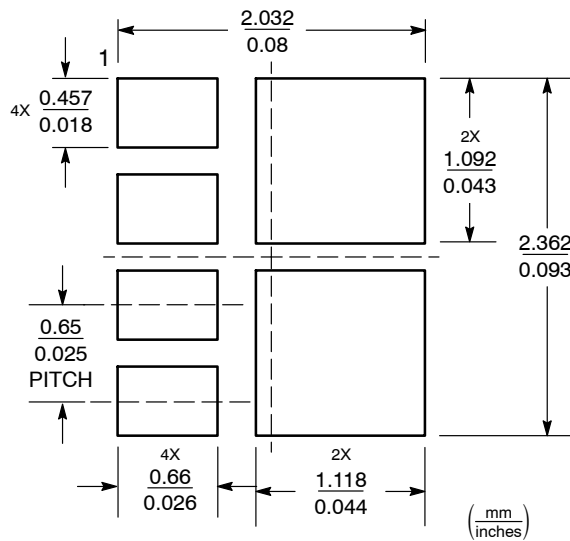
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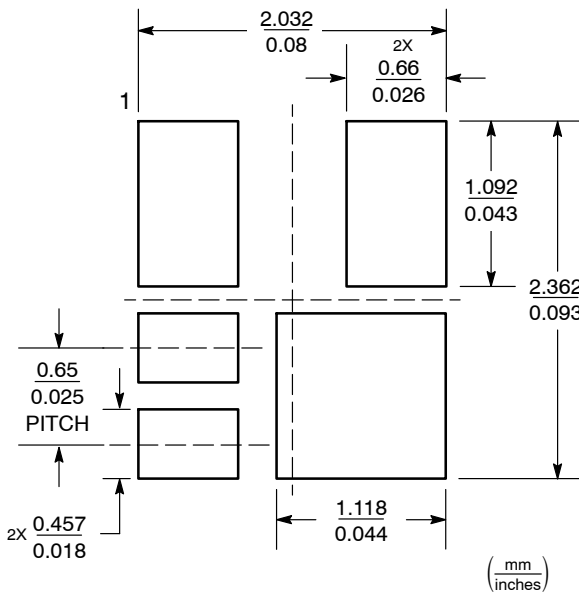
ADDITIONAL SOLDERING FOOTPRINTS*



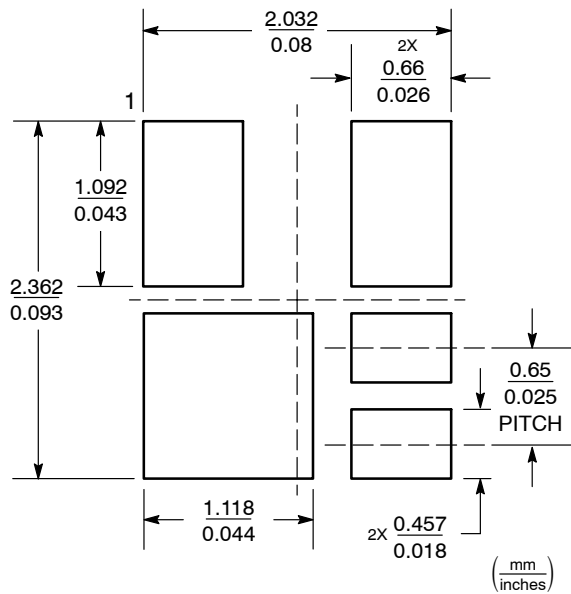
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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