Nuvoton
N-Channel FET Synchronous Buck Regulator Controller
W83321S
W83321G

Publication Release Date: January, 2006
Revision 0.51

W83321S
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1		2004/3/19	0.5	N.A	All versions before 0.5 are for internal use only.
2	5	2005/1/21	0.51	N.A	1. Add Pb-free part no:W83321G 2. Add separate VCC12 rail for VBOOT application circuit.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

Table of Content-

1. GENERAL DESCRIPTION

The W83321S is a high-speed, N-Channel synchronous buck regulator controller. The W83321S employs fixed-frequency voltage-mode PWM control architecture. Both high-side and low-side MOSFETs are lower cost N-Channel type. The regulator is biased from a 5V rail and the power for the high-side MOSFET can be supplied by a separate 12V rail or supplied from a local charge pump.

Current limit is achieved by monitoring the voltage drop across the on resistance of the low-side MOSFET. This method eliminates the requirement of extra current sensing resistor and avoids false trigger of OC protection when V_{IN} varies. The adaptive non-overlapping MOSFET gate drivers help avoid potential shoot-through problems while maintaining high efficiency.

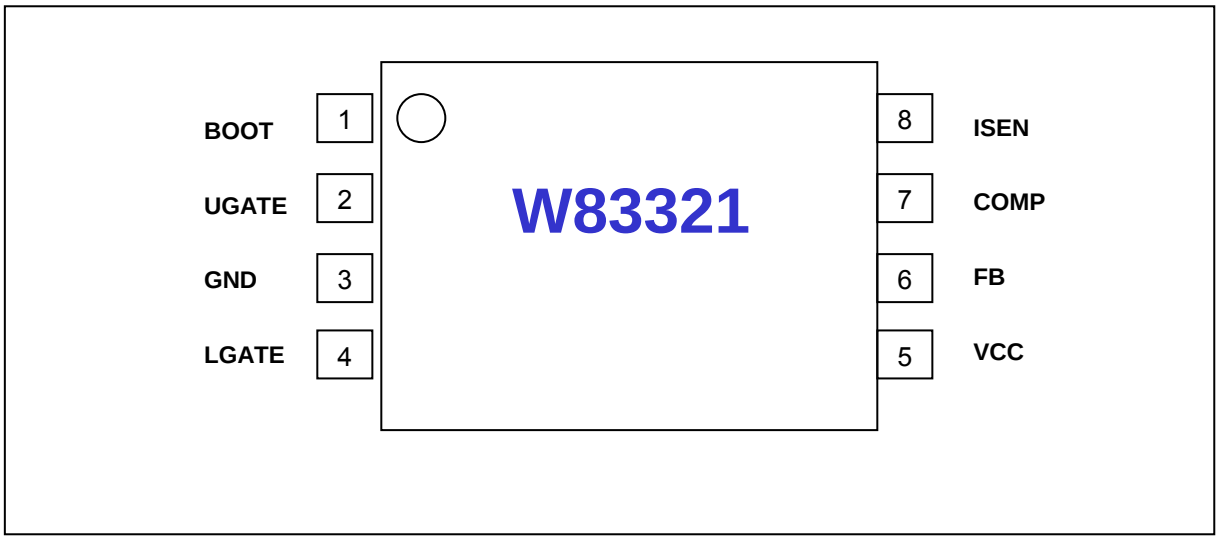
2. FEATURES

- Operates from +5V Input
- 0.8V to VIN Output Range
  - 0.8V Internal Reference
  - ±1.5% Over Line Voltage and Temperature
- Drives N-Channel MOSFETs
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
- Lossless, Programmable Overcurrent Protection
  - Uses Lower MOSFET's Rds (on)
  - Current limit without sense resistor
- Small Converter Size
  - 250 kHz Fixed Frequency Oscillator
  - Internal Soft Start
  - Tiny plastic SOP-8 package

3. APPLICATIONS

- Motherboard Power Supplies Regulation
- Subsystem Power Supplies
  - PCI/AGP/GTL+ Buses
  - ACPI Power Control
  - SSTL-2 and DDR SDRAM Bus Termination Supply
- Cable Modems, Set Top Boxes, and DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Power Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 5V-Input DC-DC Regulators
- Low-Voltage Distributed Power Supplies

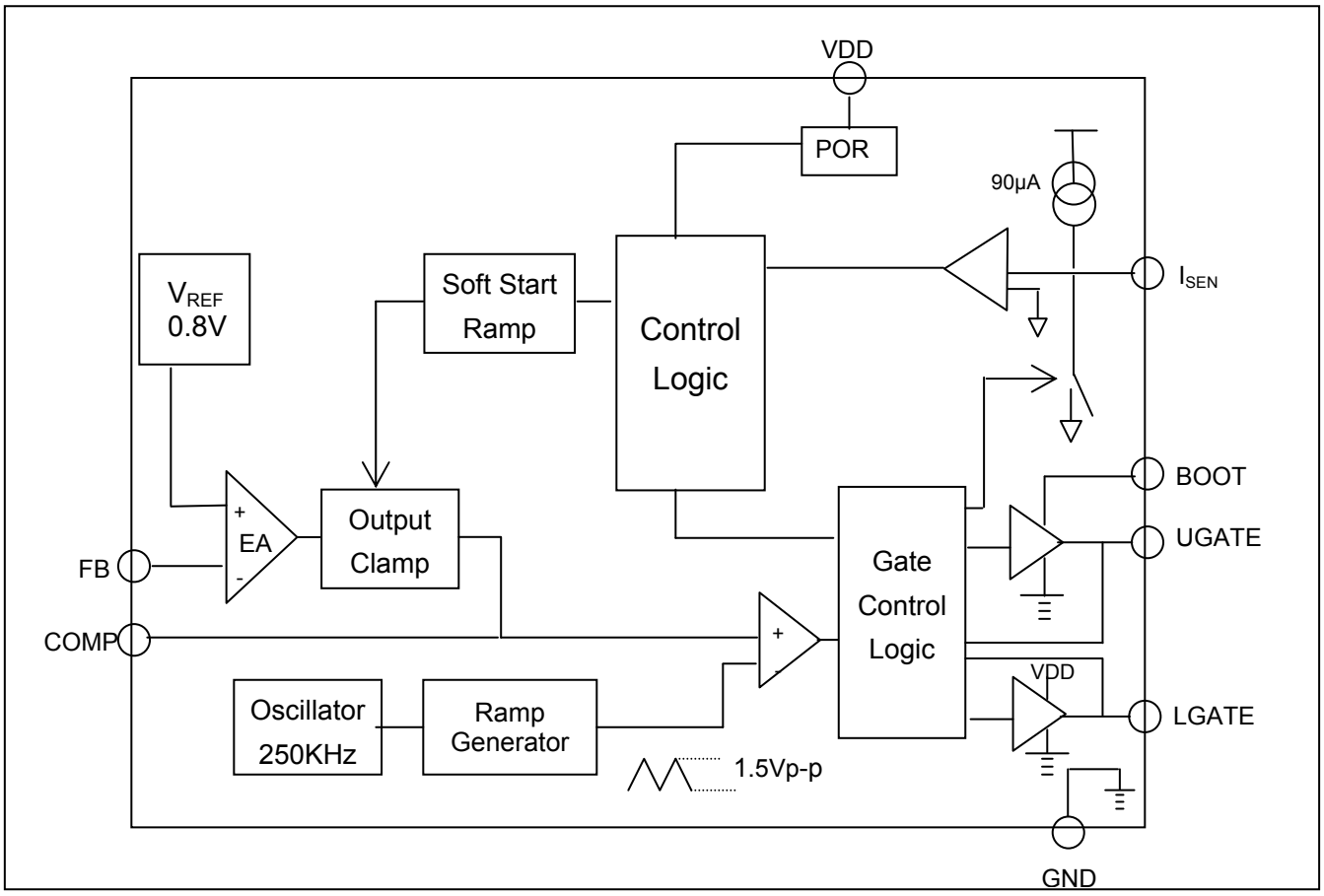
4. PIN-OUT



5. PIN DESCRIPTION

PIN	NAME	FUNCTION
1	**BOOT**	Supply rail for the high-side MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage or a separate 12V supply can be used.
2	**UGATE**	Gate drive for the high-side N-channel MOSFET. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the high-side MOSFET has turned off.
3	**GND**	Ground for analog circuit. Connect it to system ground.
4	**LGATE**	Gate drive for the low-side N-channel MOSFET. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the low-side MOSFET has turned off.
5	**VCC**	+5V supply rail for the lower gate driver and control logic circuit.
6	**FB**	Inverting Input of the Error Amplifier. This pin is available for compensation of the control loop.
7	**COMP**	Internal Error Amplifier Output Pin. This pin is available for compensation of the control loop and pulling this pin low with an open drain device will shutdown the IC.
8	**ISEN**	Current limit threshold setting. Connect a resistor (R_{OCSET}) between this pin and the drain of the low-side MOSFET.

6. INTERNAL BLOCK DIAGRAM



MOSFET Gate Drivers

Power for the high-side driver is through the BOOT pin. This voltage can be supplied by a separate, higher voltage source, or supplied from a local charge pump structure or even the combination of the two.

Since the voltage of the low-side MOSFET gate and the high-side MOSFET gate are being monitored to determine the state of the MOSFET, it should be considered carefully to add external components between the gate drivers and their respective MOSFET gates. Doing so may interfere with the shoot-through protection.

Current Limit (Over current protection)

Current limit is realized by sensing the voltage across the low-side MOSFET while it is on. This method enhances the converter's effeciency and reduces cost by eliminating a current sensing resistor.

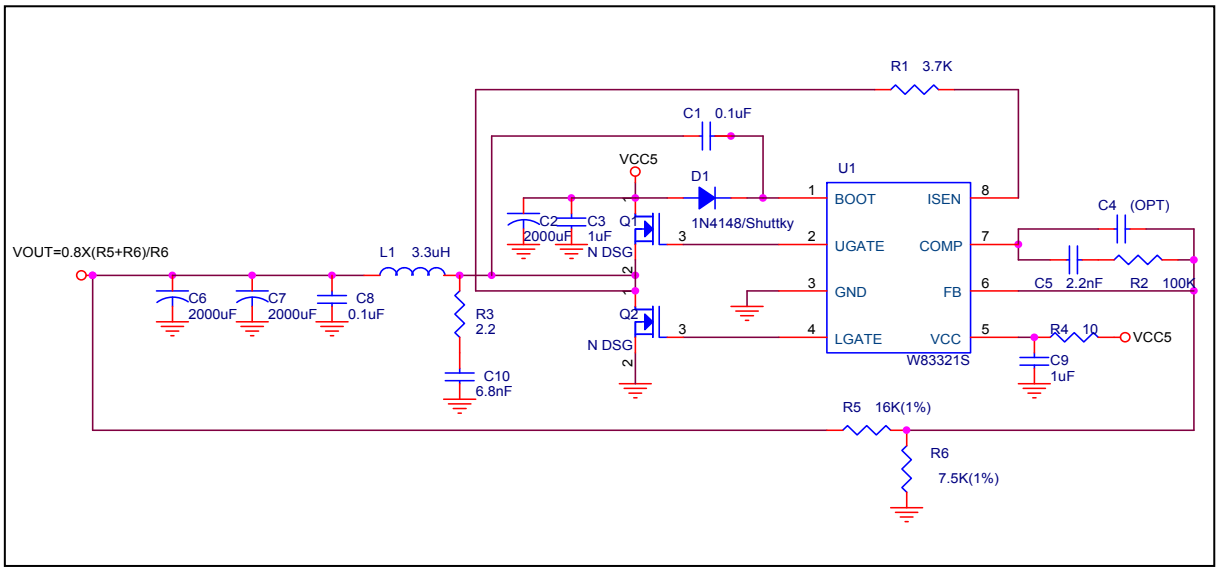
While low-side MOSFET is turned on, a constant current of 90uA is forced through R_{OCSET} which is an external resistor connected between phase and ISEN, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the chip enters current limit mode. In the current limit mode both the high-side and low-side MOSFETS are turned off. After a 25ms delay, a soft-start cycle is initiated. If the cause of the overcurrent is still present after the delay interval, the current limit

would be triggered again. The shut dowm - delay - soft start cycle will be repeated indefinitely untill the overcurrent event has cleared.

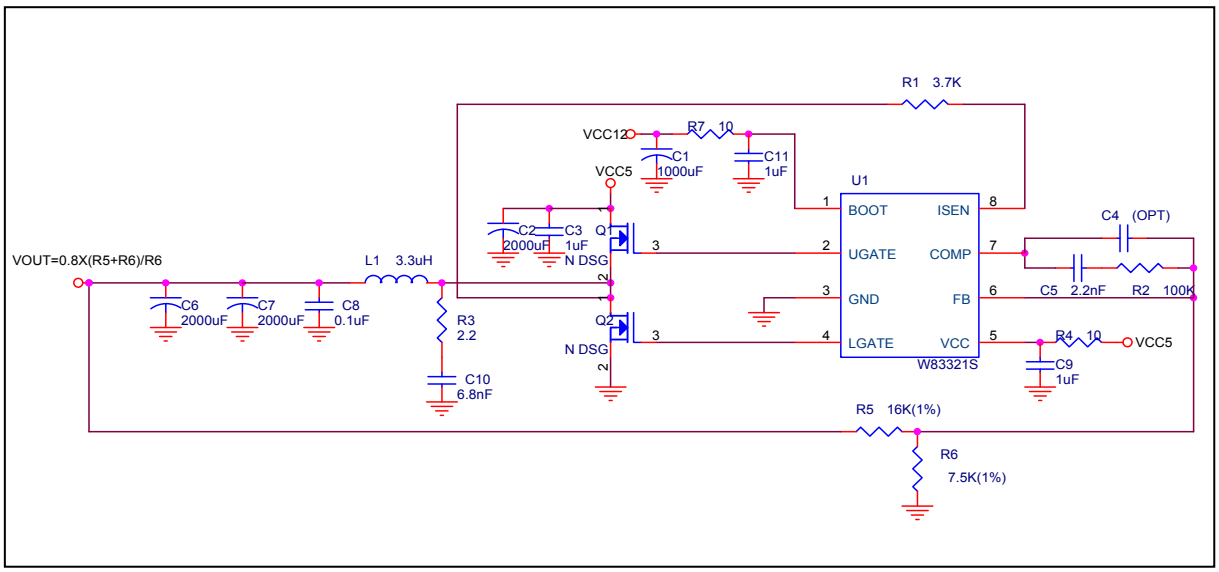
I_{PEAK} = (I_{OCSET} x R_{OCSET}) / $R_{DS(ON)}$ $R_{DS(ON)}$:Low Side MOSFET Resistance

7. APPLICATION CIRCUIT

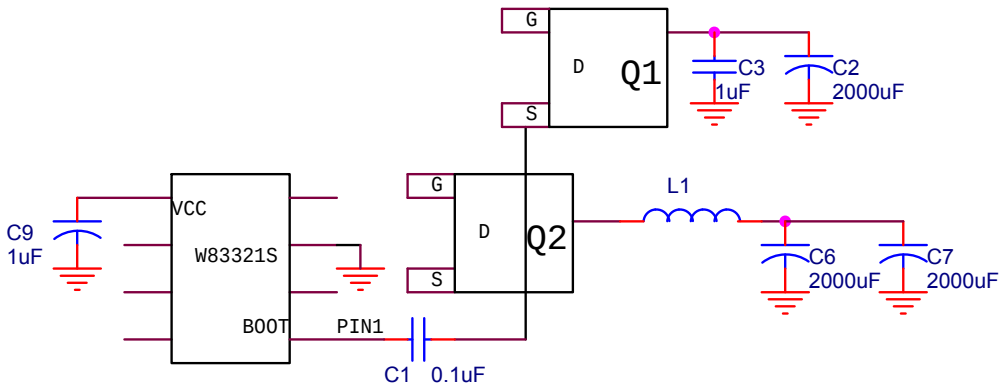
Local charge pump for VBOOT application:



Separate VCC12 rail for VBOOT application:



8. LAYOUT PLACEMENT



Layout Notes:

1. Put Q1 and Q2 as close as possible and using wide,short printed circuit traces between Q1 source and Q2 drain.
2. Put C2 and C3 to be near the Q1 drain and Q2 source nodes.
3. Put C1 as close as to BOOT pin.
4. Put C9 as close as to VCC pin.

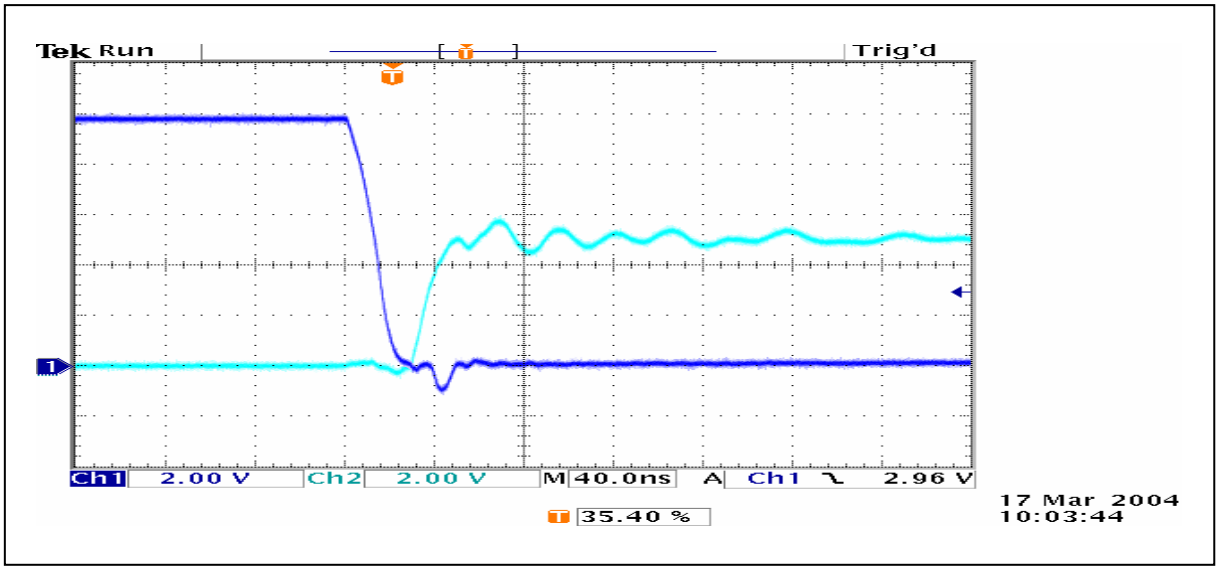
9. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Nominal Supply	I_{CC}	EN=V_{CC}; UGATE and LGATE Open	-	3	-	mA
POWER-ON RESET						
Rising V_{DD} Threshold			-	4.3	4.5	V
Falling V_{DD} Threshold			-	3.7	-	V
OSCILLATOR						
Free Running Frequency			200	250	300	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance	V_{REF}		-1.5	-	1.5	%
Reference Voltage			-	0.8	-	V
ERROR AMPLIFIER						
DC Gain			-	85	-	dB
Gain-Bandwidth			-	5.5	-	MHz
Slew Rate			-	4.1	-	$V/_{\mu S}$
GATE DRIVERS						
High-side Gate Source	$I_{HGATE-SRC}$	V_{BOOT}=12V,V_{UGATE}=6V	250	-	-	mA
High-side Gate Sink	$I_{HGATE-SNK}$	V_{BOOT}=12V,V_{UGATE}=6V	600	-	-	mA
Low-side Gate Source	$I_{LGATE-SRC}$	V_{CC}=5V, V_{LGATE}=2.5V	250	-	-	mA
Low-side Gate Sink	$I_{LGATE-SNK}$	V_{CC}=5V, V_{LGATE}=2.5V	300	-	-	mA
PROTECTION/DISABLE						
ISEN Current Source	I_{SEN}		72	90	108	µA
Disable Threshold	V_{COMP}		-	0.4	-	V

10. TYPICAL OPERATING WAVEFORMS

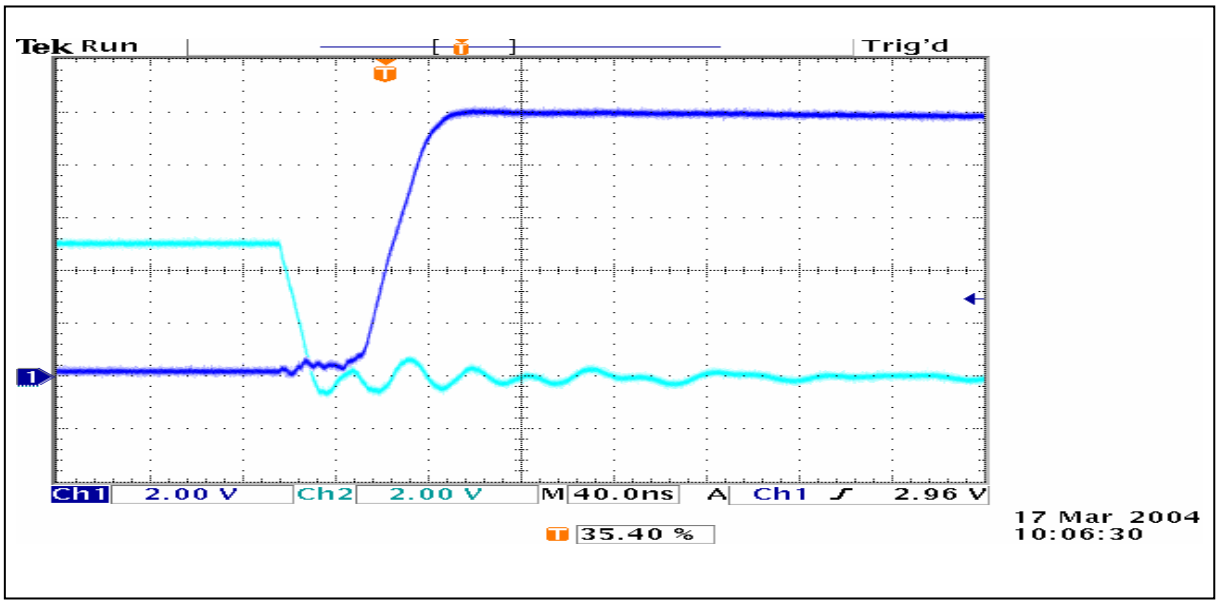
Dead Time: VCC=5V; VOUT=2.5V

Channel 1: UGATE Channel 2: LGATE



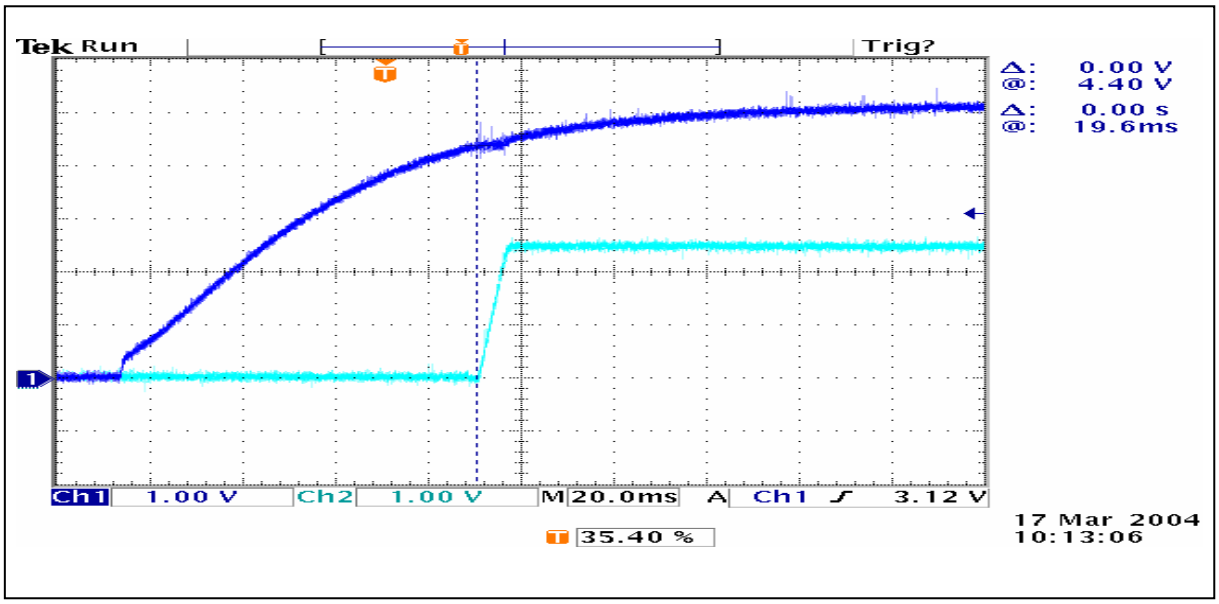
Dead Time: VCC=5V; VOUT=2.5V

Channel 1: UGATE Channel 2: LGATE



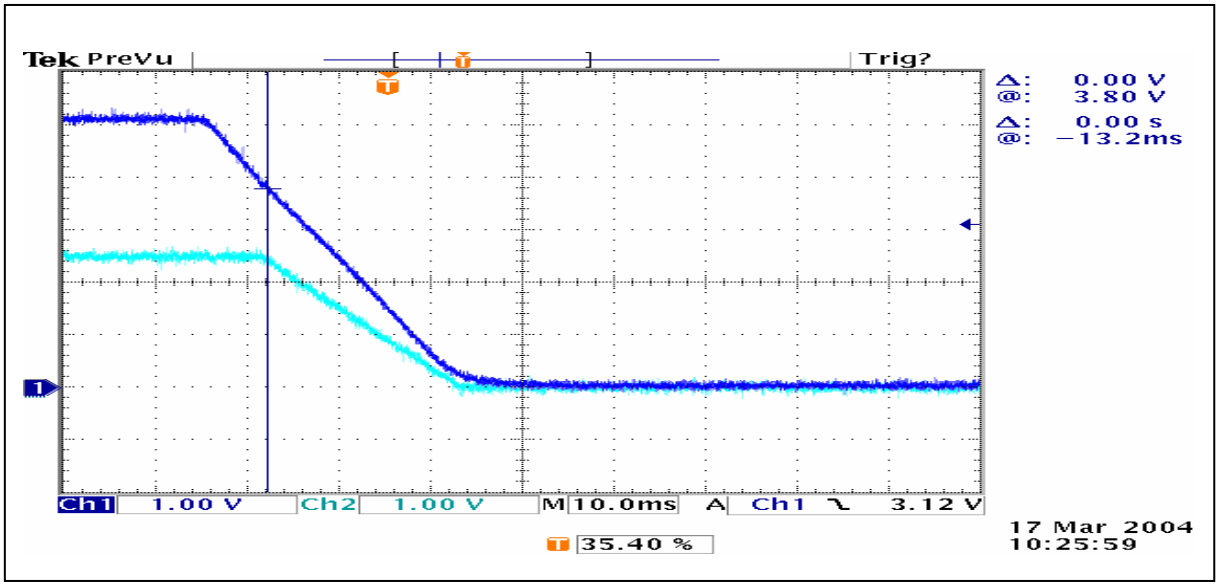
Power On: VCC=5V; VOUT=2.5V

Channel 1: VCC Channel 2: VOUT



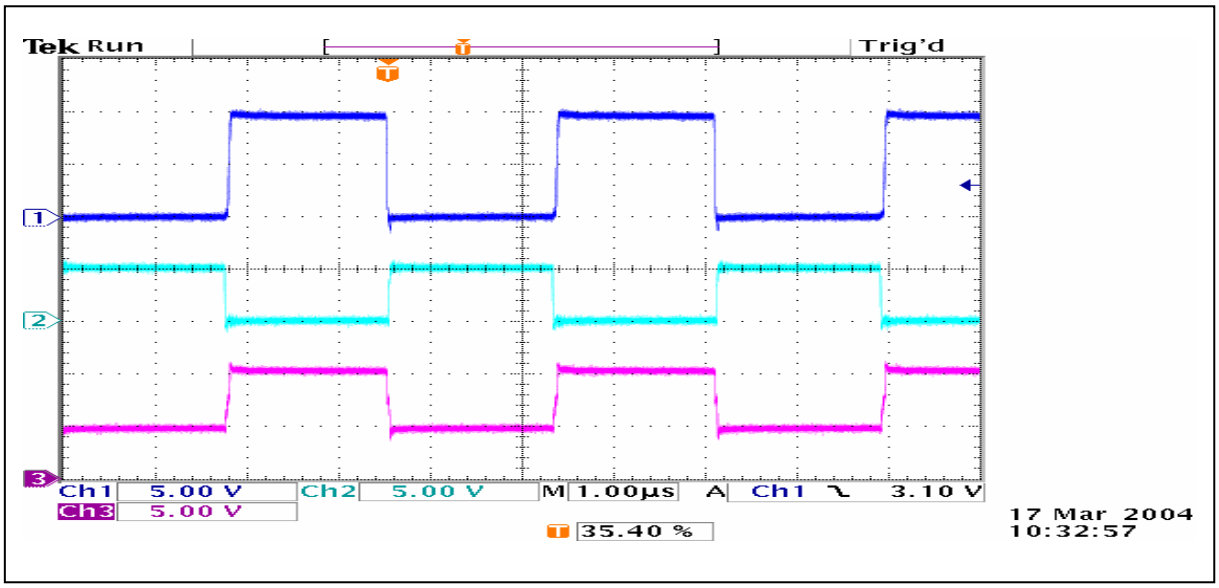
Power Off: VCC=5V; VOUT=2.5V

Channel 1: VCC Channel 2: VOUT



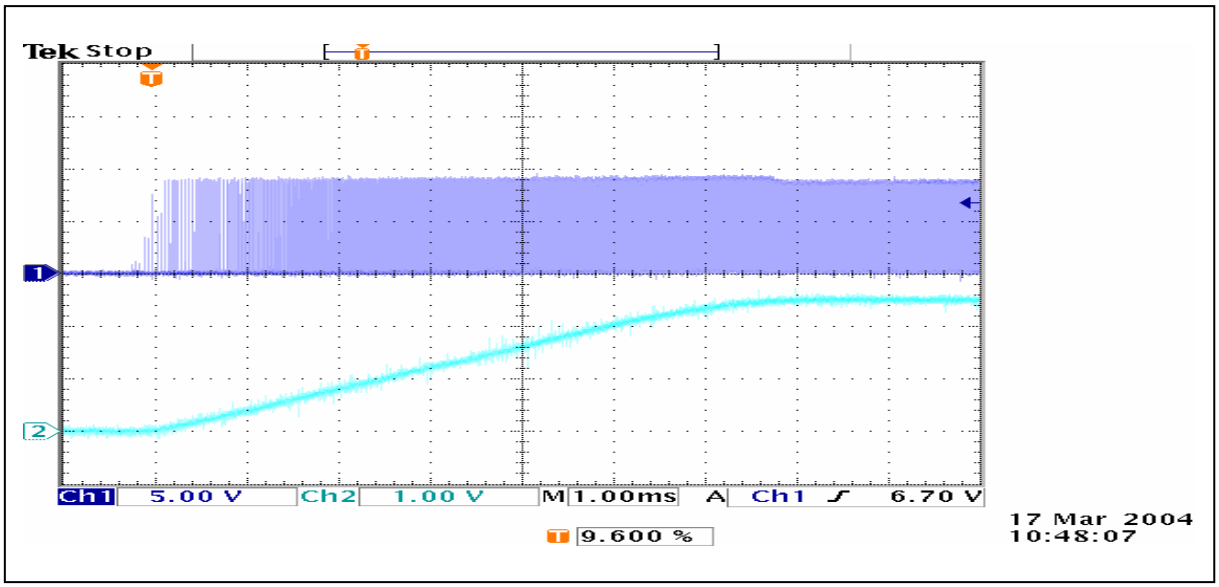
Bootstrap: VCC=5V; VOUT=2.5V

Channel 1: UGATE Channel 2: LGATE Channel 3: BOOT



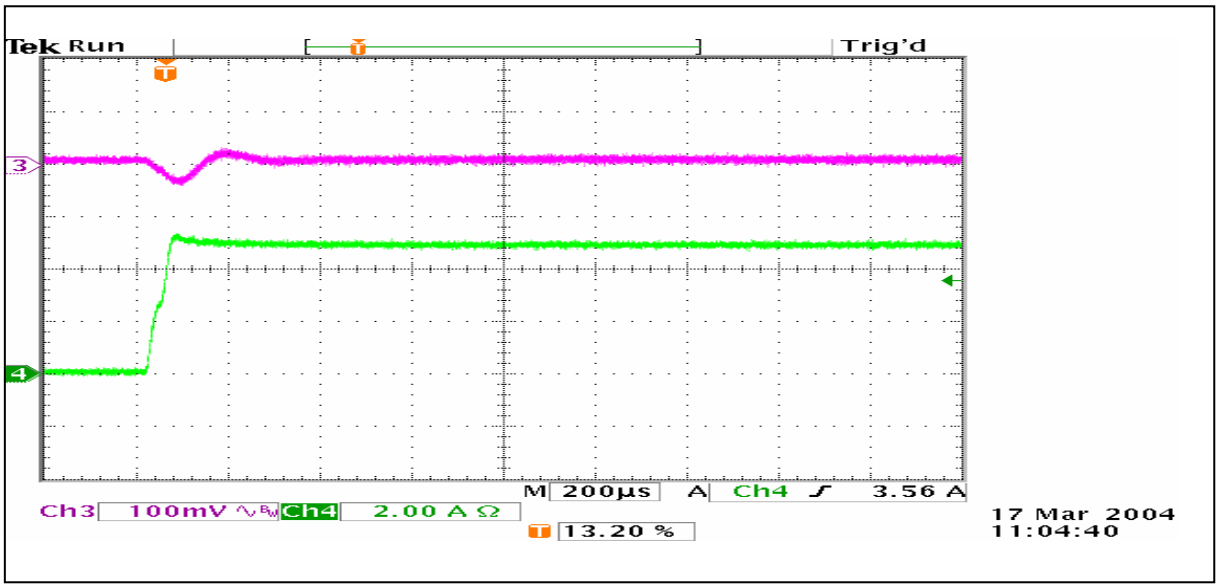
Soft Start: VCC=5V; VOUT=2.5V

Channel 1: UGATE Channel 2: VOUT



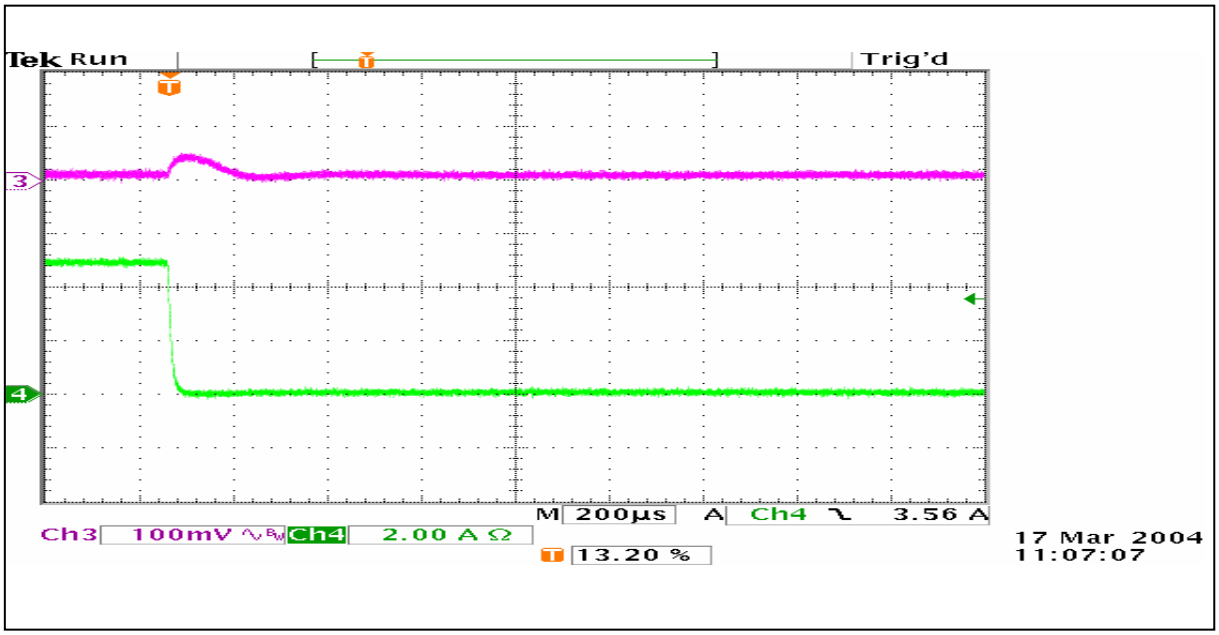
Load Transient: VCC=5V; VOUT=2.5V; Cout=2200uF

Channel 3: VOUT Channel 4: Iout (Loading=0→5A)



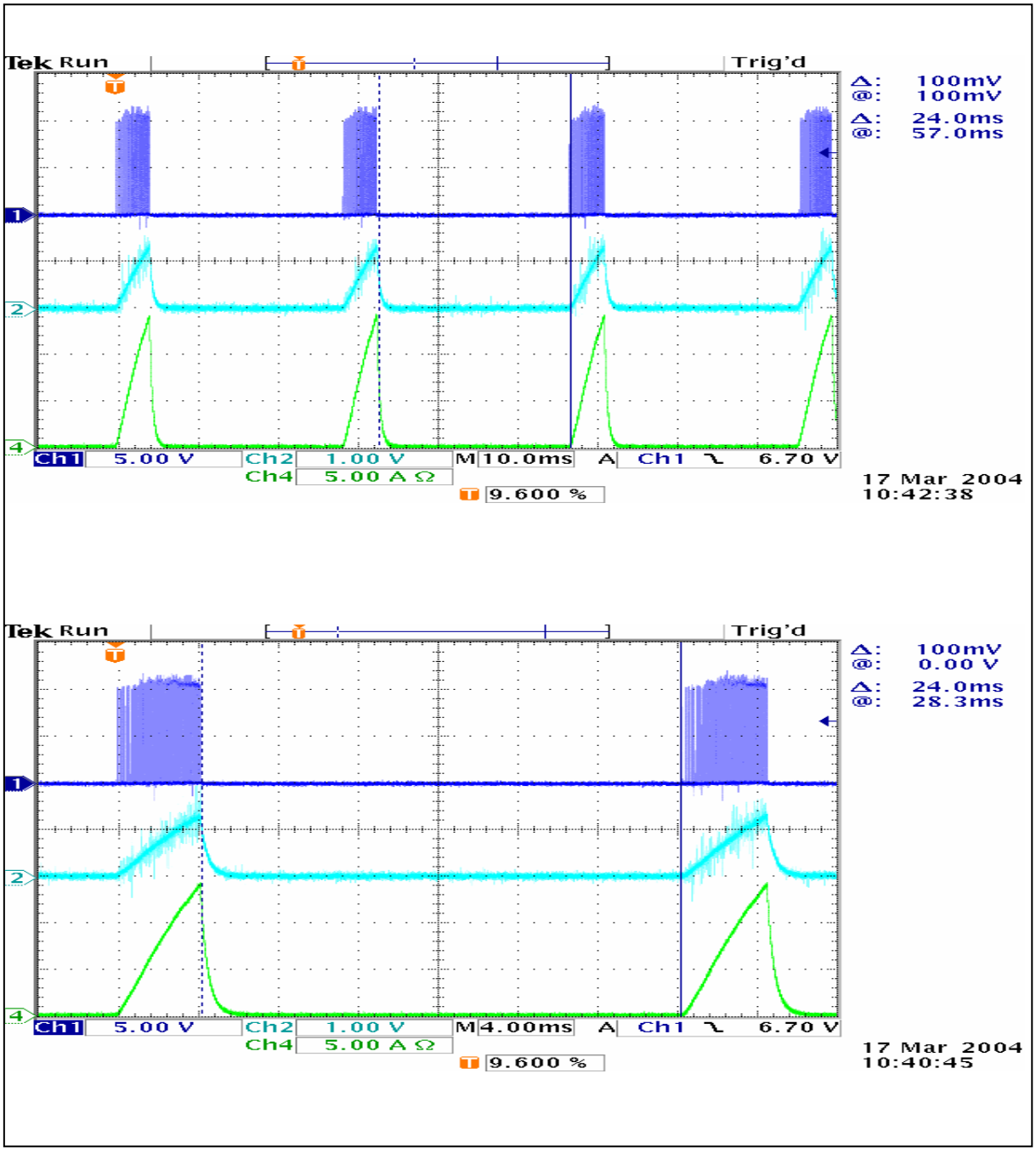
Load Transient: VCC=5V; VOUT=2.5V; Cout=2200uF

Channel 3: VOUT Channel 4: Iout (Loading=5→0A)



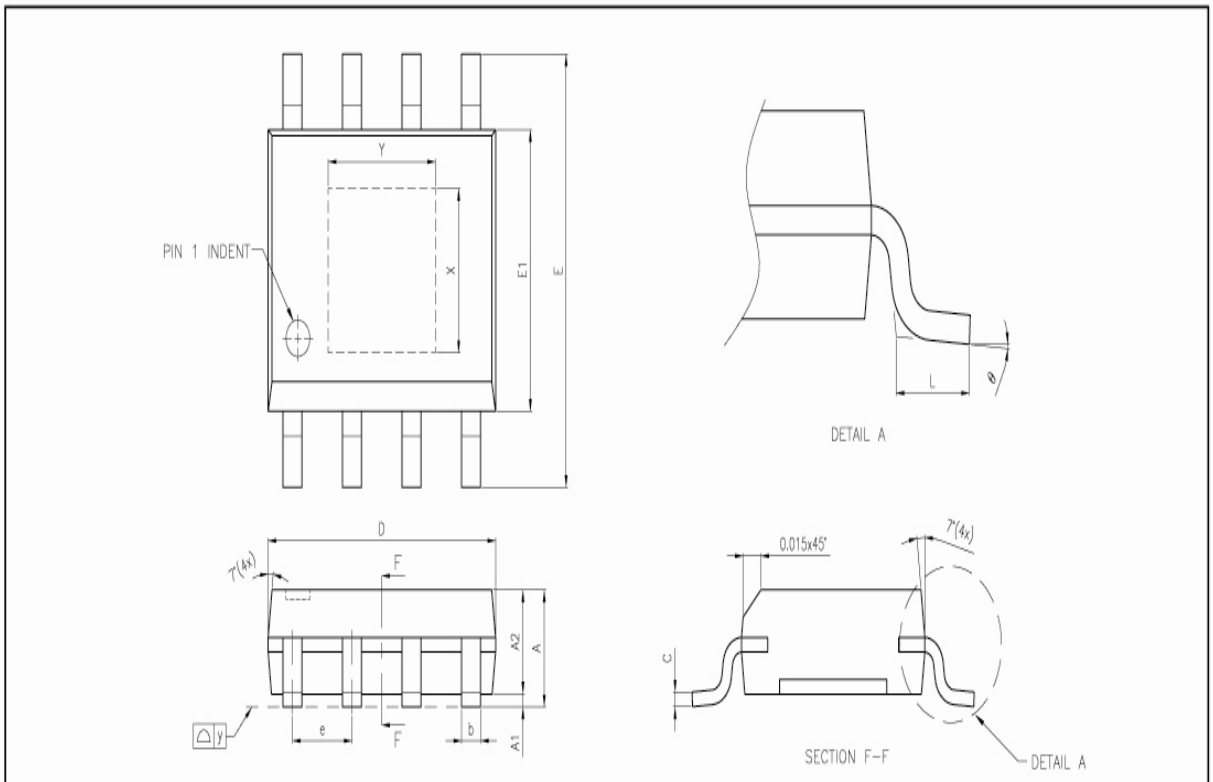
Short Hiccup: VCC=5V; VOUT=2.5V; Cout=2200uF with R=0.1(ohm) load.

Channel 1: UGATE Channel 2: VOUT Channel4: Iout



11. PACKAGE DIMENSION OUTLINE

8L SOP (150mil)



NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

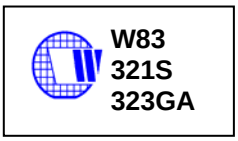
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
⚠ A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

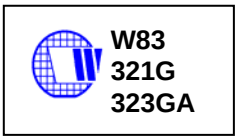
EXPOSED PAD DIMENSION : (MIL)
PAD SIZE: X Y
90*90

12. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83321S	8-pin SOP	Operation - Commercial 0~70℃
W83321G	8-pin SOP	Operation - Commercial 0~70℃ Pb-free package

13. HOW TO READ THE TOP MARKING





Left Line: Nuvoton Logo

1st and 2nd Line: the part number,**321G** is for Pb-free package

3rd Line: Tracking Code

323: packages assembled in Year 03', week 23

G: assembly house ID; G means GR, O means OSE, etc.

A: the IC version

Important Notice

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