ANALOG DEVICES

Evaluation Board User Guide
UG-276

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Evaluation Board for the ADN2850 Digital Rheostat

FEATURES

Full featured evaluation board for the ADN2850
Several test circuits
Various ac/dc input signals
PC control via a separately purchased system development platform (SDP)
PC control software
26 extra bytes in EEMEM for user-defined information
Resistor tolerance error stored in EEMEM

PACKAGE CONTENTS

EVAL-ADN2850SDZ evaluation board
CD that includes
- **Self-installing software that allows users to control the board and exercise all functions of the device**
- **Electronic version of the ADN2850 data sheet**
- **Electronic version of the UG-276 document**

GENERAL DESCRIPTION

This user guide describes the evaluation board for evaluating the ADN2850—a dual-channel, 1024-position, nonvolatile memory digital resistor. With versatile programmability, the ADN2850 allows multiple modes of operation, including read/write access in the RDAC and EEMEM registers, increment/decrement of resistance, resistance changes in ±6 dB scales, wiper setting read-back, and extra EEMEM for storing user-defined information, such as memory data for other components or a lookup table.

The ADN2850 supports a dual-supply ±2.25 V to ±2.75 V operation and a single-supply 2.7 V to 5.5 V operation, making the device suited for battery-powered applications and many other applications. In addition, the ADN2850 uses a versatile SPI-compatible serial interface, allowing speeds of up to 50 MHz.

The EVAL-ADN2850SDZ can operate in single-supply and dual-supply mode and incorporates an internal power supply from the USB.

Complete specifications for the ADN2850 part can be found in the ADN2850 data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

DIGITAL PICTURE OF EVALUATION BOARD WITH SYSTEM DEMONSTRATION PLATFORM

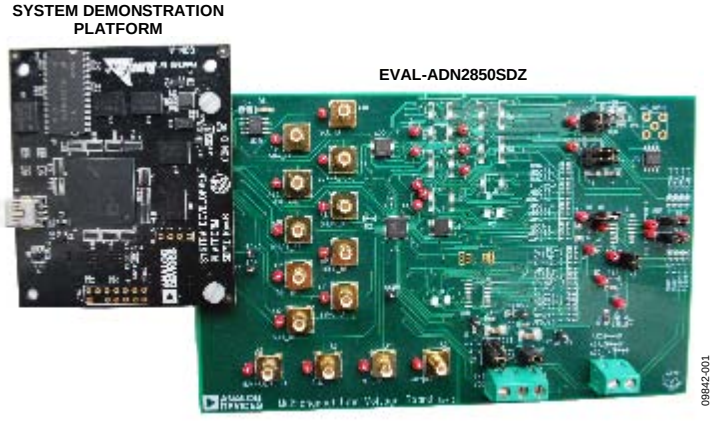

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

5/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-ADN2850SDZ supports the use of single and dual power supplies.

In single-supply mode, the evaluation board can be powered either from the SDP port or externally by the J1-1, J1-2, and J1-3 connectors, as described in Table 1.

If dual-supply mode is required, the J1-1, J1-2, and J1-3 connectors must provide the external power supply, as described in Table 1.

All supplies are decoupled to ground using 10 µF tantalum and 0.1 µF ceramic capacitors.

Table 1. Maximum and Minimum Voltages of the Connectors

Connector No.	Label	Voltage
J1-1	EXT VDD	Analog positive power supply, V_{DD}. For single-supply operation, it is 2.7 V to 5.5 V. For dual-supply operation, it is 2.5 V to 2.75 V.
J1-2	GND	Analog GND.
J1-3	EXT VSS	Analog negative power supply, V_{SS}. For single-supply operation, it is 0 V. For dual-supply operation, it is −2.5 V to −2.75 V.

LINK OPTIONS

Several link and switch options are incorporated in the evaluation board and should be set up before using the board. Table 2 describes the positions of the links to control the evaluation board by a PC, via the SDP board, using the EVAL-ADN2850SDZ in single-supply mode. The functions of these link and switch options are described in detail in Table 3 through Table 6.

Table 2. Link Options Setup for SDP Control (Default)

Link No.	Option
A25	3.3 V
A24	GND

Table 3. Link Functions

Link No.	Power Supply	Options
A25	V_{DD}	This link selects one of the following as the positive power supply: 5 V (from SDP). 3.3 V (from SDP). EXT (external supply from the J1-1 connector).
A24	V_{SS}	This link selects one of the following as the negative power supply: GND (analog ground). VSS (external supply from the J1-3 connector).

TEST CIRCUITS

The EVAL-ADN2850SDZ incorporates several test circuits to evaluate the ADN2850 performance.

Pseudologarithmic DAC

RDAC1 can be operated as a pseudologarithmic DAC, as shown in Figure 2.

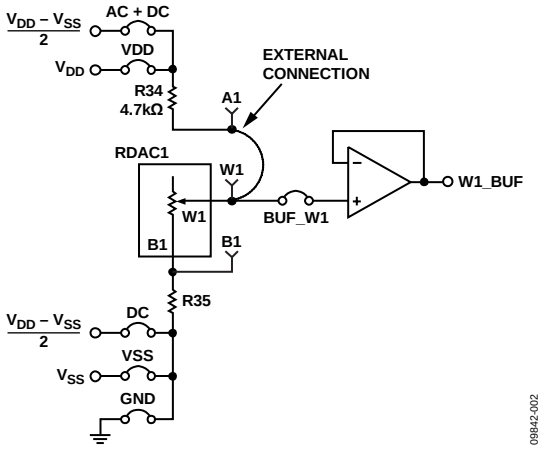

Figure 2. Pseudologarithmic DAC

The output voltage plot is shown in Figure 3. The output voltage is relative to V_{DD} and V_{SS}.

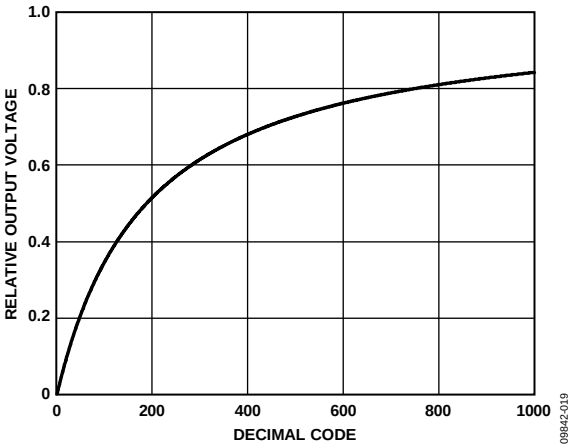

Figure 3. Pseudologarithmic Gain

Table 4 shows the options available for the voltage references.

Table 4. Pseudologarithmic DAC Voltage References

Terminal	Link	Options	Description
A1	A20	AC + DC	Connects R34 to $(V_{DD} - V_{SS})/2$
		VDD	Connects R34 to V_{DD}
W1	BUF_W1		Connects Terminal W1 to an output buffer
B1	A21	DC	Connects Terminal B1 to $(V_{DD} - V_{SS})/2$
		VSS	Connects Terminal B1 to V_{SS}
		GND	Connects Terminal B1 to analog ground

The output voltage is defined in Equation 1.

$$V_{OUT} = (V_{REF1} - V_{REF2}) \times \frac{R_{WB1}}{R_{WB1} + R34} + V_{REF2} \quad (1)$$

$$R_{WB1} = \frac{RDAC1}{1024} \times 25\ \text{k}\Omega \quad (2)$$

where:

R_{WB1} is the resistor between the W1 and B1 terminals.
V_{REF1} is the top voltage reference (A20 link).
V_{REF2} is the bottom voltage reference (A21 link).
RDAC1 is the code loaded in the RDAC1 register.

Pseudoantilogarithmic DAC

RDAC1 can be operated as a pseudoantilogarithmic DAC, as shown in Figure 4. In this case, R35 must be changed from the populated value of 0 Ω resistance to the suggested value of 4.7 kΩ.

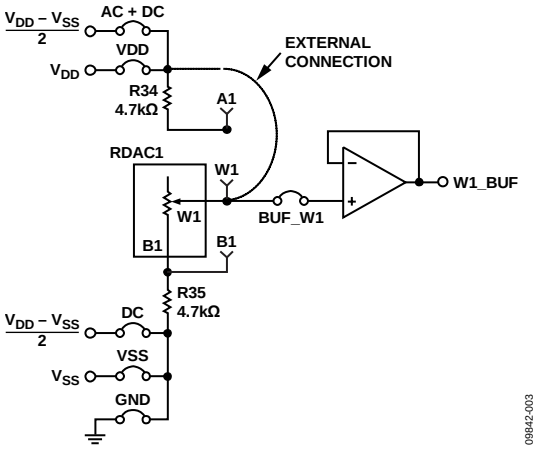

Figure 4. Pseudoantilogarithmic DAC.

The output voltage plot is shown in Figure 5. The output voltage is relative to V_{DD} and V_{SS}.

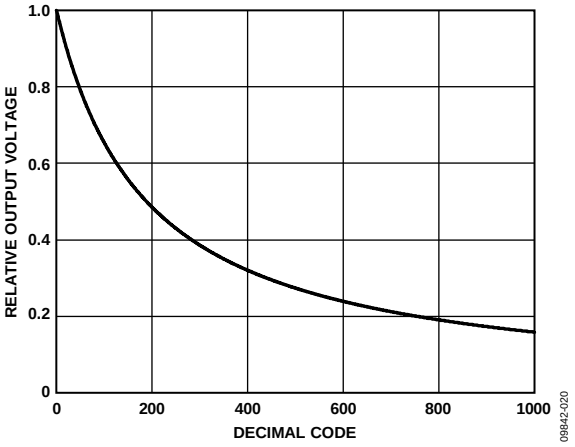

Figure 5. Pseudoantilogarithmic Gain

Table 5 shows the options available for the voltage references.

Table 5. Pseudoantilogarithmic DAC Voltage References

Terminal	Link	Options	Description
A1	A20	AC + DC	Connects Terminal W1 to $(V_{DD} - V_{SS})/2$
		VDD	Connects Terminal W1 to V_{DD}
W1	BUF_W1		Connects Terminal W1 to an output buffer
B1	A21	DC	Connects R35 to $(V_{DD} - V_{SS})/2$
		VSS	Connects R35 to V_{SS}
		GND	Connects R35 to analog ground

The output voltage is defined in Equation 3.

$$V_{OUT} = (V_{REF1} - V_{REF2}) \times \frac{R35}{R_{WB1} + R35} + V_{REF2} \quad (3)$$

$$R_{WB1} = \frac{RDAC1}{1024} \times 25\ \text{k}\Omega \quad (4)$$

where:
R_{WB1} is the resistor between the W1 and B1 terminals.
V_{REF1} is the top voltage reference (A20 link).
V_{REF2} is the bottom voltage reference (A21 link).
RDAC1 is the code loaded in the RDAC1 register.

Signal Amplifier

RDAC2 can be operated as an inverting or noninverting signal amplifier supporting linear gains. Table 6 shows the available configurations.

Table 6. Amplifier Selection Link Options

Amplifier	Gain	Link	Label
Noninverting	Linear	A27	LINEAR
		A29	NON-INVERTING
		A30	NON-INVERTING
Inverting	Linear	A27	LINEAR
		A29	INVERTING
		A30	INVERTING

The noninverting amplifier with linear gain is shown in Figure 6, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB2}}{R38} \quad (4)$$

where R_{WB2} is the resistor between the W2 and B2 terminals.

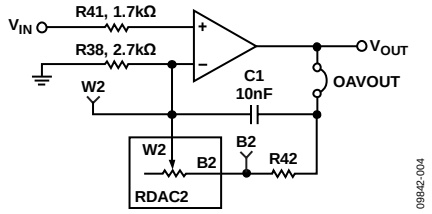

Figure 6. Linear Noninverting Amplifier

R42 can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 7, and the gain is defined in Equation 5.

$$G = -\frac{R_{WB2}}{R38} \quad (5)$$

where R_{WB2} is the resistor between the W2 and B2 terminals.

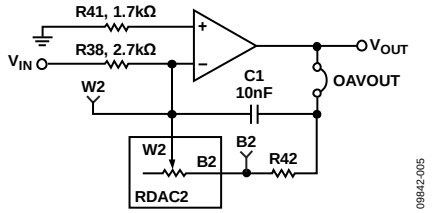

Figure 7. Linear Inverting Amplifier

R42 can be used to set the maximum and minimum gain limits.

Current Monitoring Configurable Function

The ADN2850 comes with a pair of matched diode connected PNPs (Q1 and Q2) accessible from external pins (I_1 and I_2); test points (V1 and V2) allow direct access to these pins, as shown in Figure 8.

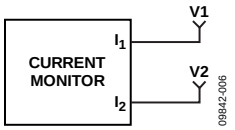

Figure 8. Current Monitoring

The ADN2850 data sheet provides a detailed description how to use these current monitor terminals.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-ADN2850SDZ evaluation kit includes evaluation board software provided on a CD. The software is compatible with Windows® XP, Windows Vista, and Windows 7 (both 32 and 64 bits).

Install the software before connecting the SDP board to the USB port of the PC to ensure that the SDP board is recognized when it is connected to the PC.

1. Start the Windows operating system and insert the CD.
2. The installation software opens automatically. If it does not, run the **setup.exe** file from the CD.
3. After installation is completed, power up the evaluation board as described in the Power Supplies section.
4. Plug the EVAL-ADN2850SDZ into the SDP board and the SDP board into the PC using the USB cable included in the box.
5. When the software detects the evaluation board, follow the instructions that appear to finalize the installation.

To uninstall the program, click **Start** > **Control Panel** > **Add or Remove Programs** > **ADN2850 Eval Board**.

RUNNING THE SOFTWARE

To run the evaluation board software, do the following:

1. Click **Start** > **All Programs** > **Analog Devices** > **ADN2850** > **ADN2850 Eval Board**.
2. If the SDP board is not connected to the USB port when the software is launched, a connectivity error is displayed (see Figure 9). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

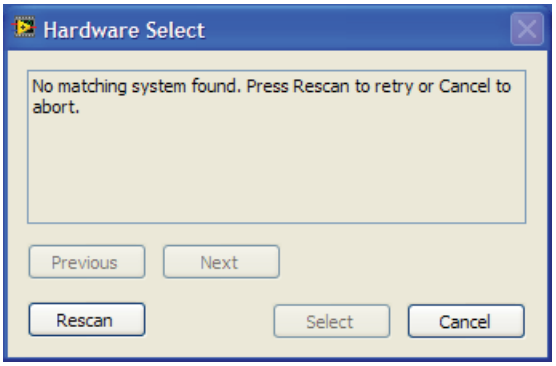

Figure 9. Pop-Up Window Error

The main window of the EVAL-ADN2850SDZ evaluation software then opens, as shown in Figure 10.

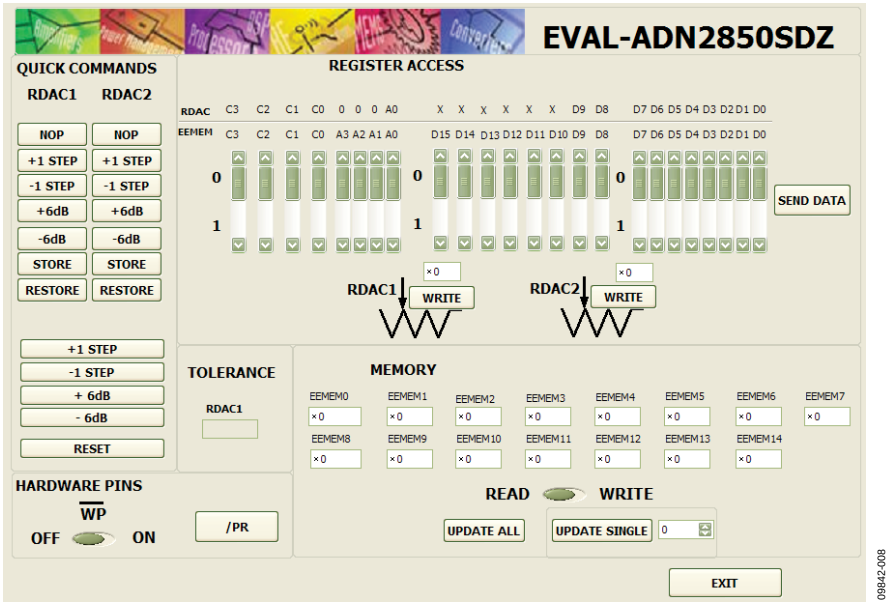

Figure 10. EVAL-ADN2850SDZ Evaluation Board Software Main Window

SOFTWARE OPERATION

The main window of the EVAL-ADN2850SDZ software is divided into the following sections: **QUICK COMMANDS**, **REGISTER ACCESS**, **HARDWARE PINS**, **TOLERANCE**, and **MEMORY**. The features of the main window are as follows:

- The **QUICK COMMANDS** section allows you to send the ADN2850 quick commands directly to the ADN2850.
- The **REGISTER ACCESS** section can be used to update the RDAC registers by typing a value into a window and clicking **WRITE**. Alternatively, you can send a customized SPI data word by manually switching the scroll bars from 0 to 1 or from 1 to 0, as desired, and then clicking **SEND DATA**. When **WRITE** is clicked or a quick command is executed, a write-read operation is performed, and the values displayed in this section are updated with the actual RDAC register values. This function can be used to verify whether the write operation was completed successfully. The scroll bars are updated upon each write transfer.
- The **HARDWARE PINS** section selects the level of the external control pins, switches the level of the $\overline{WP}$ pin, and generates a pulse in the $\overline{PR}$ pin.
- The **TOLERANCE** section displays the stored tolerance of the RDAC1 internal resistor.
- The **MEMORY** section displays the data stored in the memory block. The data can be updated by switching the scroll bar from **READ** to **WRITE**, updating a particular window value, clicking **UPDATE ALL** or **UPDATE SINGLE**, and selecting the memory location to write.
- Clicking **EXIT** closes the program but does not reset the part.

EVALUATION BOARD SCHEMATICS AND ARTWORK

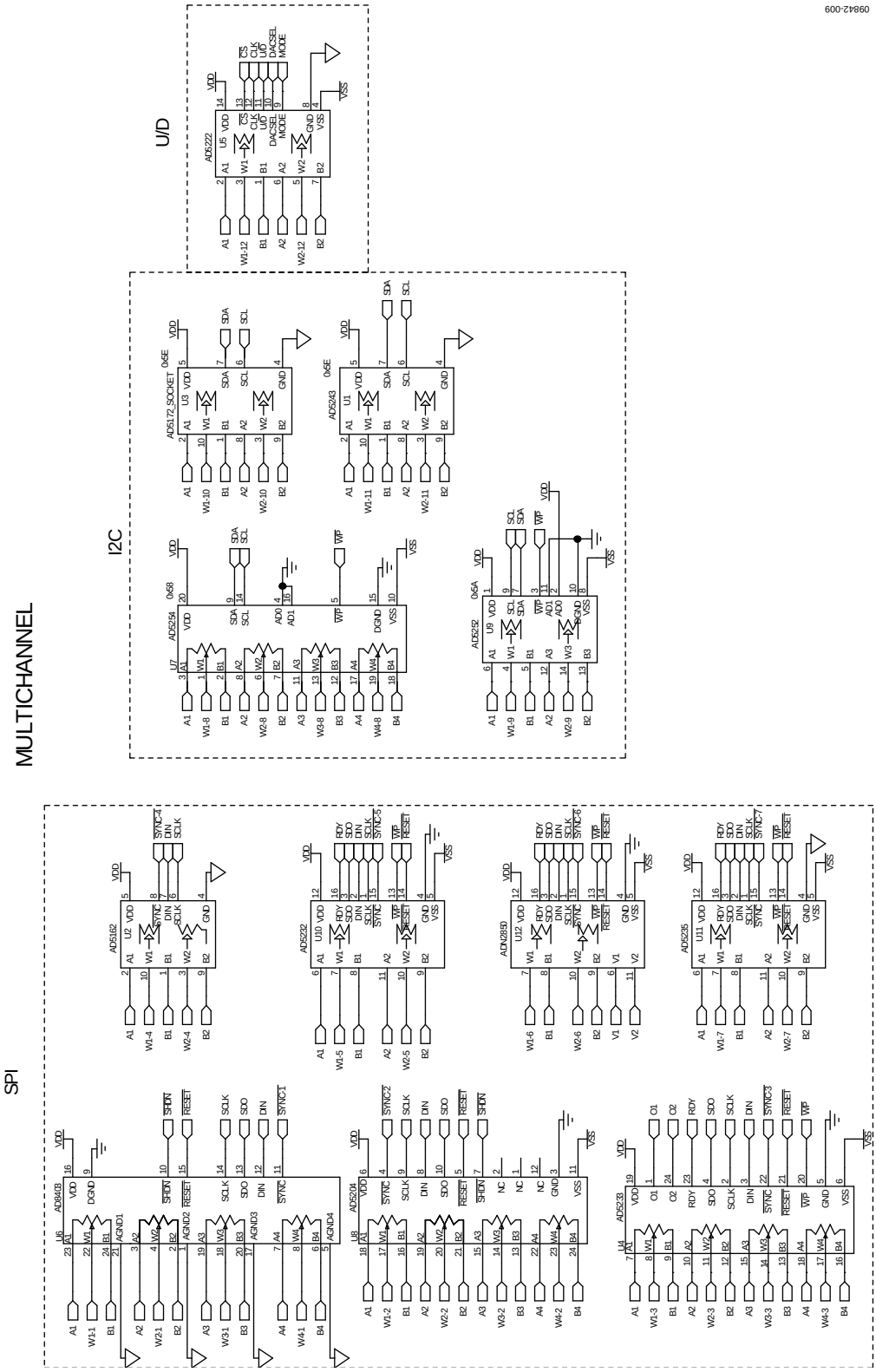

Figure 11. Schematic of Multiboard Digital Potentiometers

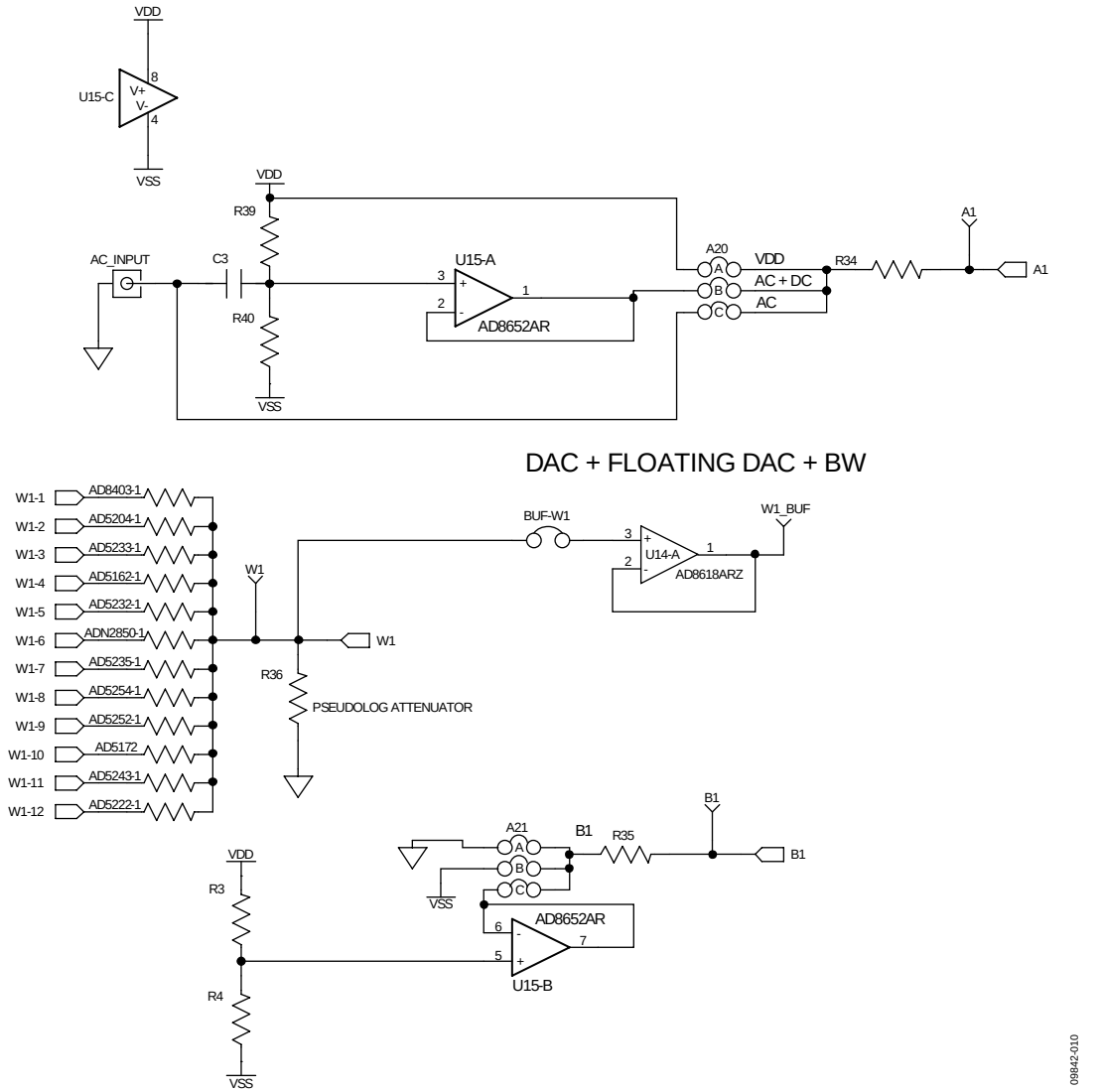

Figure 12. Schematic of Multiboard RDAC1 Circuits

INVERTING AND NON-INVERTING WITH LINEAR AND PSEUDO-LOG GAIN

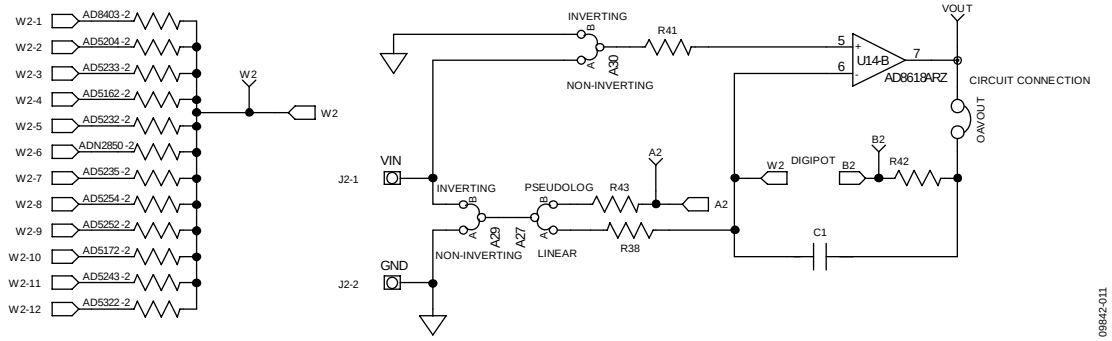

Figure 13. Schematic of Multiboard RDAC2 Circuits

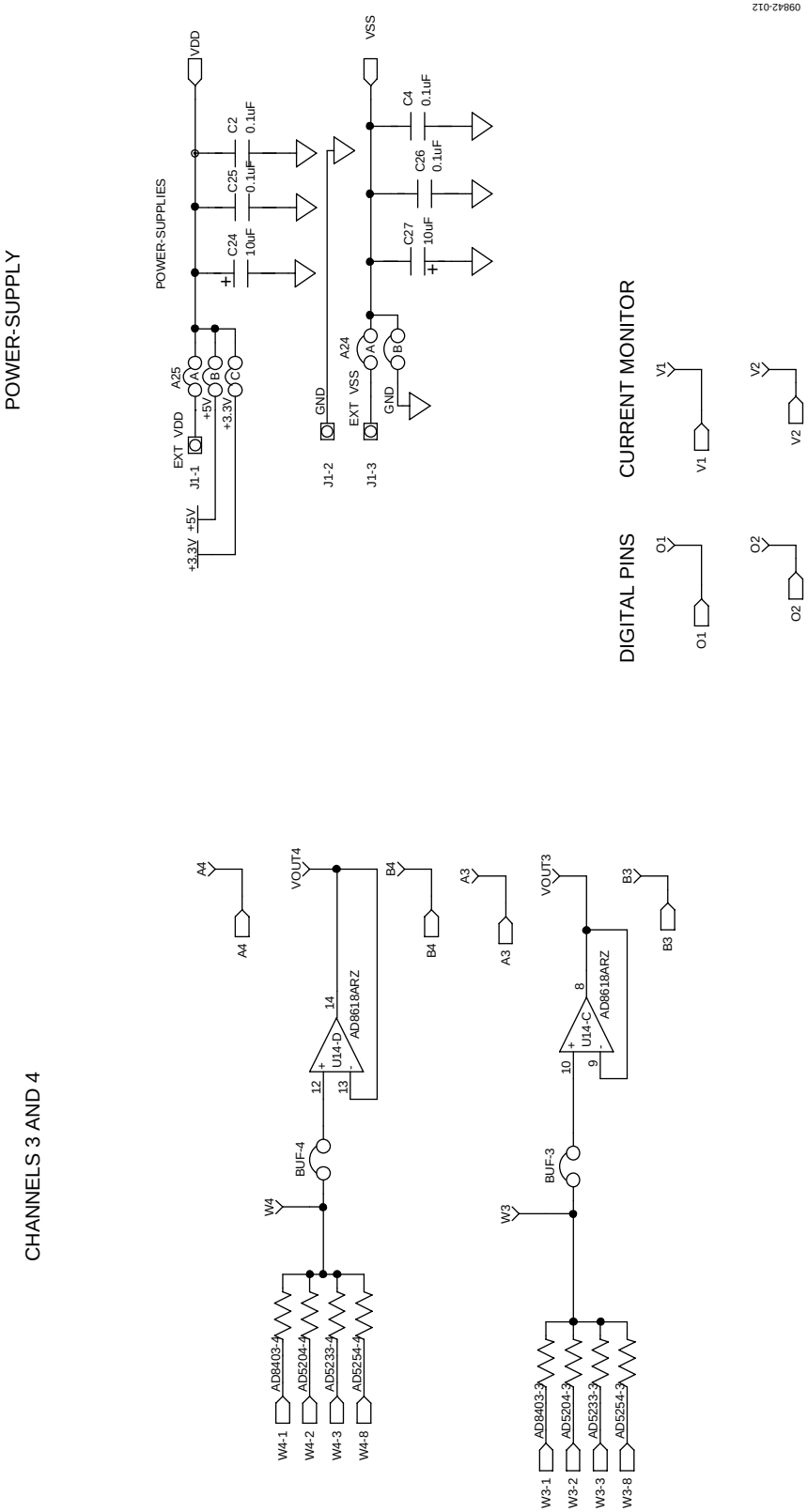

Figure 14. Schematic of ADN2850 Power Supplies and Other Channels

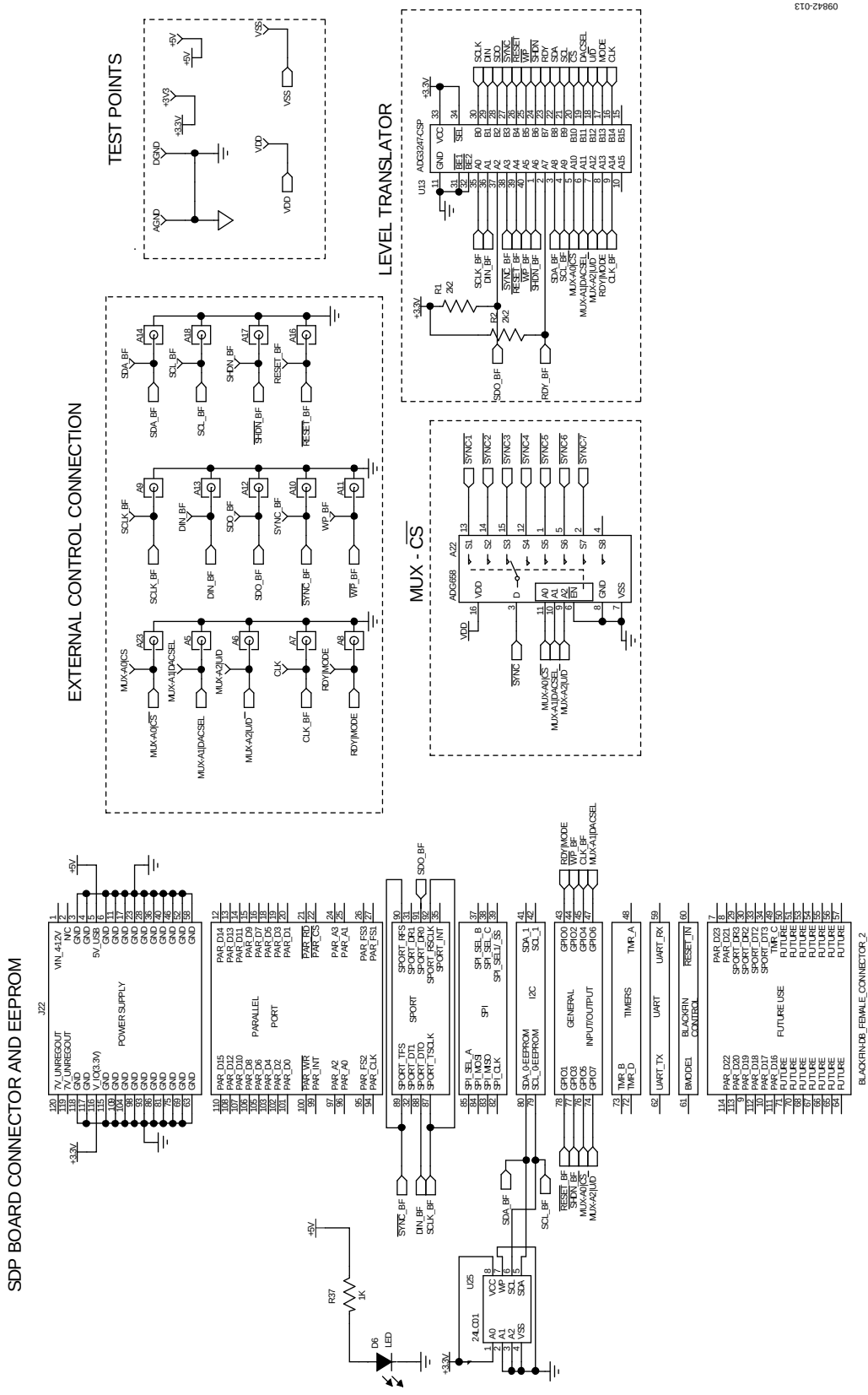

Figure 15. Schematic of SDP Connector

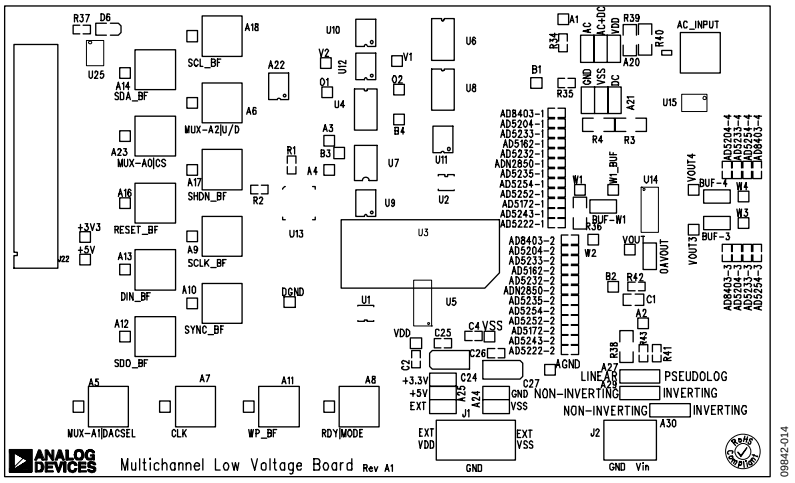

Figure 16. Component Side View

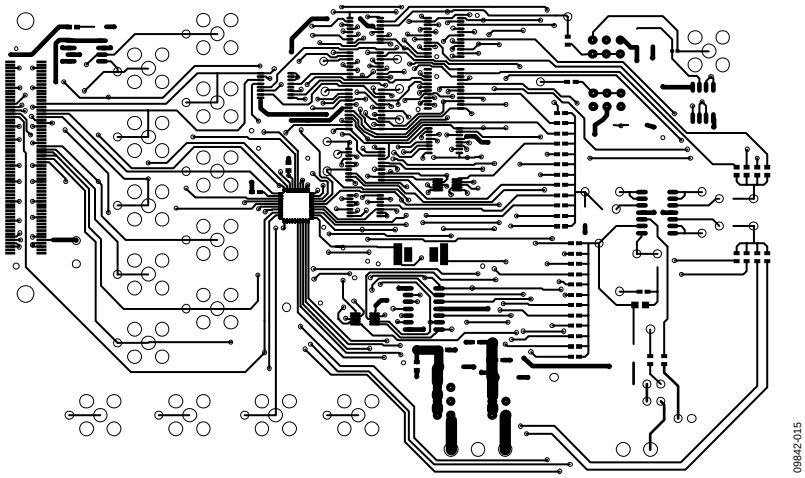

Figure 17. Component Placement Drawing

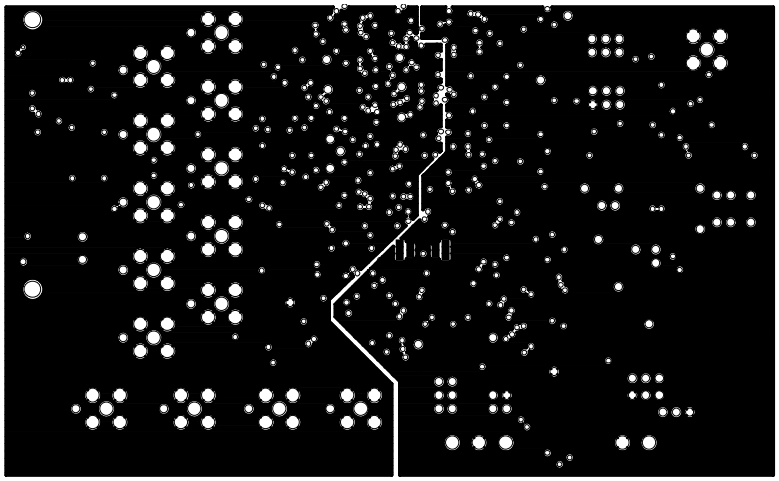

Figure 18. Layer 2 Side PCB Drawing

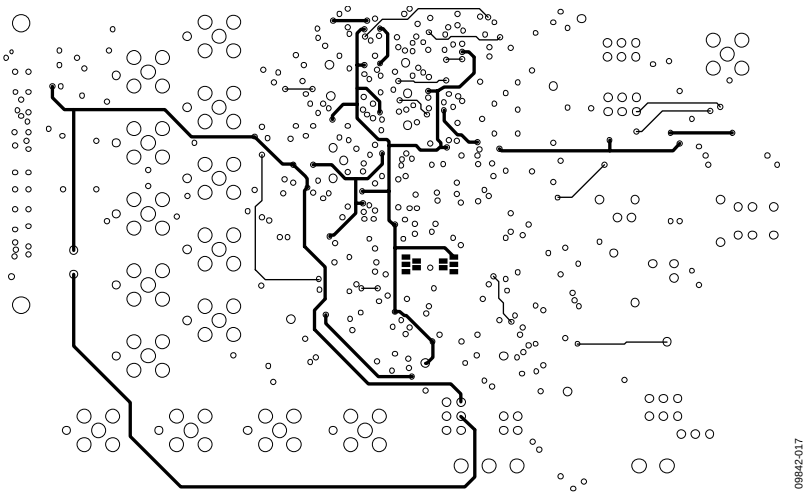

Figure 19. Layer 3 Side PCB Drawing

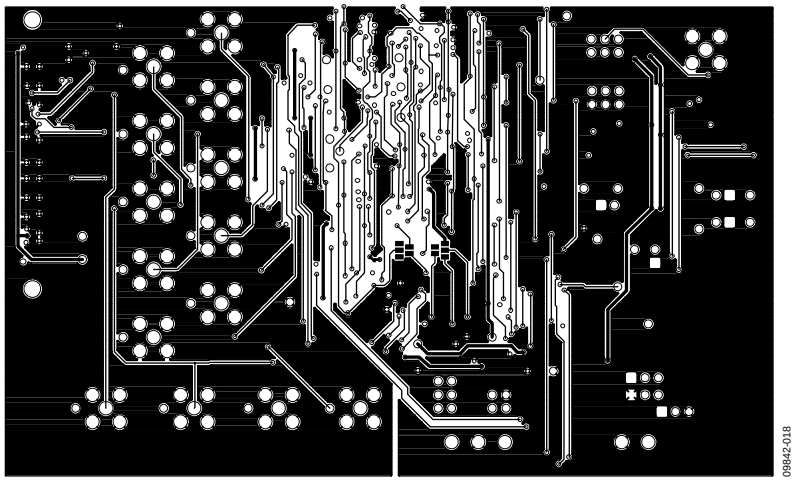

Figure 20. Solder Side PCB Drawing

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Qty	Reference Designator	Description	Supplier[1]/Part Number
1	C1	10 nF capacitor, 0805	FEC 1692285
4	C2, C4, C25, C26	0.1 µF capacitor, 0603	FEC 138-2224
1	C3	1 µF capacitor, 0402	FEC 1288253
2	C24, C27	10 µF capacitor, 1206	FEC 1611967
1	D6	LED, green	FEC 579-0852
1	J1	3-pin connector	FEC 151790
1	J2	2-pin connector	FEC 151789
1	J22	Receptacle, 0.6 mm, 120 way	Digi-Key H1219-ND
4	A20, A21, A24, A25	Header, 2-row, 36 + 36 way, and jumper socket, black	FEC 148-535 and FEC 150-410
3	A27, A29, A30	Header, 1-row, 3-way, and jumper socket, black	FEC 102-2248 and FEC 150-410
4	BUF-W1, OAVOUT, BUF-3, BUF-4	Header, 1-row, 2-way, and jumper socket, black	FEC 102-2247 and FEC 150-410
1	R41	1.78 kΩ resistor, 0603, 1%	FEC 1170811
2	R1, R2	2.2 kΩ resistor, 0603, 1%	FEC 933-0810
5	R3, R4, R38, R39, R40	2.7 kΩ resistor, 1206, 1%	FEC 9337288
1	R34	4.7 kΩ resistor, 0603, 1%	FEC 9331247
35	AD5162-1, AD5162-2, AD5172-1, AD5172-2, AD5204-1, AD5204-2, AD5204-3, AD5204-4, AD5222-1, AD5222-2, AD5232-1, AD5232-2, AD5233-1, AD5233-2, AD5233-3, AD5233-4, ADN2850-1, ADN2850-2, AD5243-1, AD5243-2, AD5252-1, AD5252-2, ADN2850-1, ADN2850-2, ADN2850-3, ADN2850-4, AD8403-1, AD8403-2, AD8403-3, AD8403-4, ADN2850-1, ADN2850-2, R35, R42, R43	0 Ω resistor, 0603	FEC 9331662
1	R37	1 kΩ resistor, 0603, 1%	FEC 933-0380
6	3.3 V, 5 V, DGND, AGND, VDD, VSS	Test point, PCB, black, PK100	FEC 873-1128
35	A1, A2, A3, A4, RDY|MODE, RESET_BF, SCL_BF, SCLK_BF, SDA_BF, SDO_BF, SHDN_BF, SYNC_BF, MUX-A0|CS, MUX-A1|DACSEL, MUX-A2|U/D, O1, O2, DIN_BF, CLK, B1, B2, B3, B4, V1, V2, VOUT, VOUT2, VOUT3, VOUT4, W1, W1_BUF, W2, W3, W4, WP_BUF	Test point, PCB, red, PK100	FEC 873-1144
1	U1	AD5243	Analog Devices AD5243
1	U2	AD5162	Analog Devices AD5162
1	U3	AD5172	Analog Devices AD5172
1	U4	AD5233	Analog Devices AD5233
1	U5	AD5222	Analog Devices AD5222
1	U6	AD8403	Analog Devices AD8403
1	U7	ADN2850	Analog Devices ADN2850
1	U8	AD5204	Analog Devices AD5204
1	U9	AD5252	Analog Devices AD5252
1	U10	AD5232	Analog Devices AD5232
1	U11	ADN2850	Analog Devices ADN2850
1	U12	ADN2850	Analog Devices ADN2850
1	U13	ADG3247	Analog Devices ADG3247
1	U14	AD8618	Analog Devices AD8618
1	U15	AD8652	Analog Devices AD8652
1	A22	ADG658	Analog Devices ADG658
1	U25	24LC64	FEC 975-8070

[1] FEC refers to Farnell Electronic Component Distributors; Digi-Key refers to Digi-Key Corporation.

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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