

# Power Modules, Passivated Assembled Circuit Elements, 25 A



PACE-PAK (D-19)

PRIMARY CHARACTERISTICS				
l <sub>O</sub> 25 A				
Type	Modules - thyristor, standard			
Package	PACE-PAK (D-19)			

#### **FEATURES**

- · Glass passivated junctions for greater reliability
- · Electrically isolated base plate
- Available up to 1200 V<sub>RRM</sub>/V<sub>DRM</sub>
- High dynamic characteristics
- · Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### **DESCRIPTION**

The VS-P100 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
Io	85 °C	25	A		
1	50 Hz	357	^		
ITSM	60 Hz	375	Α		
l <sup>2</sup> t	50 Hz	637	A <sup>2</sup> s		
	60 Hz	580	A-5		
I <sup>2</sup> √t		6365	A <sup>2</sup> √s		
V <sub>DRM</sub> , V <sub>RRM</sub>		400 to 1200	V		
V <sub>ISOL</sub>		2500	V		
T <sub>J</sub>	Range	-40 to +125	°C		
T <sub>Stg</sub>		-40 to +125	°C		

#### **ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS			
TYPE NUMBER	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> MAXIMUM AT T <sub>J</sub> MAXIMUM mA
VS-P101, VS-P121, VS-P131	400	500	
VS-P102, VS-P122, VS-P132	600	700	
VS-P103, VS-P123, VS-P133	800	900	10
VS-P103, VS-P124, VS-P134	1000	1100	
VS-P105, VS-P125, VS-P135	1200	1300	



PARAMETER	SYMBOL		TEST CON	DITIONS	VALUES	UNITS
PANAIVIETEN	STIVIBUL		1EST CON	OHIONO		
Maximum DC output current at case temperature	Io	Full bridge			25 85	°C
		t = 10 ms	No voltage	No voltage		
Maximum peak, one-cycle non-repetitive	I <sub>TSM</sub> ,	t = 8.3 ms	reapplied		375	
on-state or forward current	I <sub>FSM</sub>	t = 10 ms	100 % V <sub>RBM</sub>		300	Α
		t = 8.3 ms	reapplied	Sinusoidal half wave,	315	
		t = 10 ms	No voltage	initial $T_J = T_J$ maximum	637	- A <sup>2</sup> s
Maximum I <sup>2</sup> t for fusing	l <sup>2</sup> t	t = 8.3 ms	reapplied		580	
		t = 10 ms	100 % V <sub>RBM</sub>		450	
		t = 8.3 ms	reapplied		410	
Maximum I²√t for fusing	I²√t	$t=0.1$ ms to 10 ms, no voltage reapplied $I^2t$ for time $tx=I^2\sqrt{t}\cdot\sqrt{t}x$		6365	A²√s	
Maximum value of threshold voltage	V <sub>T(TO)</sub>	T <sub>J</sub> = 125 °C		0.82	V	
Maximum level value of on-state slope resistance	r <sub>t1</sub>	$T_J = 125 ^{\circ}\text{C}$ , average power = $V_{T(TO)} \times I_{T(AV)} + r_t + (I_{T(RMS)})^2$		12	mΩ	
Maximum on-state voltage drop	$V_{TM}$	$I_{TM} = \pi \times I_{T(AV)}$ $T_J = 25  ^{\circ}C$		1.35	V	
Maximum forward voltage drop	$V_{FM}$	$I_{FM} = \pi \times I_{F(AV)}$ $T_J = 25  ^{\circ}C$		1.35	V	
Maximum non-repetitive rate of rise of turned-on current	dl/dt	$T_J = 125$ °C from 0.67 $V_{DRM}$ $I_{TM} = \pi \times I_{T(AV)}, I_q = 500$ mA, $t_r < 0.5 \mu s, t_p > 6 \mu s$		200	A/μs	
Maximum holding current	I <sub>H</sub>	T <sub>J</sub> = 25 °C a	node supply = 6	V, resistive load, gate open	130	mΛ
Maximum latching current	ΙL	T <sub>J</sub> = 25 °C anode supply = 6 V, resistive load		250	mA	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T <sub>J</sub> = 125 °C, exponential to 0.67 V <sub>DRM</sub> gate open	200	V/µs
Maximum peak reverse and off-state leakage current at V <sub>RRM</sub> , V <sub>DRM</sub>	I <sub>RRM</sub> , I <sub>DRM</sub>	T <sub>J</sub> = 125 °C, gate open circuit	10	mA
Maximum peak reverse leakage current	I <sub>RRM</sub>	T <sub>J</sub> = 25 °C	100	μA
RMS isolation voltage	V <sub>ISOL</sub>	50 Hz, circuit to base, all terminals shorted, $T_J = 25$ °C, $t = 1$ s	2500	V

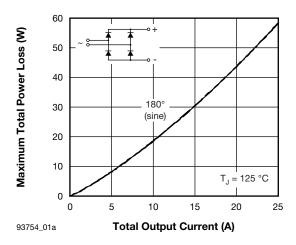
TRIGGERING					
PARAMETER	SYMBOL	TEST CO	NDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$			8	W
Maximum average gate power	P <sub>G(AV)</sub>			2	VV
Maximum peak gate current	I <sub>GM</sub>			2	Α
Maximum peak negative gate voltage	-V <sub>GM</sub>			10	V
		T <sub>J</sub> = -40 °C		3	
Maximum gate voltage required to trigger	V <sub>GT</sub>	T <sub>J</sub> = 25 °C	Anode supply =	2	V
		T <sub>J</sub> = 125 °C		1	·
		T <sub>J</sub> = -40 °C	6 V resistive load	90	
Maximum gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C	]	60	mA
		T <sub>J</sub> = 125 °C		35	
Maximum gate voltage that will not trigger	$V_{GD}$	T 105 °C material V annulised		0.2	V
Maximum gate current that will not trigger	I <sub>GD</sub>	T <sub>J</sub> = 125 °C, rated V <sub>DRM</sub> applied		2	mA



THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		-40 to +125	°C
Maximum thermal resistance, junction to case per junction	R <sub>thJC</sub>	DC operation	2.24	K/W
Maximum thermal resistance, case to heatsink	R <sub>thCS</sub>	Mounting surface, smooth and greased	0.10	r√ vv
Mounting torque, base to heatsink (1)			4	Nm
Approximate weight			58	g
Approximate weight			2.0	OZ.
Case style			PACE-PA	AK (D-19)

#### Note

<sup>(1)</sup> A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound



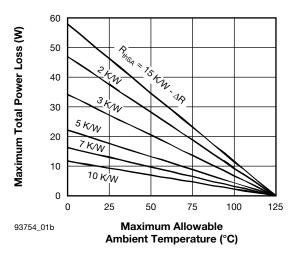


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

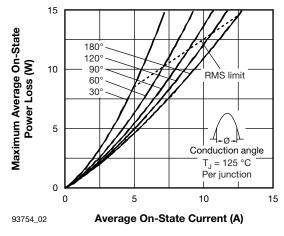


Fig. 2 - On-State Power Loss Characteristics

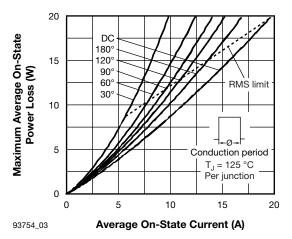


Fig. 3 - On-State Power Loss Characteristics



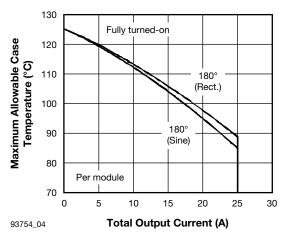


Fig. 4 - Current Ratings Characteristics

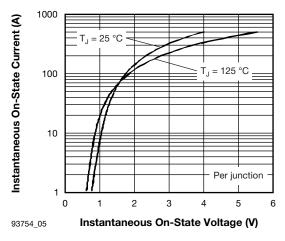


Fig. 5 - On-State Voltage Drop Characteristics

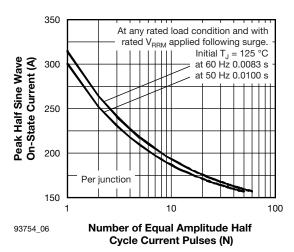


Fig. 6 - Maximum Non-Repetitive Surge Current

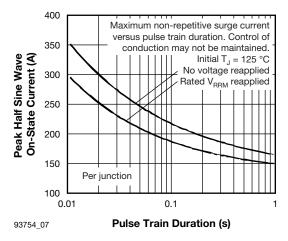


Fig. 7 - Maximum Non-Repetitive Surge Current

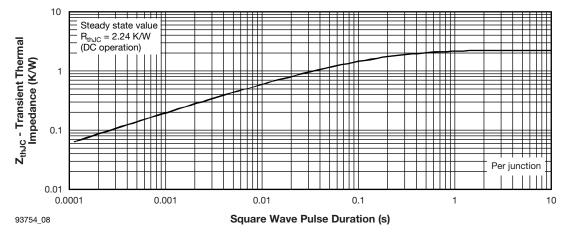


Fig. 8 - Thermal Impedance Z<sub>thJC</sub> Characteristics



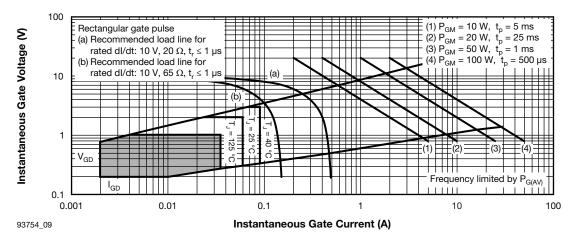
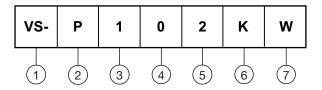


Fig. 9 - Gate Characteristics

#### **ORDERING INFORMATION TABLE**

**Device code** 



- Vishay Semiconductors product
- 2 Module type
- Current rating
  - 1 = 25 A DC (P100 series)
  - 4 = 40 A DC (P400 series)
- 4 Circuit configuration
  - 0 = single phase, hybrid bridge common cathode
  - 2 = single phase, hybrid bridge doubler connection
  - 3 = single phase, all SCR Bridge
- 5 Voltage code
  - 1 = 400 V
  - 2 = 600 V
  - 3 = 800 V
  - 4 = 1000 V
  - 5 = 1200 V
- 6 K = optional voltage suppression
- 7 W = optional freewheeling diode



CIRCUIT CONFIGURATION				
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	SCHEMATIC DIAGRAM	TERMINAL POSITIONS	
Single phase, hybrid bridge common cathode	0	AC20 (+)	AC1 G1 - AC2 G2 +	
Single phase, hybrid bridge doubler connection	2	G1 9 9 G2 AC2 AC1 (+)	AC1 G1 - AC2 G2 +	
Single phase, all SCR bridge	3	G3 9 G1 AC10 AC20 G4 G2 (+)	AC2 G2 - G1 G4 - AC1 G3 +	

CODING (1)						
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	BASIC SERIES	WITH VOLTAGE SUPPRESSION	WITH FREEWHEELING DIODE	WITH BOTH VOLTAGE SUPPRESSION AND FREEWHEELING DIODE	
Single phase, hybrid bridge common cathode	0	P10.	P10.K	P10.W	P10.KW	
Single phase, hybrid bridge doubler connection	2	P12.	P12.K	-	-	
Single phase, all SCR bridge	3	P13.	P13.K	-	-	

#### Note

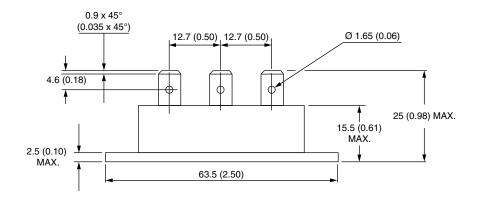
<sup>(1)</sup> To complete code refer to Voltage Ratings table, i.e.: for 600 V P10.W complete code is P102W

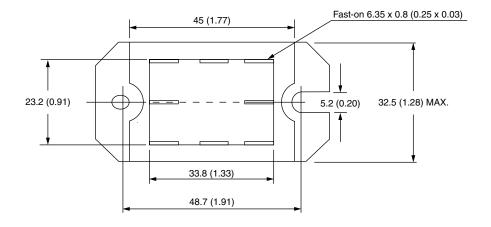
LINKS TO RELAT	ED DOCUMENTS
Dimensions	www.vishay.com/doc?95335



## **D-19 PACE-PAK**

#### **DIMENSIONS** in millimeters (inches)







## **Legal Disclaimer Notice**

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