Title	***Engineering Prototype Report for EP48 – 1.4 W Non-Isolated Buck Converter Using LNK304P (LinkSwitch®-TN)***
Specification	85–265 VAC Input, 12 V, 120 mA, 1.44 W Output
Applications	Room Air Conditioners, White Goods, LED Lighting, and Other Applications Requiring a Non-Isolated Supply
Author	Power Integrations Applications Department
Document Number	EPR-48
Date	02-May-2005
Revision	1.1

Summary and Features

- Low cost, low component count solution (only 16 components)
- No optocoupler required
- Much higher output current than “reactive dropper” type power supplies
- High efficiency (>69% over full input voltage range)
- Less than 1 W input power with 0.5 W load
- Low no-load consumption (<0.2 W at 265 VAC)
- Fully protected against open-loop faults, output overload, short circuit and thermal overload
- Low-cost input stage meets EMI and surge requirements

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Important Note:
Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. In addition, as the output is not electrically isolated from the input, all testing should be performed using an isolation transformer to provide the AC line input to the prototype board.

1 Introduction

This document is an engineering report describing a non-isolated 12 V, 120 mA power supply utilizing a LNK304. This power supply is intended as a general purpose evaluation platform for *LinkSwitch-TN* in a buck converter configuration.

The document contains the power supply specification, schematic, bill of materials, printed circuit layout, and performance data.

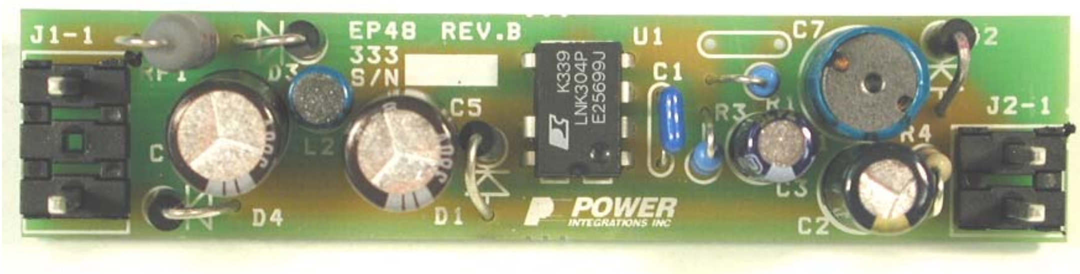

Figure 1 – EP48 Populated Circuit Board Photograph.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – No Protective Earth
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.3	W	
Output						
Output Voltage 1	V_{OUT}	10.8	12.0	13.2	V	±10%
Output Ripple Voltage 1	$V_{RIPPLE1}$			120	mV	20 MHz Bandwidth
Output Current 1	I_{OUT}	0		120	mA	3.5 mA pre-load fitted on board
Total Output Power						
Continuous Output Power	P_{OUT}		1.44		W	
Standby Input Power	$P_{IN (S/B)}$			1	W	0.5 W output load
Efficiency	η	70			%	Measured at 85 VAC, 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				> 6 dB Margin
Surge		4			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode 2 Ω Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	-20		50/85	°C	Free convection, sea level. For operation at >70 °C substitute D1 for a diode with t_{rr} ≤35 ns

Table 1 - EP48 Specifications

3 Schematic

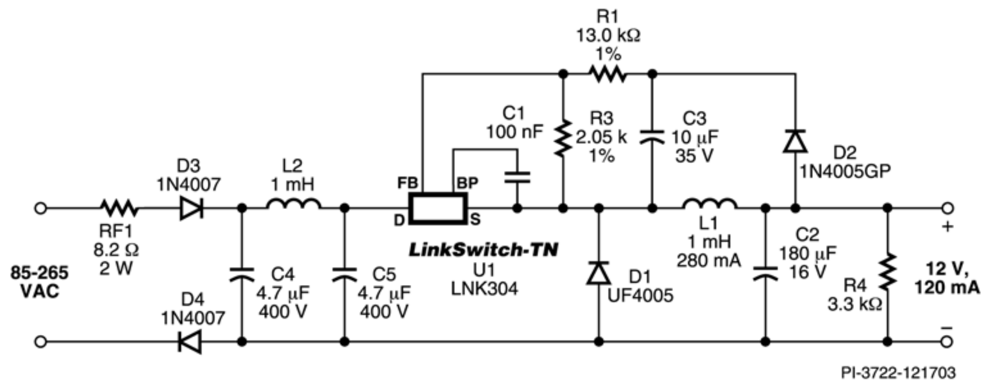

Figure 2 – EP48 Schematic.

4 Circuit Description

4.1 Input Stage and EMI Filtering

The input stage is comprised of fusible resistor RF1, diodes D3 and D4, capacitors C4 and C5, and inductor L2. Two diodes are used to both increase the surge withstand to 2 kV and provide EMI gating (noise current only flows when the diodes conduct). Placing D3 and D4 directly in series would meet the surge requirements, but without EMI gating, conducted EMI on the neutral line would be higher.

Resistor RF1 is a flameproof, fusible, wire wound resistor. It accomplishes several functions: (a) limits inrush current to safe levels for rectifiers D3 and D4, (b) provides differential mode noise attenuation and (c) acts as an input fuse in the event any other component fails short circuit. As this component is used as a fuse, it should fail safely open circuit without emitting smoke, fire or incandescent material to meet typical safety requirements. To withstand the instantaneous inrush power dissipation, wire wound types are recommended. Metal film resistors are not recommended.

4.2 LinkSwitch-TN

LinkSwitch-TN integrates a 700 V power MOSFET and control circuitry into a single low cost IC. The internal fixed switching frequency of 66 kHz was selected to allow up to 120 mA of output current using a standard 1 mH inductor. Lower frequencies require higher value, more costly inductors while higher frequencies increase EMI and cause undesirable high di/dt values as the inductor value reduces.

The device is completely self-powered from the DRAIN pin with local supply decoupling provided by a small 100 nF capacitor connected to the BYPASS pin.

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Here, the device is configured in a buck converter. The supply is designed to operate in mostly discontinuous conduction mode (MDCM), with the peak L1 inductor current set by the LNK304P internal current limit. The control scheme used is similar to the ON/OFF control used in *TinySwitch®*. The on-time for each switching cycle is set by the inductance value of L1, *LinkSwitch-TN* current limit and the high voltage DC input bus across C5.

Output regulation is accomplished by skipping switching cycles in response to an ON/OFF feedback signal applied to the FEEDBACK (FB) pin. This differs significantly from traditional PWM schemes that control the duty factor (duty cycle) of each switching cycle.

Unlike *TinySwitch,* the logic of the FB pin has been inverted in *LinkSwitch-TN*. This allows a very simple feedback scheme to be used when the device is used in the buck converter configuration. Current into the FB pin greater than 49 μA will inhibit the switching of the internal MOSFET, while current below this allows switching cycles to occur.

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, *LinkSwitch-TN* enters into auto-restart operation. If no feedback is received for >50 ms, the internal MOSFET is disabled for 800 ms and auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed and feedback is received.

4.3 Output Rectification

During the ON time of U1, current ramps in L1 and is simultaneously delivered to the load. During the OFF time the inductor current ramps down via free-wheeling diode D1 into C2 and is delivered to the load. Diode D1 should be selected as an ultra-fast diode ($t_{rr} \leq$50 ns) with a voltage rating greater than the maximum DC voltage across C5, 600 V in this case. In designs that operate in continuous conduction mode, t_{rr} of ≤35 ns is recommended. Capacitor C2 should be selected to have an adequate ripple current rating (low ESR type).

4.4 Output Feedback

The voltage across L1 is rectified and smoothed by D1 and C2 during the off-time of U1. To a first order, the forward voltage drops of D1 and D2 are identical and therefore, the voltage across C3 tracks the output voltage. To provide a feedback signal, the voltage developed across C3 is divided by R1 and R3 and connected to U1's FB pin. The values of R1 and R3 are selected such that at the nominal output voltage, the voltage on the FB pin is 1.65 V. This voltage is specified for U1 at an FB current of 49 μA with a tolerance of +/-7% over a temperature range of –40 to 125 °C. This allows this simple feedback to meet the required overall output tolerance of +/-10% at rated output current.

Operation down to 0 mA output current can be accomplished while still meeting +/-10% by increasing the size of the preload from 3.5 mA to 5 mA.

4.5 Operation Below Minimum Drain Voltage Specification

In certain abnormal conditions, the drain voltage can drop below the minimum drain voltage specification of 50 V. If these conditions exist in combination with very light output loading (<5 mA), it is possible for the output voltage to go out of regulation.

These abnormal conditions can exist, for example, during a brownout condition when the input voltage can drop to <30 VAC. To avoid the output voltage exceeding acceptable levels under these conditions, the output of the power supply has to either be pre-loaded with 5 mA or the output has to be clamped with an appropriate Zener diode (e.g. 15 V, 1.3 W device).

5 PCB Layout

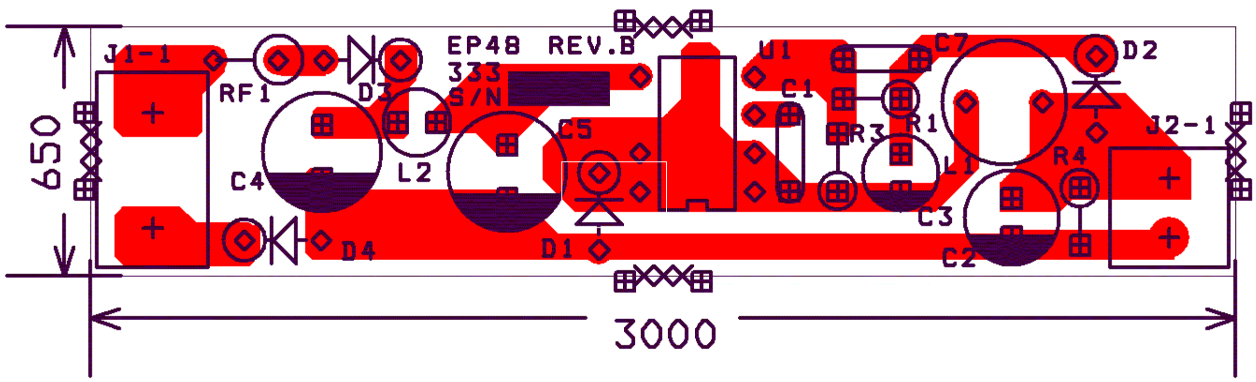

Figure 3 – EP48 Printed Circuit Layout (Dimension 0.001 Inches).

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6 Bill Of Materials

Item	Qty	Reference	Description	P/N	Manufacturer
1	2	C4, C5	4.7 μF, 400 V, 8mm x 11 mm	380VB4R7M8X11LL	UCC
2	1	C1	0.1 μF, 50 V, ceramic	ECU-S1H104KBB	Panasonic
3	1	C3	10 μF, 35 V general purpose	ECA-1VM100	Panasonic
4	1	C2	180 μF, 16 V, low ESR 250 mΩ, 400 mA	EEU-FC1C181	Panasonic
5	2	D3, D4	1 A, 1000 V, plastic rectifier	1N4007	Diodes Inc (or Generic)
6	1	D1	1 A, 600 V, Ultra Fast ($t_{rr} \leq$50 ns)	UF4005	General Semiconductor (or Generic)
7	1	D2	1A, 600 V, glass passivated rectifier (t_{rr} = 2 μs)	1N4005GP	General Semiconductor (or Generic)
8	1	L1	1 mH inductor 0.28 A	SBC3-102-281	Tokin
9	1	L2	1 mH inductor 0.21 A	SBC1-102-211	Tokin
10	1	R3	2.05 kΩ, 0.25 W, 1%	MFR-25FBF-2K05	Yageo (or generic)
11	1	R1	13.0 kΩ, 0.25 W, 1%	MFR-25FBF-13K	Yageo (or generic)
12	1	R4	3.3 kΩ, 0.25 W, 5%	CFR-25JB-3K3	Yageo (or generic)
13	1	RF1	8.2 Ω wire wound fusible, 2 W	CRF0414-253-4 8R2	VTM
14	1	U1	*LinkSwitch-TN*	LNK304P	Power Integrations
15	1	J1	3-pin connector (center pin removed)	26-48-1031	Molex
16	1	J2	2-pin connector	26-48-1021	Molex

7 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

7.1 Efficiency

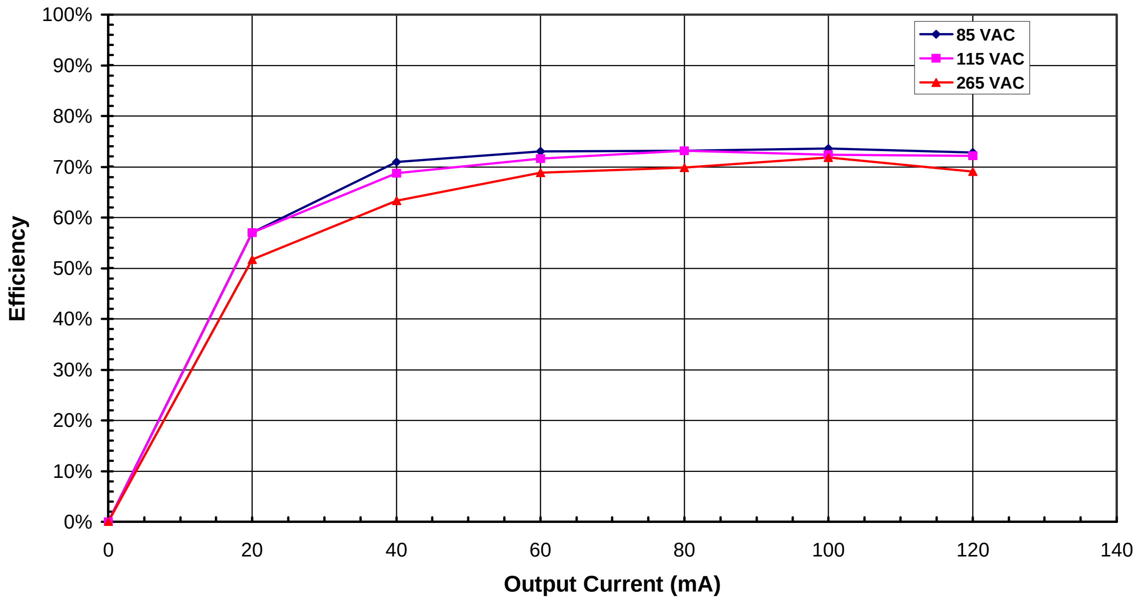

Figure 4 - Efficiency vs. Output Current, Room Temperature, 60 Hz.

7.2 No-load Input Power

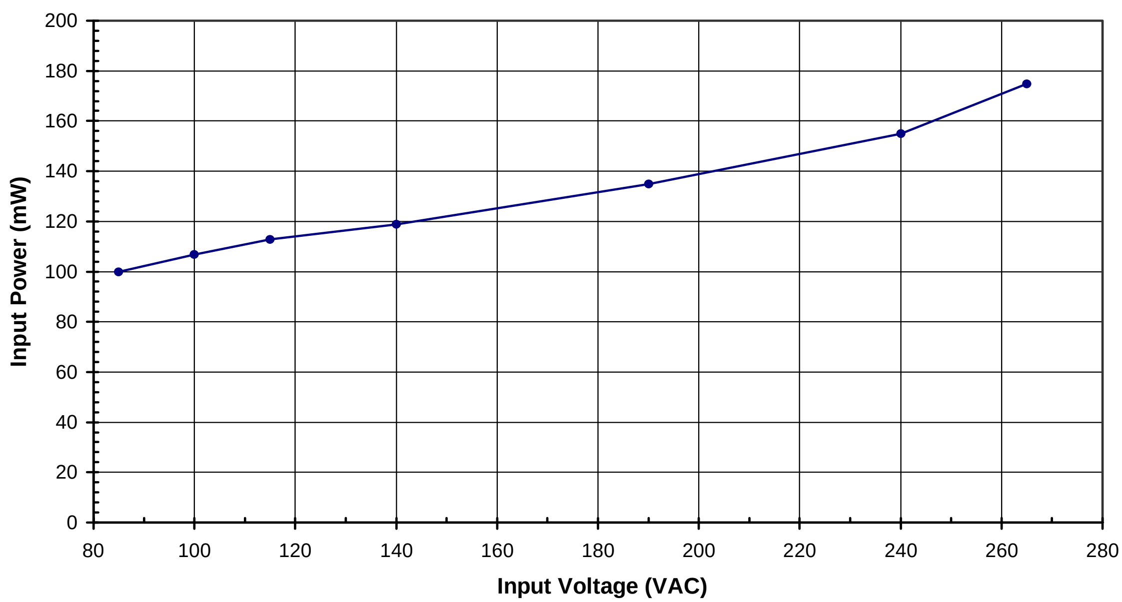

Figure 5 - Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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7.3 Regulation

7.3.1 Load

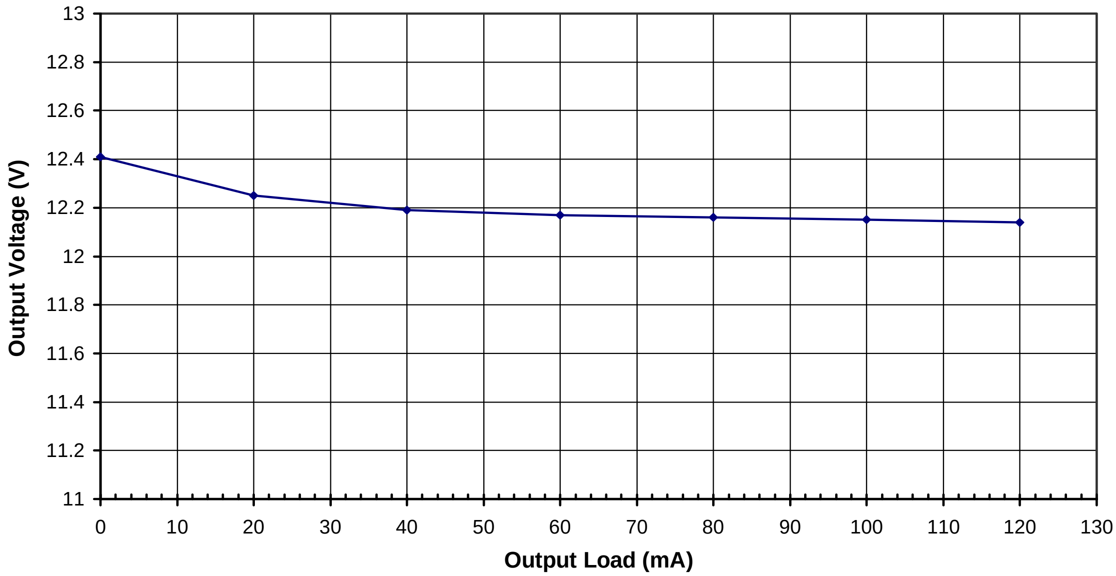

Figure 6 - Load Regulation, Room Temperature.

7.3.2 Line

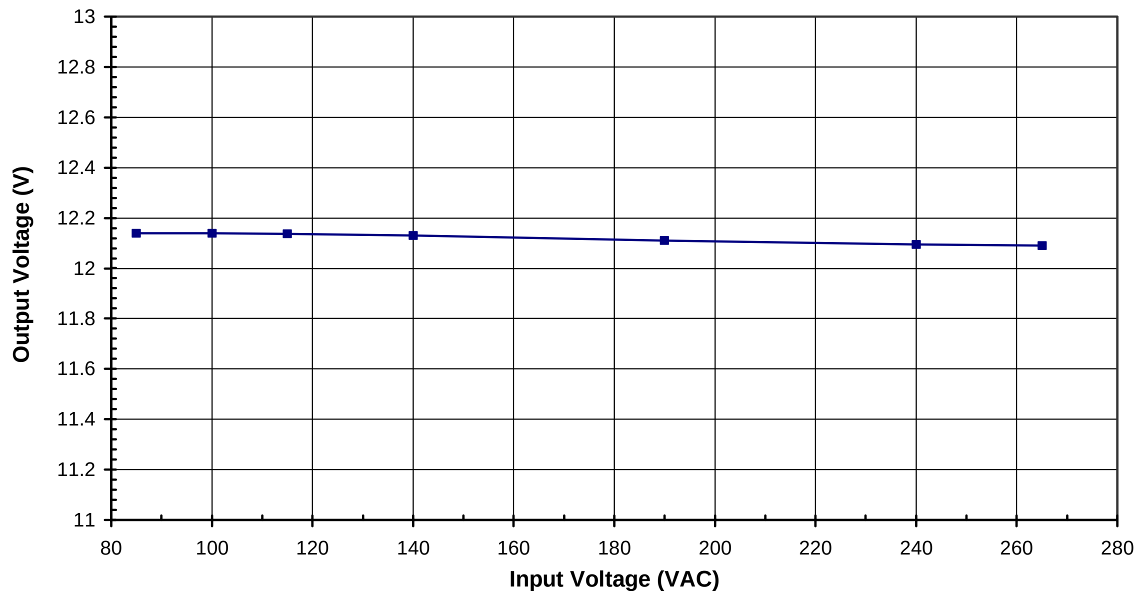

Figure 7 - Line Regulation, Room Temperature, Full Load.

7.4 *Thermal Performance*

To verify acceptable thermal performance, thermocouples were placed on key components on the board and the unit was placed into a thermal chamber. The ambient was raised to 85 °C with no air flow over the board. The unit was fully loaded and allowed to stabilize at three different line voltages, at which point temperature measurements were recorded.

In addition, a thermal image was taken of a unit painted matte black, operating at full load, 85 VAC and an ambient temperature of 23 °C.

These results show very acceptable temperature rise figures and show that the unit can operate in a very high ambient with sufficient margin to thermal shutdown.

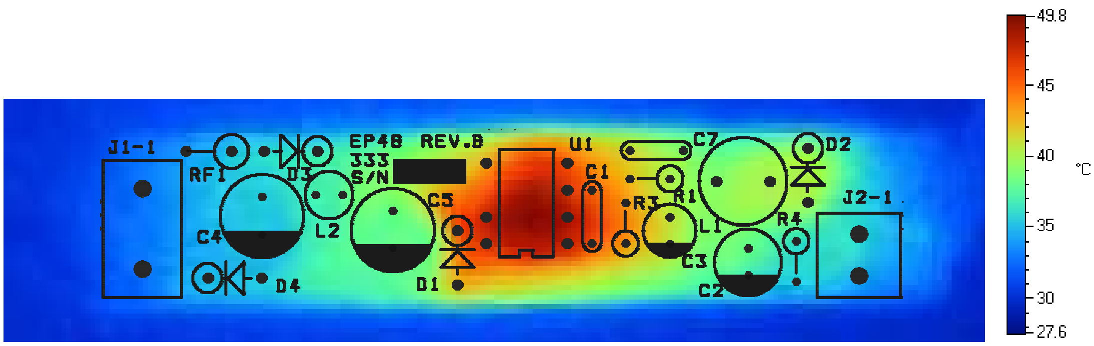

Figure 8 – Infrared Thermograph of EP48, 85 VAC Input, Full Load and 23 °C Ambient.

Temperature (°C)			
Item	**90 VAC**	**115 VAC**	**240 VAC**
Ambient	85	85	85
***LinkSwitch-TN* (U1)**	112	112	106
Output Inductor (L1)	102	103	105
Freewheeling Diode (D1)	103	103	107
Input Capacitor (C5)	95	92	90
Output Capacitor (C2)	90	90	91

Table 2 - Temperature of Key Components, 85 VAC, Full Load, 85 °C Ambient.

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8 Waveforms

8.1 Source Voltage and Current, Normal Operation

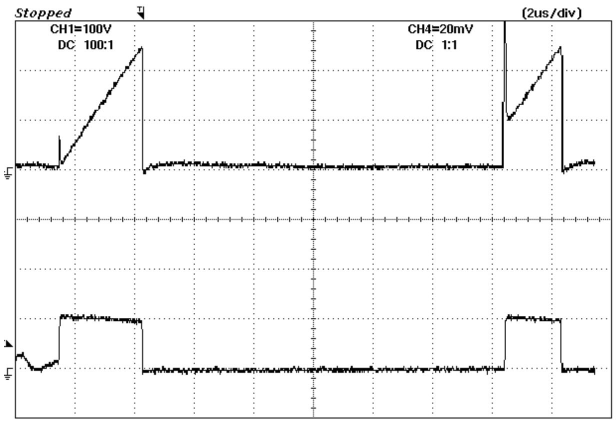

Figure 9 - 85 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div
Lower: V_{SOURCE}, 100 V, 2 μs / div

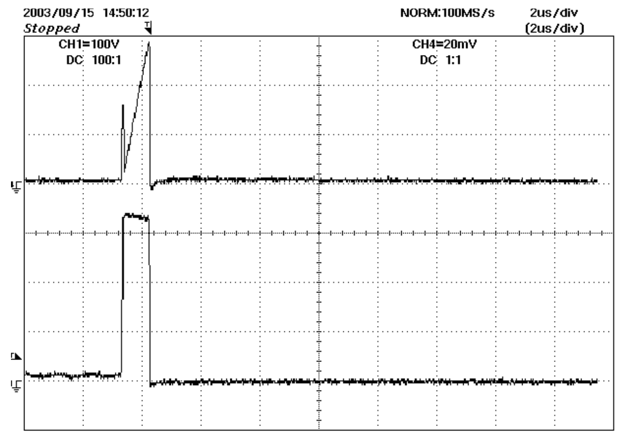

Figure 10 - 265 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div
Lower: V_{SOURCE}, 100 V / div

8.2 Source Voltage and Current Start-up Profile

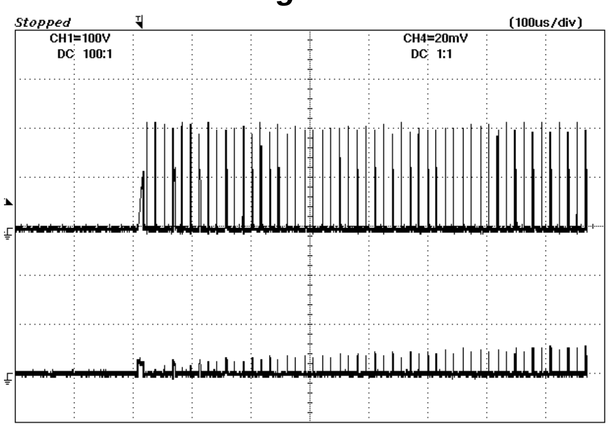

Figure 11 - 85 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.1 A / div
Lower: V_{SOURCE}, 100 V & 1 ms / div

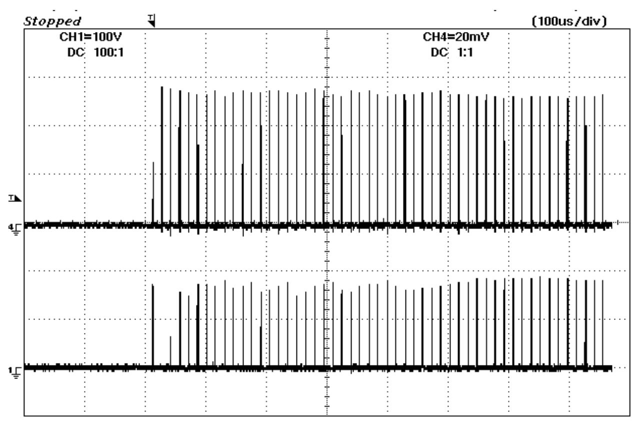

Figure 12 - 265 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.1 A / div
Lower: V_{SOURCE}, 100 V & 1 ms / div

8.3 Output Voltage Start-up Profile

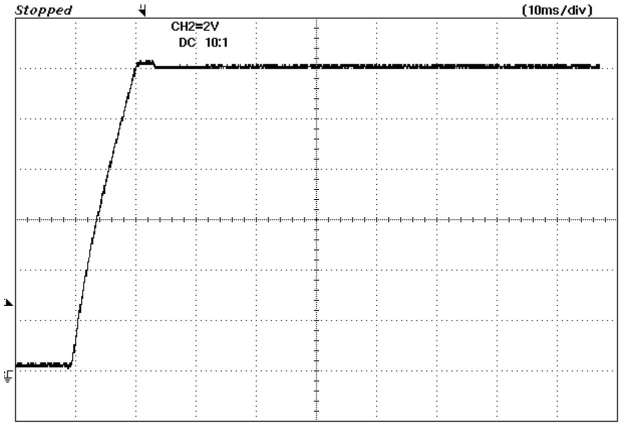

Figure 13 - 85 VAC Input and Maximum Load.
2 V / div, 10 ms

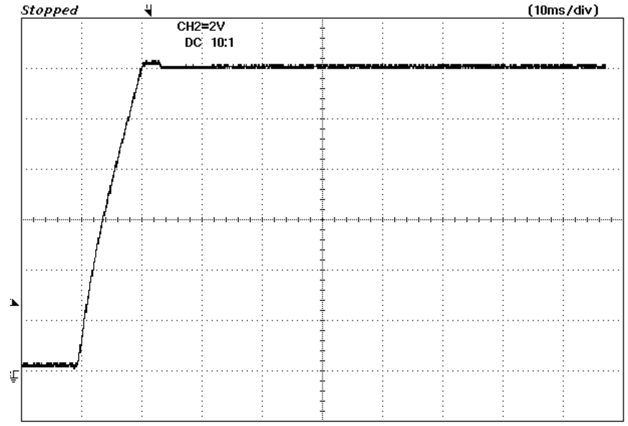

Figure 14 - 265 VAC Input and Maximum Load.
2 V / div, 10 ms

8.4 Load Transient Response (75% to 100% Load Step)

The oscilloscope was triggered using the load current step as a trigger source.

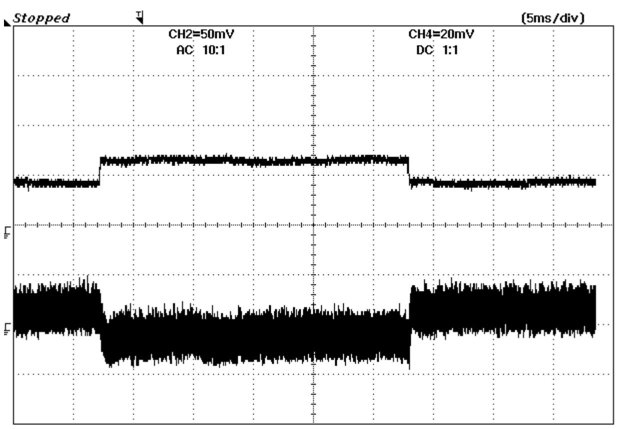

Figure 15 - 85 VAC Input and Maximum Load.
Upper: 100 mA / div
Lower: 50 mV / div, 5 ms / div

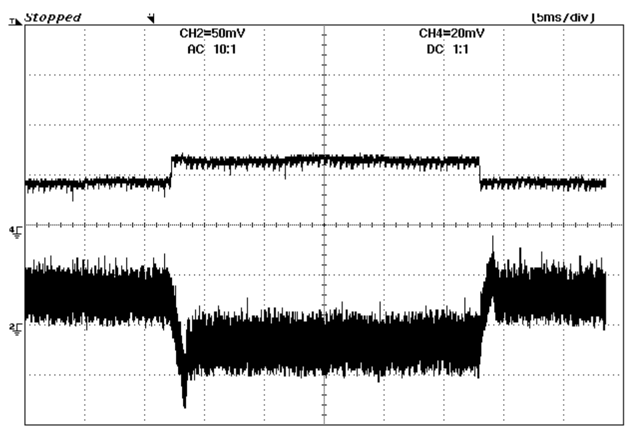

Figure 16 - 265 VAC Input and Maximum Load.
Upper: 100 mA / div
Lower: 50 mV / div, 5 ms / div

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8.5 Output Ripple Measurements

8.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 17 and Figure 18.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

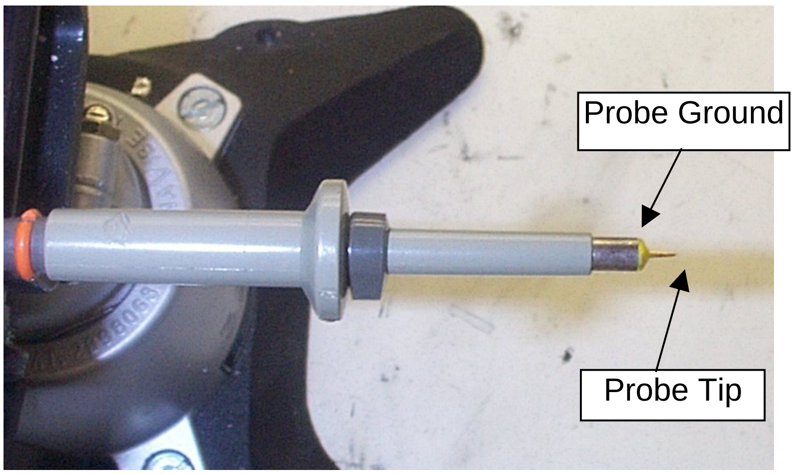

Figure 17 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed).

Figure 18 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement and Two Parallel Decoupling Capacitors Added).

8.5.2 Measurement Results

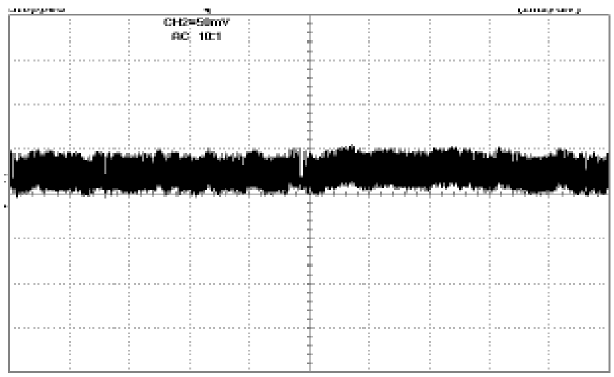

Figure 19 - Ripple, 85 VAC, Full Load.
2 ms, 50 mV / div

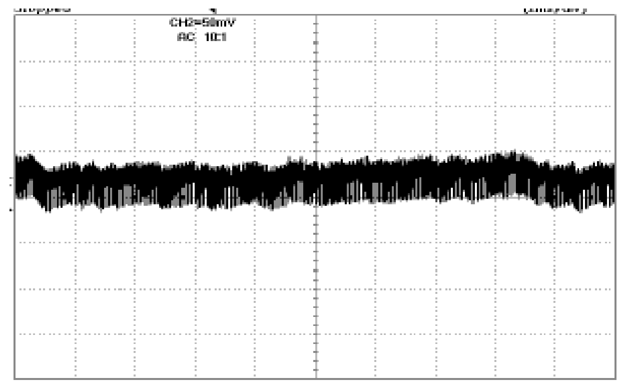

Figure 20 - 5 V Ripple, 115 VAC, Full Load.
2 ms, 50 mV / div

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9 Conducted EMI

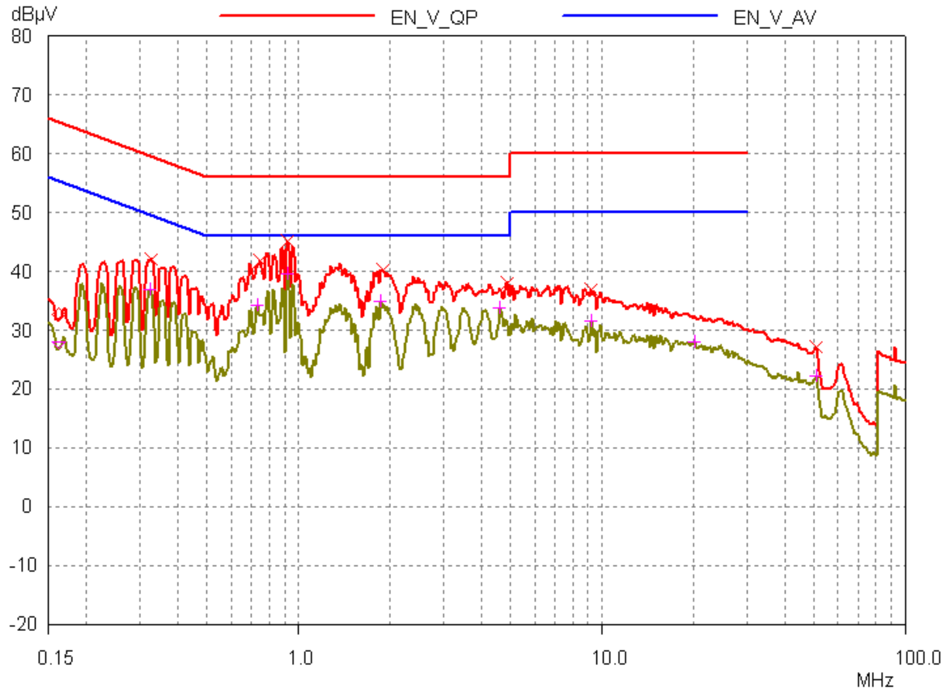

Figure 21 - Conducted EMI, 12 V Out, 120 mA, 115 VAC, 60 Hz, EN55022 B Limits, Neutral.

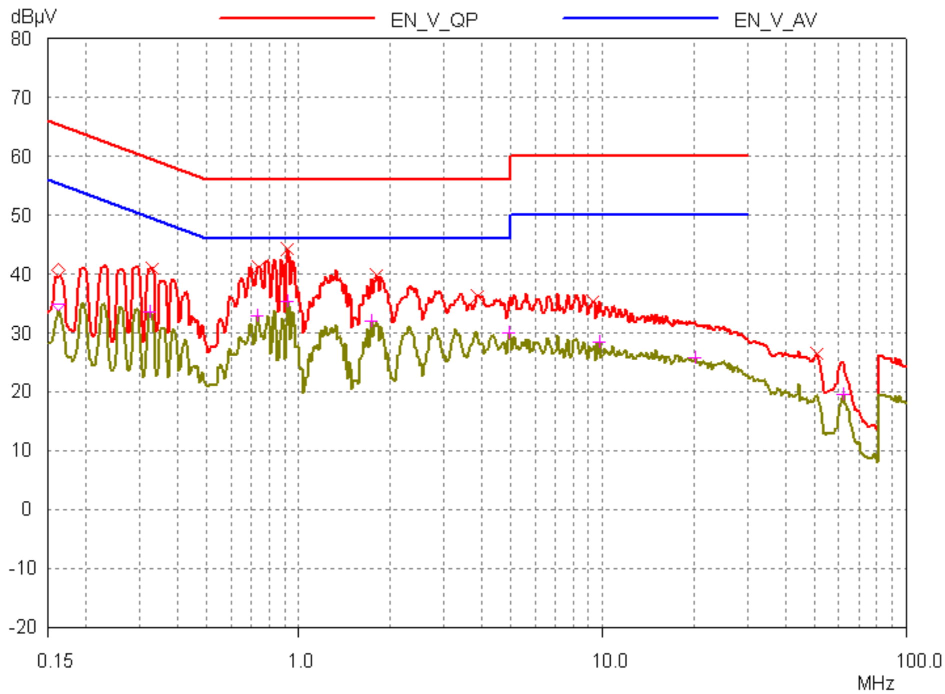

Figure 22 - Conducted EMI, 12 V Out, 120 mA, 115 VAC, 60 Hz, EN55022 B Limits, Line.

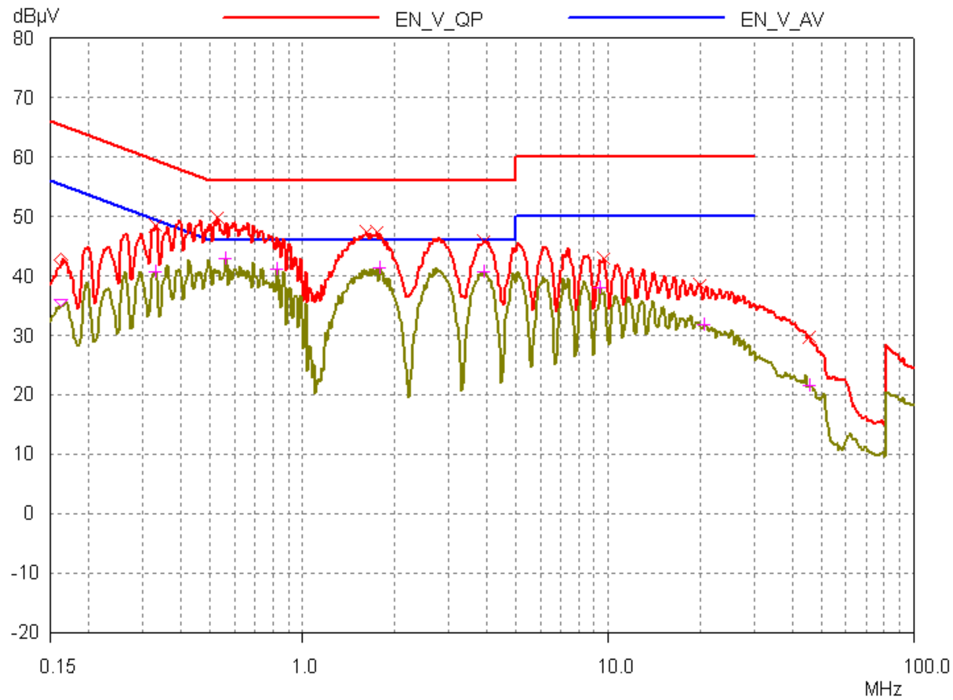

Figure 23 - Conducted EMI, 12 V Out, 120 mA, 230 VAC, 60 Hz, EN55022 B Limits, Neutral.

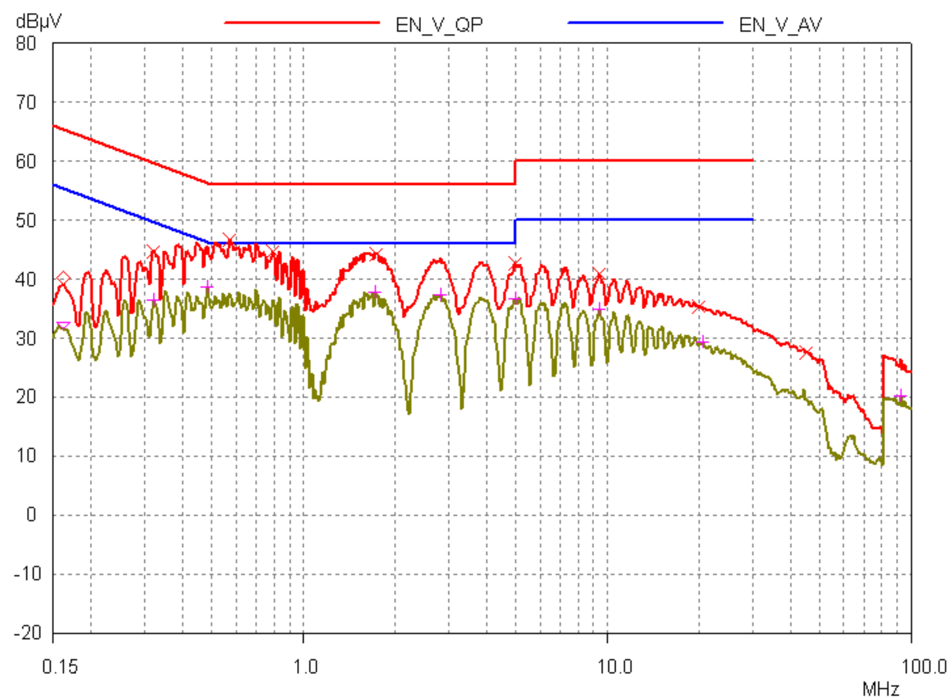

Figure 24 - Conducted EMI, 12 V Out, 120 mA, 230 VAC, 60 Hz, EN55022 B Limits, Line.

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10 Revision History

Date	Author	Revision	Description & changes
16-Sept-03	AO	0.1	First Draft
17-Sept-03	PV	0.2	2nd Draft
22-Sept-03	PV	0.3	3rd Draft
20-Nov-03	AO	0.4	4thDraft
22-Dec-03	PV	1.0	5th Draft
02-May-05	SK	1.1	Corrected scales in Figures 10 and 12

NOTES

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PATENT INFORMATION

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at *www.powerint.com*.

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