BD71815AGW

(Power Management IC designed for
“Freescale i.MX 7Solo and i.MX 7Dual Processors”)

Platfrom Design Guide

June 2017
Revision 1.30

Revision History

Revision Number	Description	Revision Date
1.00	Initial release	October 2016
1.10	Replaced Figure. 4-3-1-1 since pin name of A9 and B9 were modified as PGND1A and PGND1B	January 2017
1.20	Fixed typo	June 2017
1.30	Deleted the description of “Rohm confidential”	June 2017

Contents

1 Introduction

BD71815AGW is a Power Management Integrated Circuit (PMIC) for battery-powered portable devices. It integrates 5 Bucks, 8 LDOs, a boost driver for LED, 500mA single-cell linear charger, Coulomb counter, RTC, 32 kHz crystal circuitry and a GPO. And it is designed to support the specific power requirement of Freescale i.MX 7Solo and i.MX 7Dual platforms with minimum cost requirement.

The “BD71815AGW Platform Design Guide” provides design guideline which is recommended to PCB layer stack up, the components placement and the PCB routing. To reduce the risk that comes from PCB layout or parts placement, the guideline is strongly recommended to be adapted to the PCB design.

1.1 Terminology

Table 1-1-1. Acronyms, Conventions and Terminology

Term	Definition
BOM	Bill Of Materials
FET	Field Effect Transistor
I2C	Inter-Integrated Circuit
IRQ	Interrupt Request
LDO	Low Drop-Out regulator
OCP	Over Current Protection
OVP	Over Voltage Protection
PFM	Pulse-Frequency Modulation
PWM	Pulse-Width Modulation
RTC	Real-Time Clock
SoC	System-On-a-Chip
UVLO	Under Voltage-LockOut
DVS	Dynamic Voltage Scaling

1.2 Reference Documents

Table 1-1-2. Reference Documents

Document
BD71815AGW(EN)_Rev001, Oct, 2016

2 System Features

BD71815AGW is used to supply the required power to the SoC and peripheral devices. Once powered up, it can be controlled by I2C bus to determine internal settings. The following explains the features that are incorporated in the IC.

Voltage Rails

- 5 Buck regulators
  - BUCK1: Initial 1.100V, 0.800V – 2.000V / 25mV step DVS, I_{OMAX} = 800mA
  - BUCK2: Initial 1.000V, 0.800V – 2.000V / 25mV step DVS, I_{OMAX} = 1000mA
  - BUCK3: 1.800V, 1.200V – 2.700V / 50mV step programmable, I_{OMAX} = 500mA
  - BUCK4: 1.200V, 1.000V – 1.850V / 50mV step programmable, I_{OMAX} = 1000mA
  - BUCK5: 3.300V, 1.800V – 3.300V / 50mV step programmable, I_{OMAX} = 1000mA

- 3 LDO regulators (General purpose)
  - LDO1: 3.3V, 0.8V – 3.3V / 50mV step programmable, I_{OMAX} = 100mA
  - LDO2: 3.3V, 0.8V – 3.3V / 50mV step programmable, I_{OMAX} = 100mA
  - LDO3: 3.3V, 0.8V – 3.3V / 50mV step programmable, I_{OMAX} = 50mA

- LDO for SD Card with dedicated enable terminal
  - LDO4: 3.3V, 0.8V – 3.3V / 50mV step programmable, I_{OMAX} = 400mA

- LDO for SD Card Interface with dedicated terminal to dynamically change output voltage
  - LDO5: 1.8V / 3.3V, 0.8V – 3.3V / 50mV step programmable, I_{OMAX} = 250mA

- LDO for DDR Reference Voltage
  - VODVREF: DVREFIN/2, I_{OMAX} = 10mA

- LDO for Secure Non-Volatile Storage
  - SNVSC: 3.0V, I_{OMAX} = 25mA

- LDO for Low-Power State Retention
  - LDOLPSR: 1.8V, I_{OMAX} = 100mA

White LED Boost Converter

- ~ 25mA LED Boost Converter

Single-cell Linear LIB Charger with 30V OVP

- Selectable Charging Voltage: 3.72V – 4.34V
- Programmable Charge Current: 100mA – 500mA
- Support for up to 2000mA charge current using external MOSFET
- DCIN Over Voltage Protection
- Battery Over Voltage Protection
- Support Battery Supplement Mode
- Battery Short Circuit Detection

Voltage Measurement for Thermistor

- CHGREF: Bias Voltage Output for External Thermistor

Embedded Coulomb Counter for Battery Fuel Gauging

- 15-bit ΔΣ-ADC with External Current Sense Resistor (10 mΩ, ±1%)
- 1sec cycle, 28-bit Accumulation
- Coulomb Count while Charging/Discharging

Battery Monitoring and Alarm Output

- Under Voltage Alarm while Discharging
- Over Discharge Current Alarm
- Over/Under Temperature Alarm
- Programmable Thresholds and Time Durations

Real Time Clock with 32.768kHz Crystal Oscillator

- CLK32KOUT: 32.768kHz Clock Output (Open Drain or CMOS Output Selectable)

1 GPO

- GPO (Open Drain or CMOS Output Selectable)

Power Control I/O

- PWRON: Power ON/OFF Control Input
- STANDBY: Standby Input for Switching ON / STANDBY Mode
- RESETINB: Reset Input to Reset Hung PMIC
- POR: Power ON Reset Output

Serial Interface

- I2C interface provides access to configuration registers.

3 General Design Considerations

This chapter provides general PCB design guidelines such as BD71815AGW general parts placement.

3.1 Package Dimension of BD71815AGW

Figure 3-1-1 shows the package dimension of BD71815AGW.

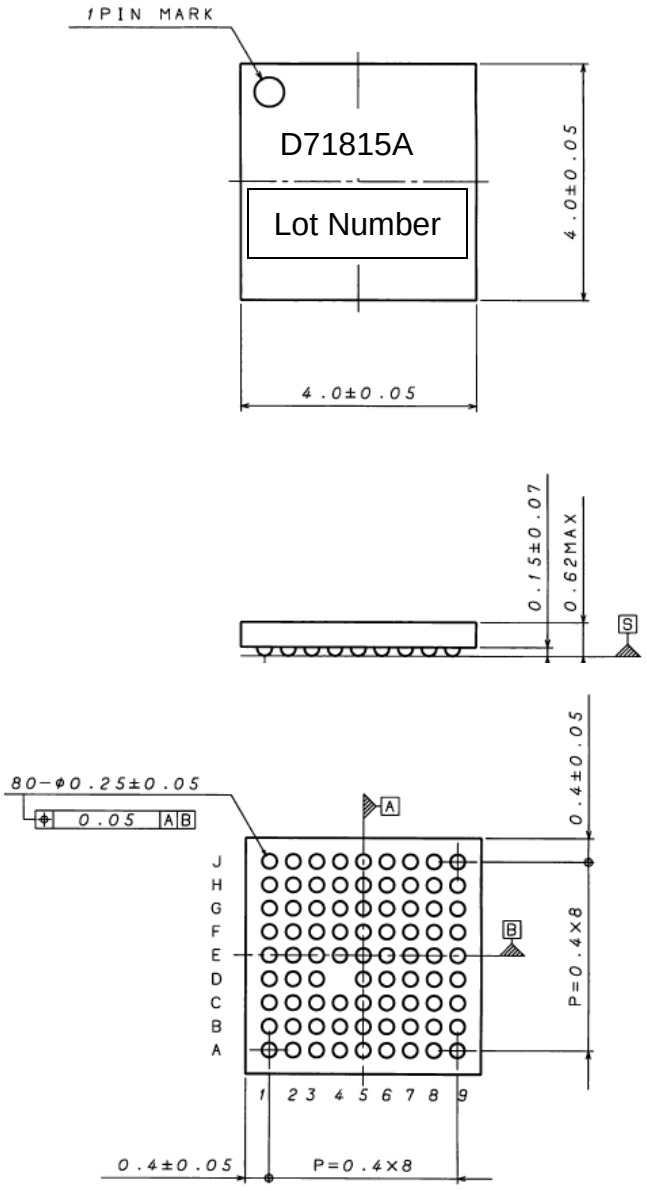

Figure 3-1-1 BD71815AGW Package Dimension

3.2 Pin Configuration

Figure 3-2-1 shows the BD71815AGW pin configuration with which signals from respective blocks are effectively routed out from PMIC to SoC, SDRAM, and other platform components.

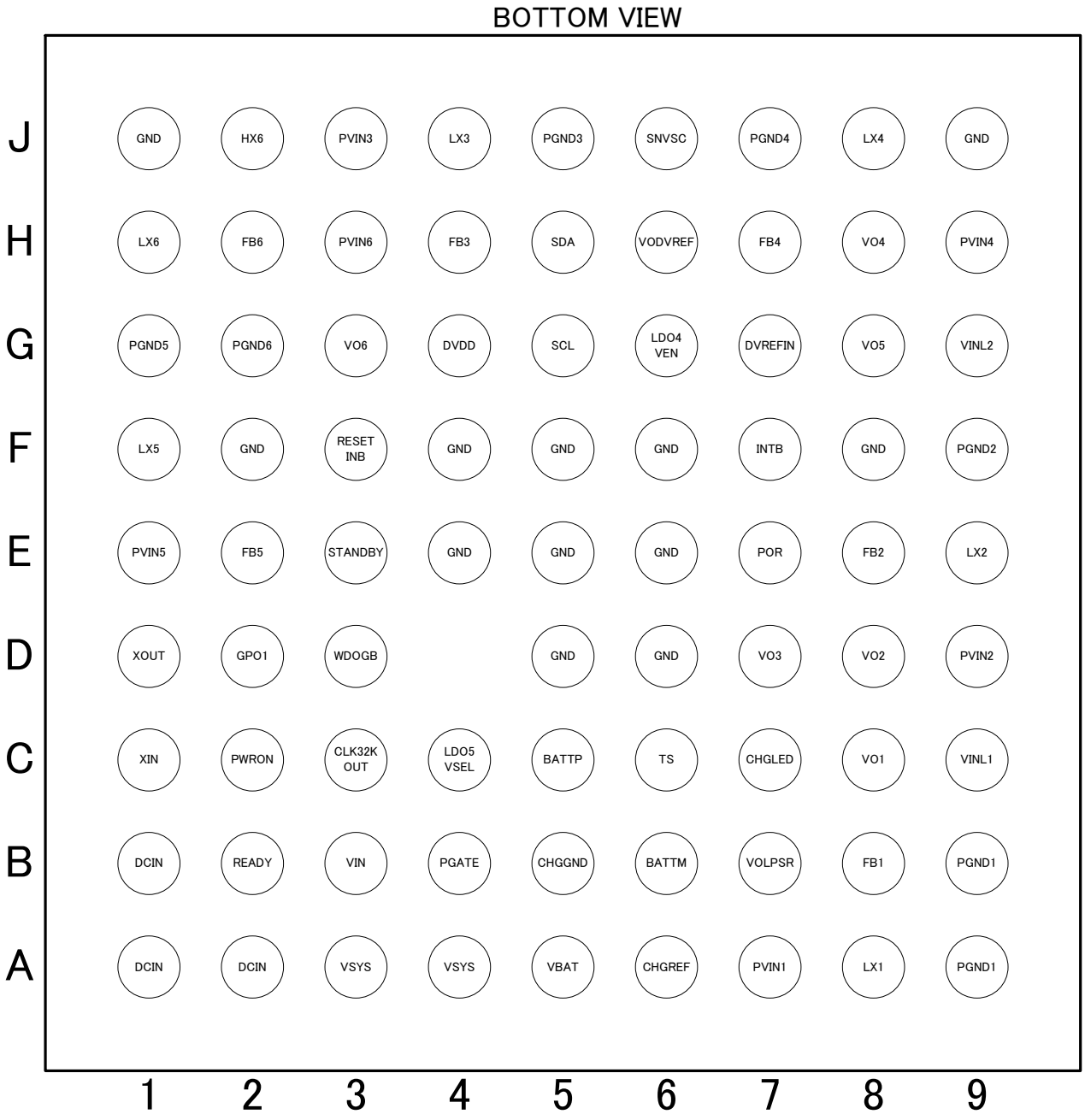

Figure 3-2-1 Pin Configuration

3.3 General Stack-up Recommendations

Type-4 and 6 layers PCB technology is used for BD71815AGW. The following general stack-up is strongly recommended to be applied to all the routings on the PCB.

- Surface plane layer are recommended to be 2.0 Mils thick copper.
- Internal plane layers are recommended to be 1.3 Mils thick copper.
- It is recommended that I2C signals have reference to solid planes over the length of their routing and do not cross plane splits. Ground is preferred as reference.
- PCB should be filled with as much ground or other power rails as possible with copper. There should not be any large areas with no metal in the board. Heat dissipation gets improved with larger metal areas. Large metal area also reduces stray resistance and inductance.

3.4 6-layer Board Stack-up

BD71815AGW Boards uses the PCB technologies of a high density interconnect, Type 4, 6-layer board. Figure 3-3-1 shows PCB 1-4-1 stack-up.

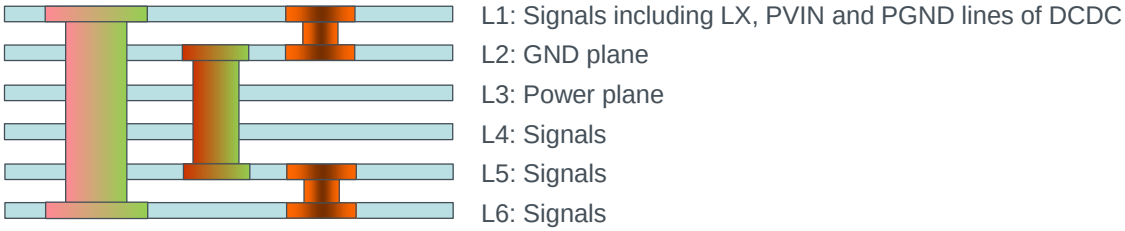

Figure 3-3-1 6-Layer PCB Stack-up

3.5 General PCB Pad Design Guidelines

The following guidelines are to improve mechanical robustness and solder joint reliability (SJR) of Pb-free SLI. The following guidelines are highly recommended to be followed for robust platform signal integrity.

3.5.1 Pad Size and Shape

1. The ratio of package solder resist opening (SRO) to PCB pad size must be less than 1:1.1. The pad size can be calculated by the package side SRO. First, the side package length is divided by 1.1 then the result is rounded up to the next whole number by mil.
   250/ 1.1 = 227.27 µm,
   227.27µml = 8.95 mils = ~9 mils
2. If SRO is not provided, the alternate method for calculating pad size is that the nominal ball diameter is multiplied by 0.8, then rounded up to the nearest whole mil.

3.6 Via Guidelines

This section explains proper via-drill, pad, and anti-pad size.

Note: Improper drill, pad, and anti-pad size may cause some trouble on the PCB cost, reliability, manufacturability, and electrical characteristics.

Type-3 PCB technology employs plated through-hole (PTH) vias for breakout routing. The dimension of PTH vias may vary as necessary. Table 3-6-1 shows the recommended via dimension used for the breakout areas of BD71815AGW. Figure 3-6-1 shows about the dimensions of via.

Type-4 PCB technology employs plated through-hole (PTH) vias and micro via holes (MVH) for breakout routing. Since the PTH vias are used in less space-constrained areas outside the BGA field, the dimension of PTH vias may vary as necessary. Table 3-6-1 shows the recommended via dimension used for the breakout areas of BD71815AGW. Figure 3-6-1 shows about the dimensions of via.

Table 3-6-1: Platform via Examples

Via type	Hole size	Pad size	Anti-Pad size
Micro via holes (MVH)	6 mil	12 mil	16 mil
Plated through-hole (PTH)	10 mil	22 mil	30 mil

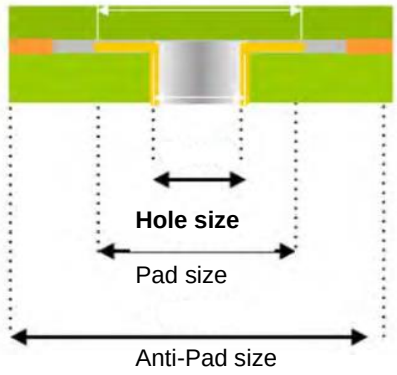

Figure 3-6-1: Dimension of via

3.7 BD71815AGW Breakout Example

For the breakout routing on Layer 1(Top layer) thru 6 (Bottom layer), refer to Figure 3-7-1 thru Figure 3-7-6.

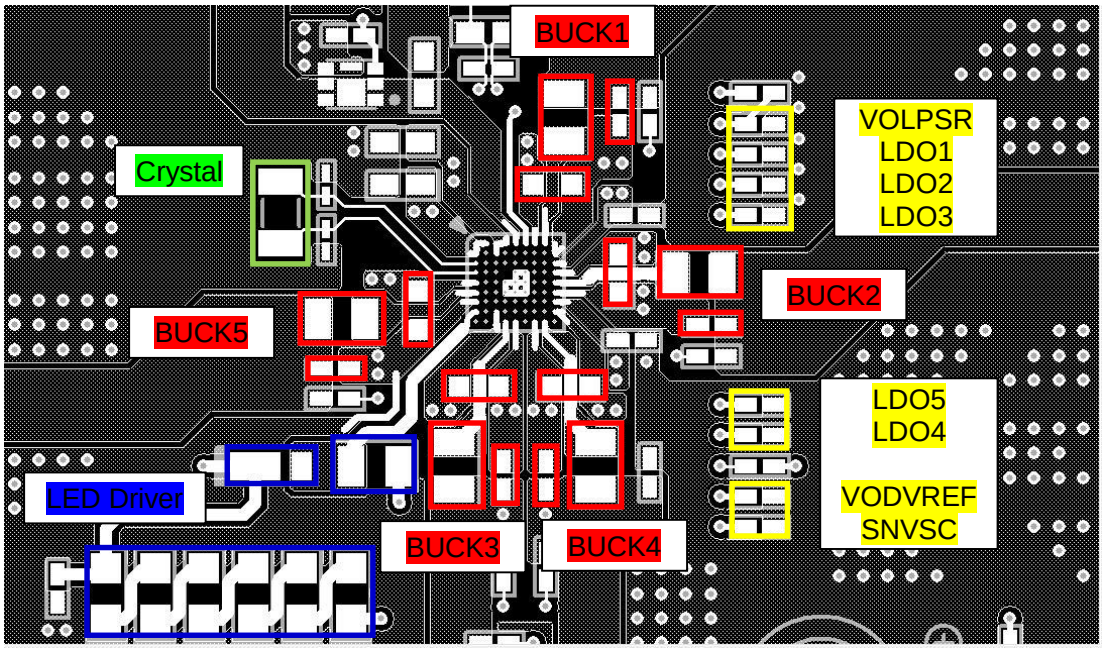

Figure 3-7-1 BD71815AGW Reference Board Breakout and Parts Placement (Top Layer)

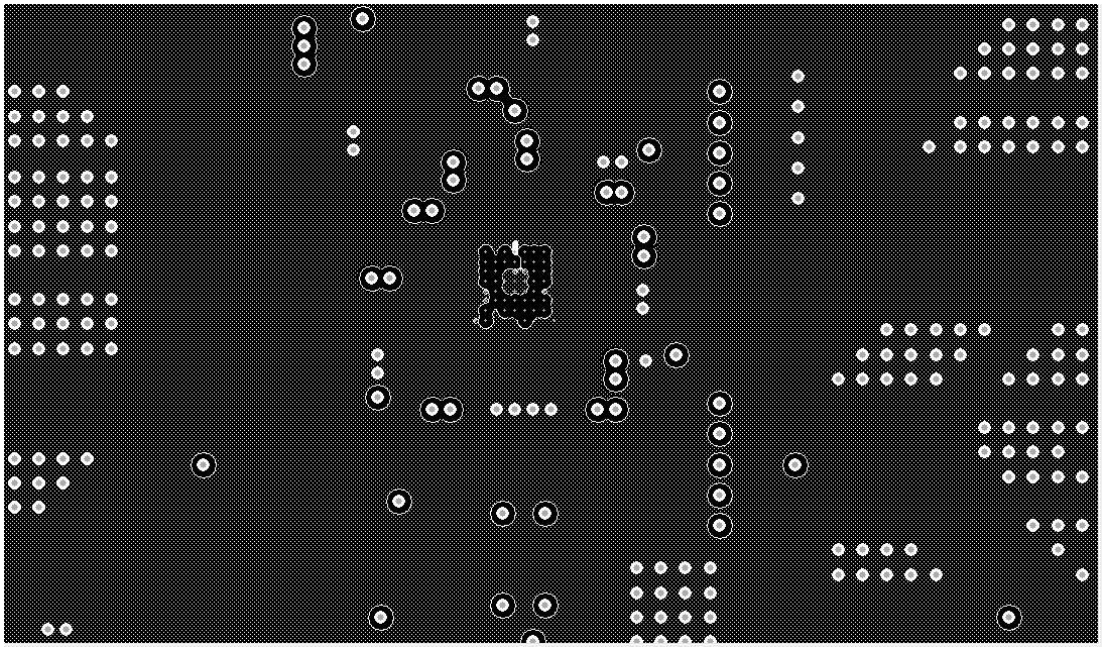

Figure 3-7-2 BD71815AGW Reference Board Breakout (Layer 2)

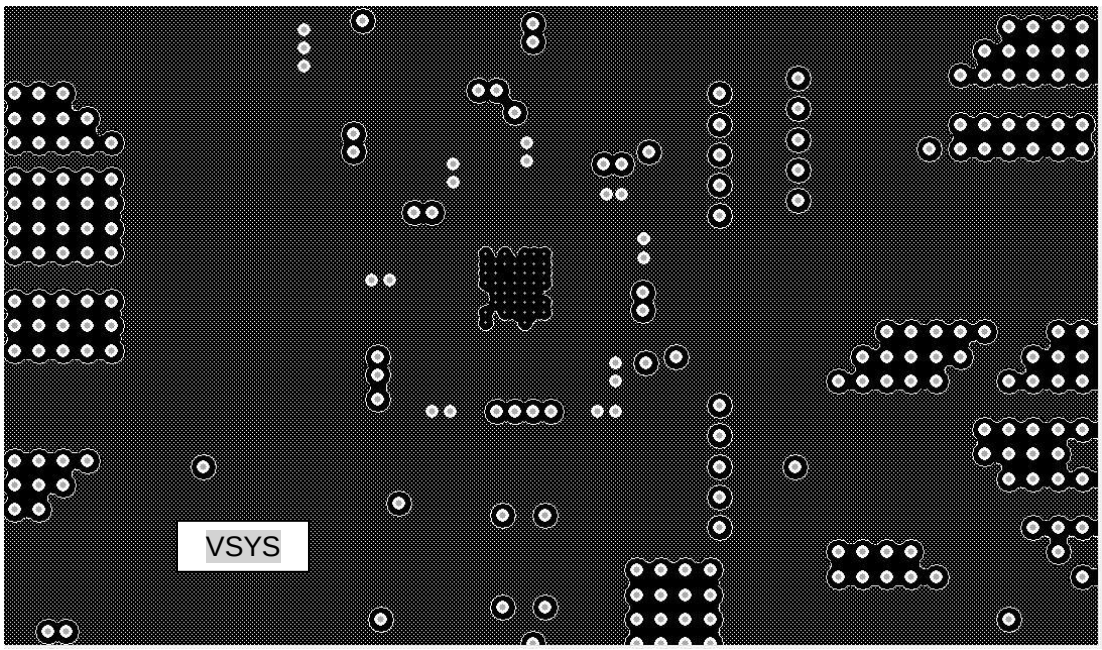

Figure 3-7-3 BD71815AGW Reference Board Breakout (Layer 3)

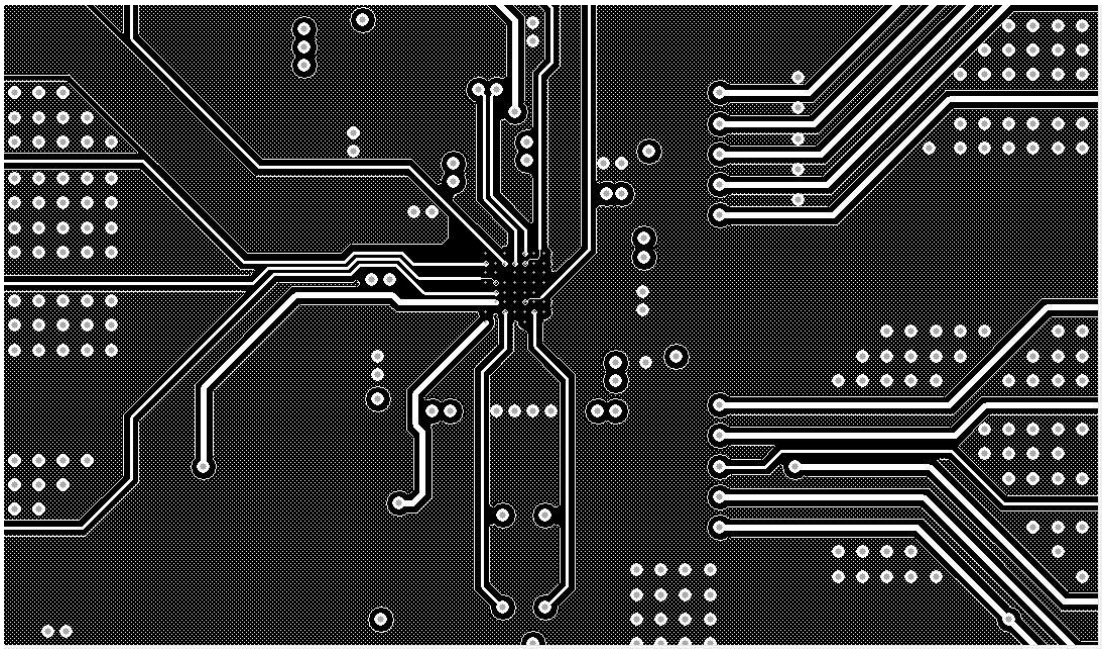

Figure 3-7-4 BD71815AGW Reference Board Breakout (Layer 4)

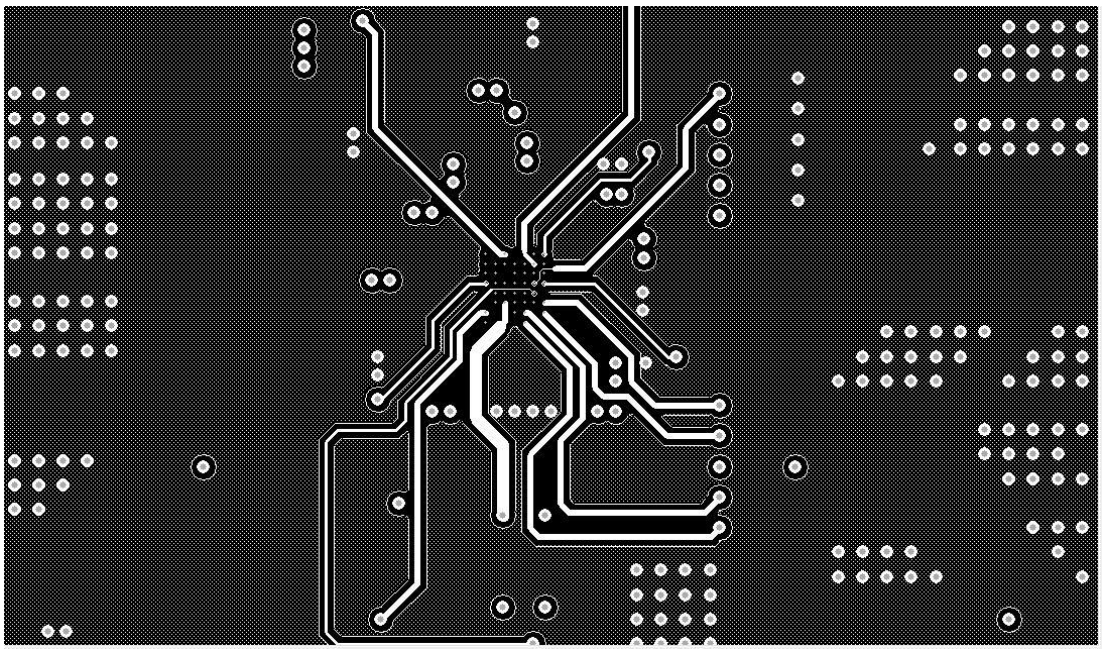

Figure 3-7-5 BD71815AGW Reference Board Breakout (Layer 5)

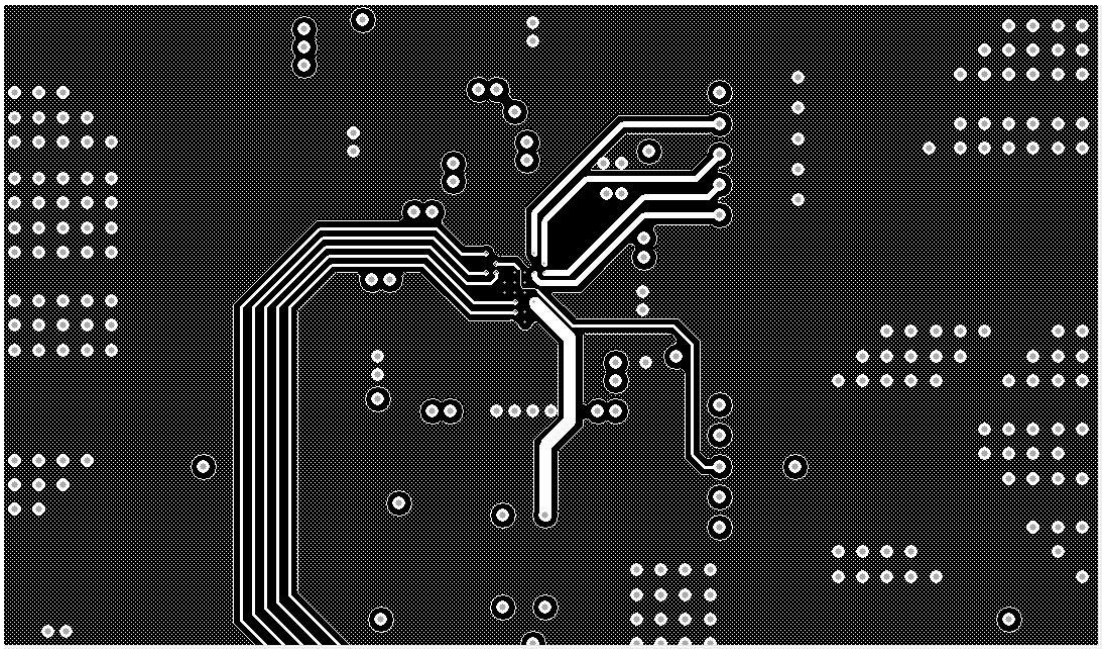

Figure 3-7-6 BD71815AGW Reference Board Breakout (Layer 6)

4 Platform Power Delivery Guidelines

BD71815AGW is a PMIC (Power Management Integrated Circuit) that incorporates single-channel switching regulators (Buck), Linear VRs (LDO), LED Driver, RTC, Single-cell Linear LIB charger and Coulomb counter. It is essential to follow the guidelines for stable power delivery to the SoC and the system.

4.1 Platform Power Delivery

Figure 4-1-1-1 shows the voltages BD71815AGW provides to the SoC and the other devices in the system and Table 4-1-1-1 provides the maximum current guideline for respective voltage rail.

Table 4-1-1-1 DC-to-DC converters and Linear VRs Maximum Design Power

Voltage Rail	Type	Input Voltage	Default Output Voltage [V]	Max Current [mA]
BUCK1	Buck [DVS]	PVIN1	1.100	800
BUCK2	Buck [DVS]	PVIN2	1.000	1000
BUCK3	Buck	PVIN3	1.800	500
BUCK4	Buck	PVIN4	1.200	1000
BUCK5	Buck	PVIN5	3.300	1000
LDO1	LDO	VINL1	3.300	100
LDO2	LDO	VINL1	3.300	100
LDO3	LDO	VINL1	3.300	50
LDO4	LDO	VINL2	3.300	400
LDO5	LDO	VINL2	1.800 / 3.300	250
VODVREF	LDO	VIN	0.5*DVREFIN	10
SNVSC	LDO	VIN	3.000	25
LDOLPSR	LDO	VIN	1.800	100

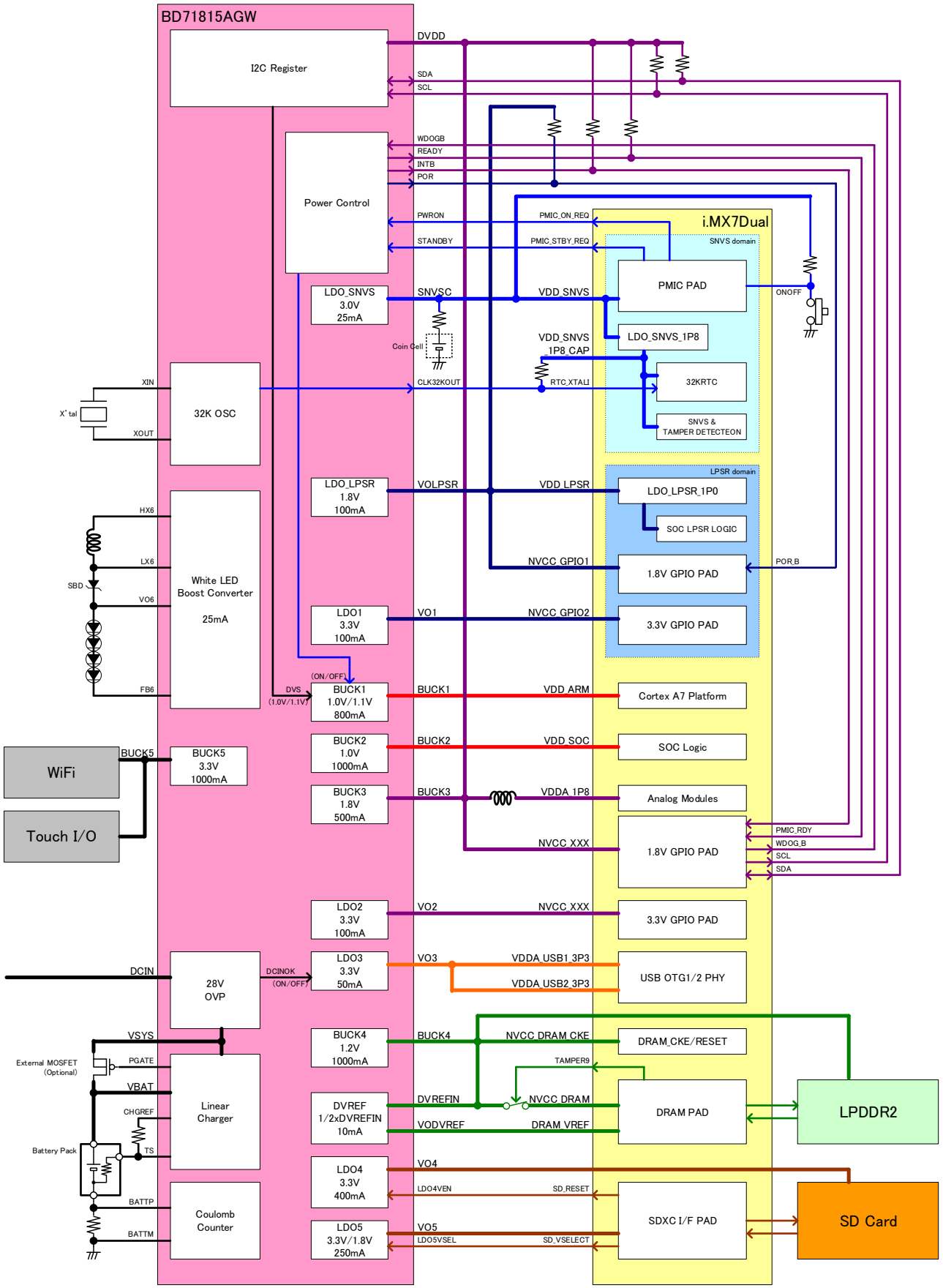

Figure 4-1-1-1: BD71815AGW typical application (E-Book Reader with i.Mx7D)

4.2 General Layout Guideline

This section explains the guideline for Voltage Regulators. High current voltage rails must be carefully laid out to avoid unwanted noise interference from other signals and voltage drop. Especially for switching regulators, abrupt current/ voltage change occurs around the switch-nodes, so please note this in your layout and be sure to follow all the guidelines in this section.

4.2.1 Overall component Placement Example

Figure 4-2-1 shows the overall component-placement example.
The figure shows the components that are needed to put closely to the BD71815AGW. It is strongly recommended that power components are put prior to any other components so that the signals do not interfere with each other.

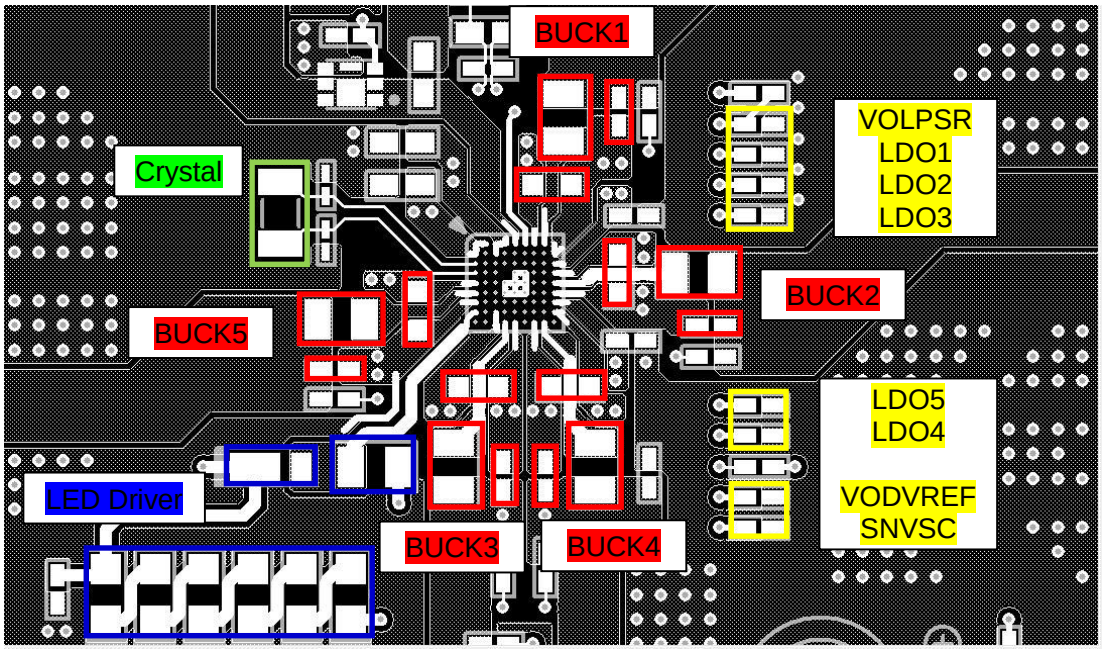

Figure 4-2-1: Overall component placement example

4.2.2 Large Current Loop

There are 2 high pulsing current flowing loops in the buck regulator system.

Loop1:
When Tr2 turns ON, the loop starts from the input capacitor, to VIN terminal, to LX terminal, to L (inductor), to output capacitors, and then returns to the input capacitor through GND.

Loop2:
When Tr1 turns ON, the loop starts from Tr1, to L (inductor), to output capacitors, and then returns to Tr1 through GND.

To reduce the noise and improve the efficiency, please minimize these two loops area. Figure 4-2-2-1 shows the current loops which needs to be designed by taking care of parts placement and the routings.

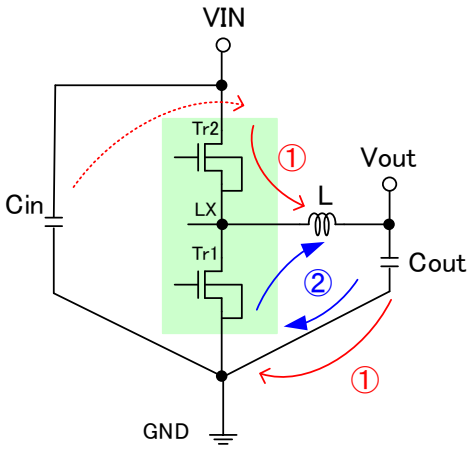

Figure 4-2-2-1: DC-to-DC Converter Large Current Loops

As Figure 4-2-2-2 shows, please route patterns which load heavy current with short and wide traces as much as possible to suppress noise that comes from parasitic inductance on PCB and switching operation, especially for the node's current that changes drastically such as VIN (input voltage) and power ground (GND).

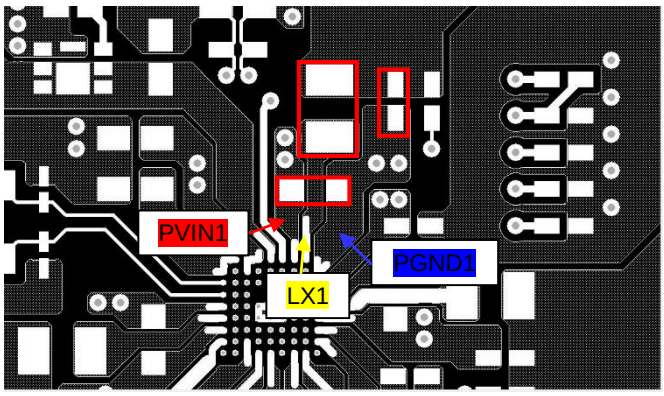

Figure 4-2-2-2: Example of parts placement and routing in the top layer of a buck regulator (BUCK1)

4.2.3 Power GND

Power grounds of DC-to-DC Converters (PGNDx) are noisy ground due to current loops indicated in the previous section. Thus, power grounds should take large area as much as possible to keep impedance low and reduce the swing ground voltage level.

4.2.4 VIN (Power supply for BD71815AGW analog circuit)

VIN should not connect with plane VSYS directly to avoid external noise from PVINx due to common impedance. Also, please place a capacitor near this pin as much as possible to stabilize input power.

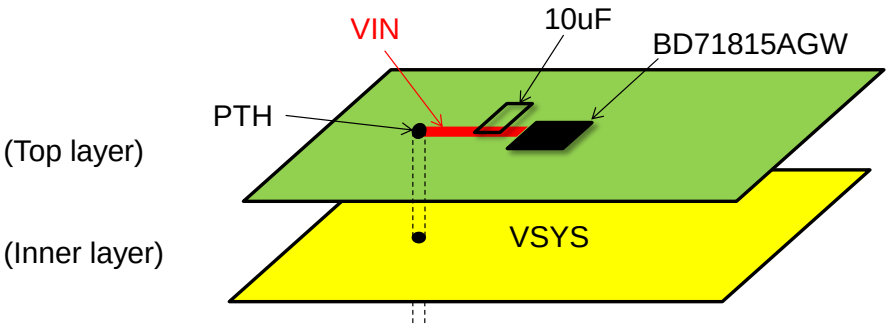

Figure 4-2-4: Layout for VIN

4.2.5 Other Signal Pattern Precautions

Make sure to leave adequate space between noisy lines of voltage rail and serial interface (I2C).

4.2.6 Feedback sense line

Feedback Sense terminals (FBx) are used for voltage rails to send out the accurate voltage. In order for output voltage of each VRs to avoid voltage drop caused by the large current and the parasitic impedance, please make sure that the feedback sense lines are independently routed from the point near output capacitors.

4.3 Switching regulators

4.3.1 BUCK1

BUCK1 is a high-efficiency single buck regulator with integrated FET that converts the VSYS voltage to a regulated voltage. This VR can dynamically change its output voltage setting using the I2C interface. BUCK1 output voltage range is from 0.8V to 2.0V (25mV/ step).

4.3.1.1 Schematic Example

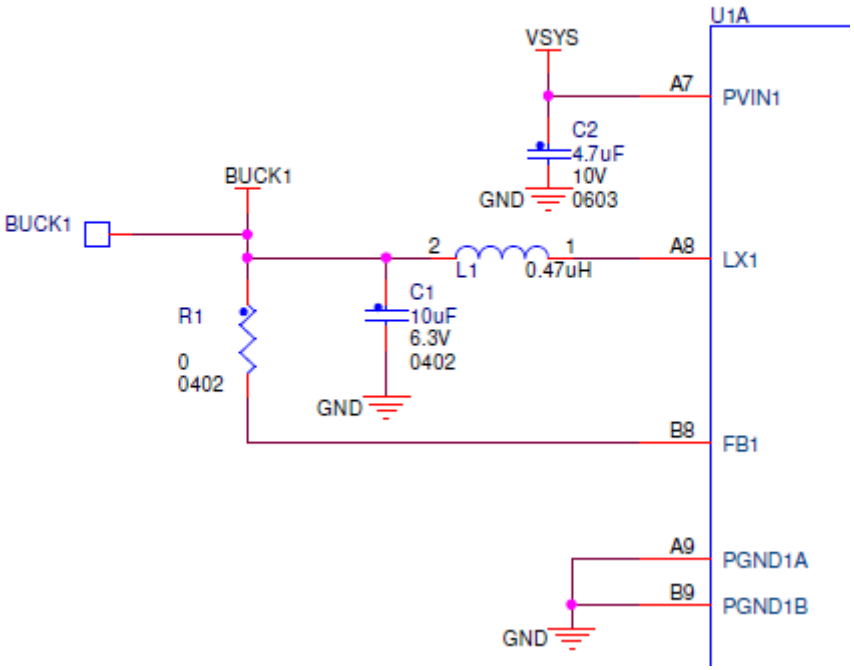

Figure 4-3-1-1 BUCK1 Schematic Example

4.3.1.2 Schematic checklist

Table4-3-1-2 BUCK1 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
BUCK1			
PVIN1	I	Connect to VSYS.	
		As decoupling capacitor, use **one** 4.7µF.	
PGND1[1:0]	I	Connect to Power GND.	
LX1	O	Connect **one** 0.47uH inductor to LX1.	
		As output capacitors, use **one** 10uF capacitors.	
FB1	I	Connect to BUCK1 output voltage which is regulated by the DC/DC converter of BD71815AGW.	

4.3.1.3 Layout Example

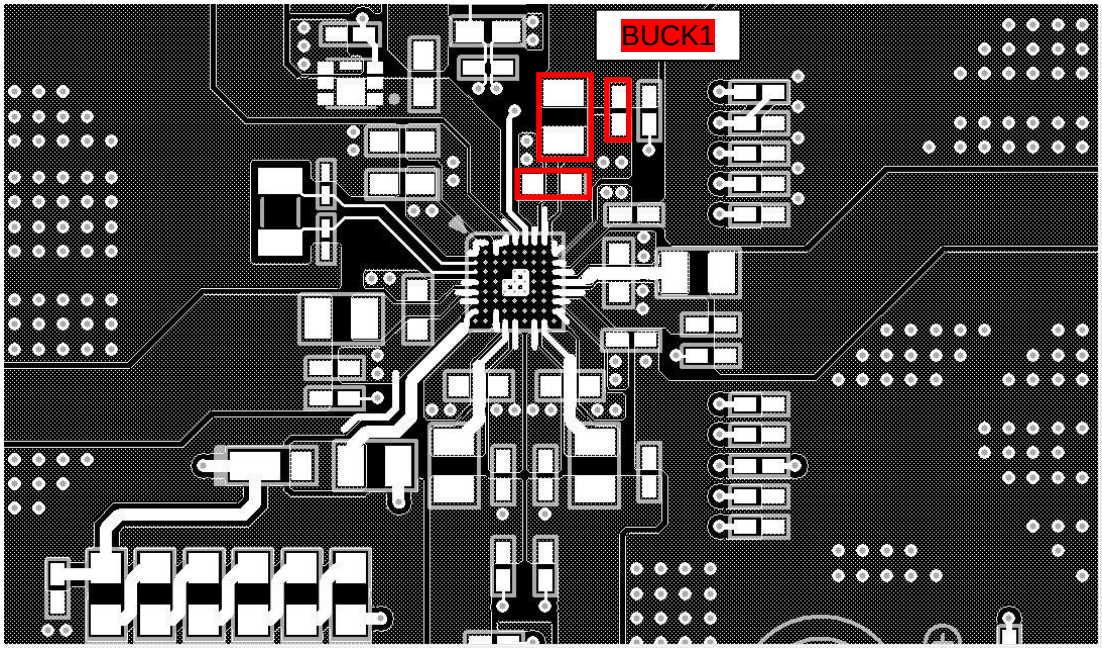

Figure 4-3-1-2 BUCK1 Layout Example (Top Layer)

4.3.2 BUCK2

BUCK2 is a high-efficiency single buck regulator with integrated FET that converts the VSYS voltage to a regulated voltage. This VR can dynamically change its output voltage setting using the I2C interface. BUCK2 output voltage range is from 0.8V to 2.0V (25mV/ step).

4.3.2.1 Schematic Example

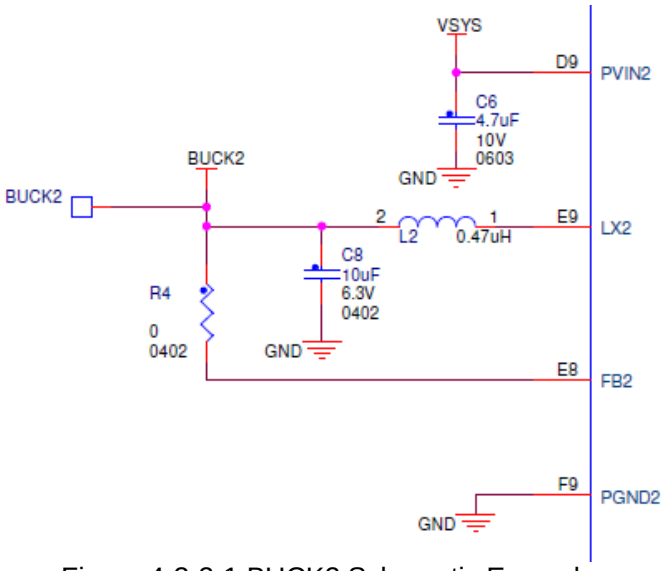

Figure 4-3-2-1 BUCK2 Schematic Example

4.3.2.2 Schematic checklist

Table4-3-2-2 BUCK2 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
BUCK2			
PVIN2	I	Connect to VSYS.	
		As decoupling capacitor, use **one** 4.7µF.	
PGND2	I	Connect to Power GND.	
LX2	O	Connect **one** 0.47uH inductor to LX2.	
		As output capacitors, use **one** 10uF capacitors.	
FB2	I	Connect to BUCK2 output voltage which is regulated by the DC/DC converter of BD71815AGW.	

4.3.2.3 Layout Example

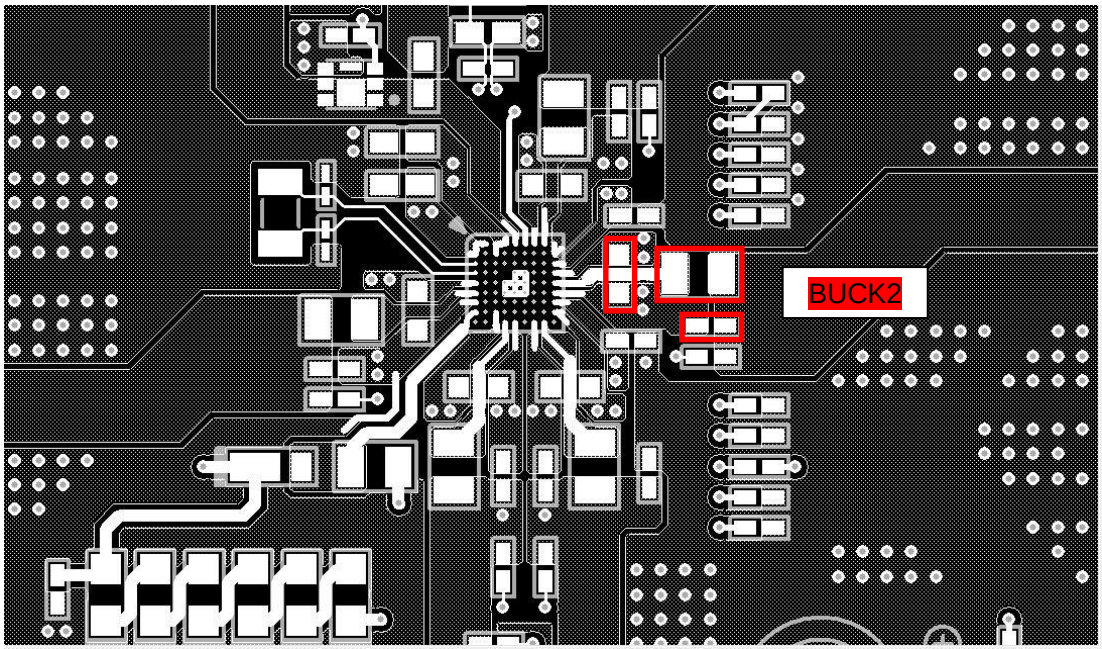

Figure 4-3-2-2 BUCK2 Layout Example (Top Layer)

4.3.3 BUCK3

BUCK3 is a high-efficiency single buck regulator with integrated FET that converts the VSYS voltage to a regulated voltage.

4.3.3.1 Schematic Example

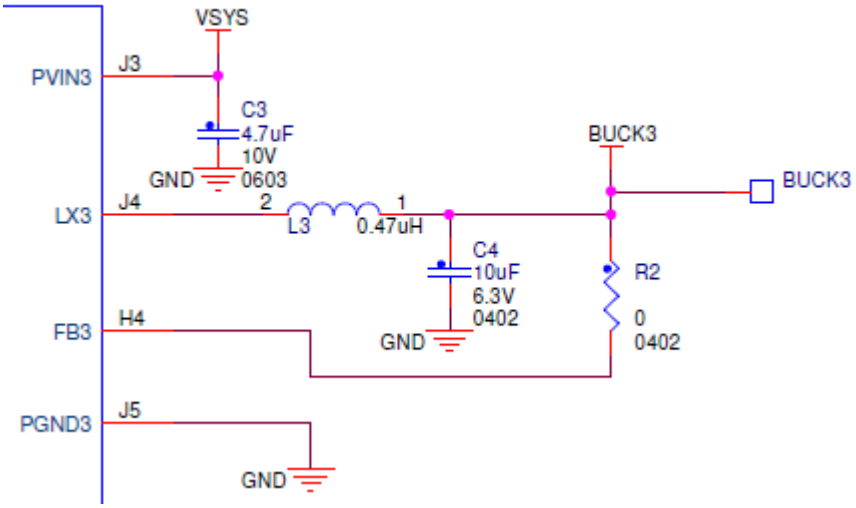

Figure 4-3-3-1 BUCK3 Schematic Example

4.3.3.2 Schematic checklist

Table4-3-3-2 BUCK3 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
BUCK3			
PVIN3	I	Connect to VSYS.	
		As decoupling capacitor, use **one** 4.7µF.	
PGND3	I	Connect to Power GND.	
LX3	O	Connect **one** 0.47uH inductor to LX3.	
		As output capacitors, use **one** 10uF capacitors.	
FB3	I	Connect to BUCK3 output voltage which is regulated by the DC/DC converter of BD71815AGW.	

4.3.3.3 Layout Example

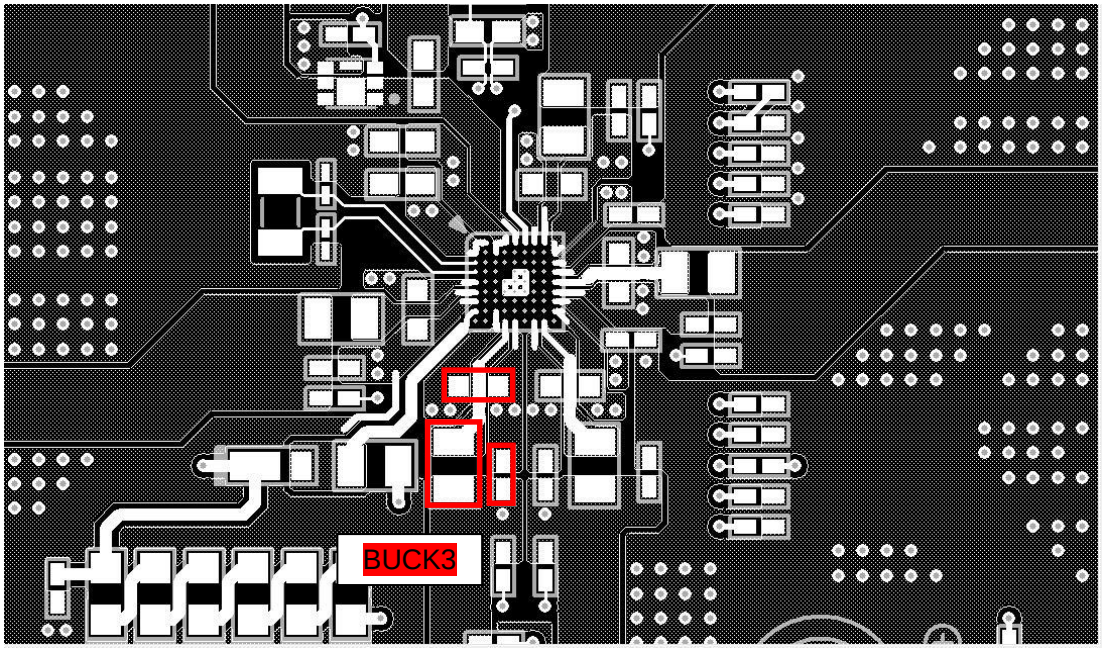

Figure 4-3-3-2 BUCK3 Layout Example (Top Layer)

4.3.4 BUCK4

BUCK4 is a high-efficiency single buck regulator with integrated FET that converts the VSYS voltage to a regulated voltage.

4.3.4.1 Schematic Example

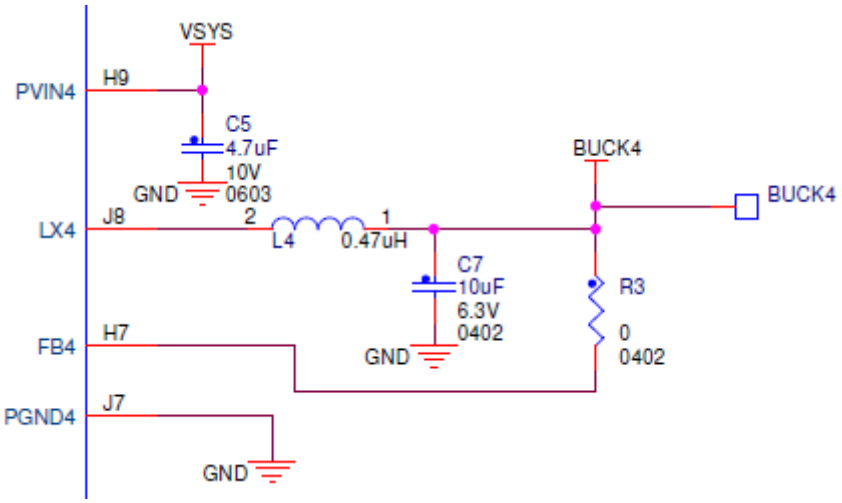

Figure 4-3-4-1 BUCK4 Schematic Example

4.3.4.2 Schematic checklist

Table4-3-4-2 BUCK4 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
BUCK4			
PVIN4	I	Connect to VSYS.	
		As decoupling capacitor, use **one** 4.7µF.	
PGND4	I	Connect to Power GND.	
LX4	O	Connect **one** 0.47uH inductor to LX4.	
		As output capacitors, use **one** 10uF capacitors.	
FB4	I	Connect to BUCK4 output voltage which is regulated by the DC/DC converter of BD71815AGW.	

4.3.4.3 Layout Example

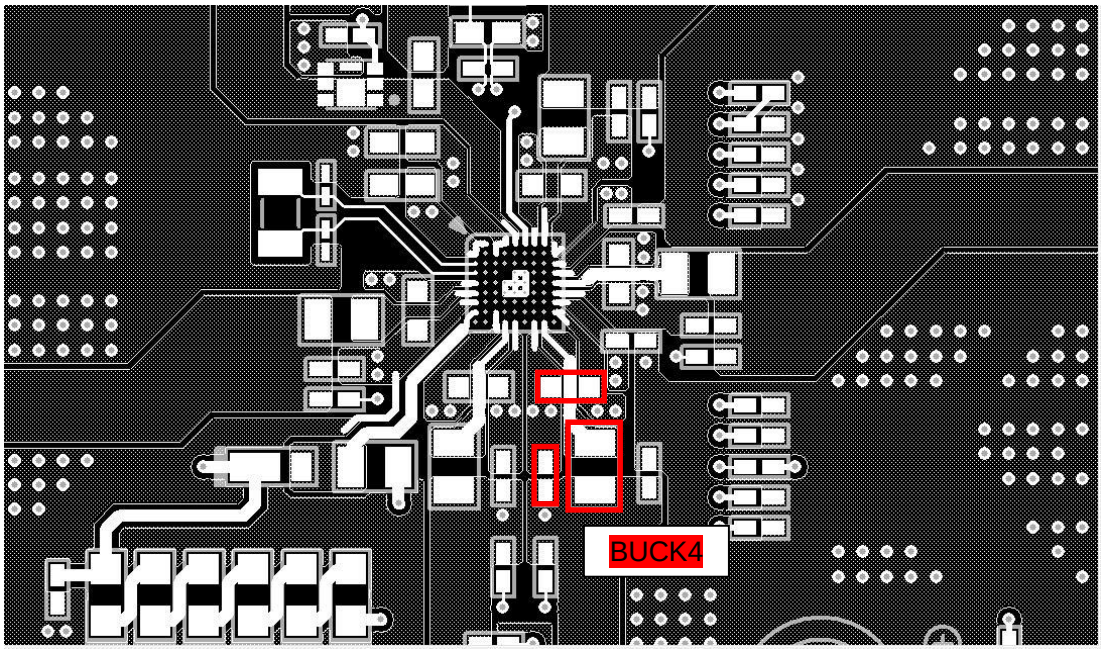

Figure 4-3-4-2 BUCK4 Layout Example (Top Layer)

4.3.5 BUCK5

BUCK5 is a high-efficiency single buck regulator with integrated FET that converts the VSYS voltage to a regulated voltage.

4.3.5.1 Schematic Example

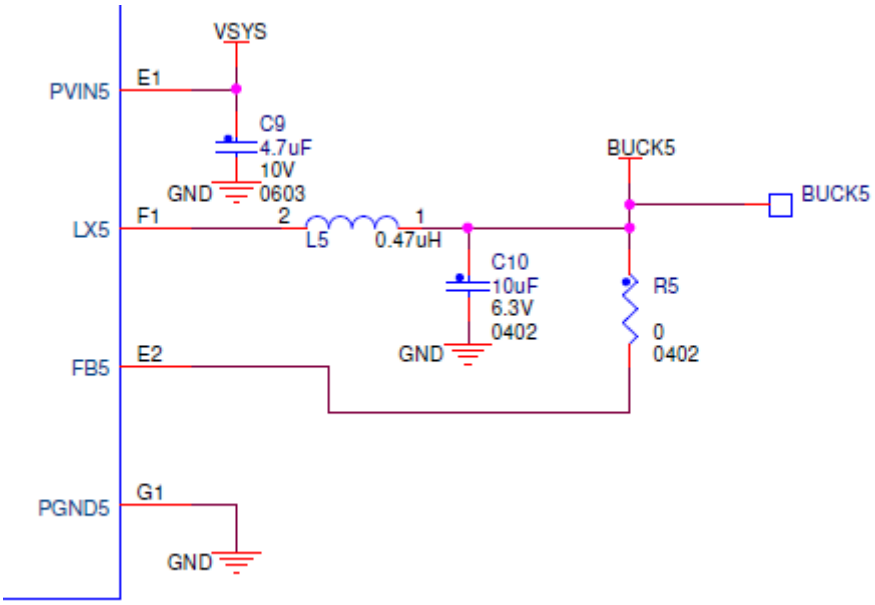

Figure 4-3-5-1 BUCK5 Schematic Example

4.3.5.2 Schematic checklist

Table4-3-5-2 BUCK5 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
BUCK5			
PVIN5	I	Connect to VSYS.	
		As decoupling capacitor, use **one** 4.7µF.	
PGND5	I	Connect to Power GND.	
LX5	O	Connect **one** 0.47uH inductor to LX5.	
		As output capacitors, use **one** 10uF capacitors.	
FB5	I	Connect to BUCK5 output voltage which is regulated by the DC/DC converter of BD71815AGW.	

4.3.4.3 Layout Example

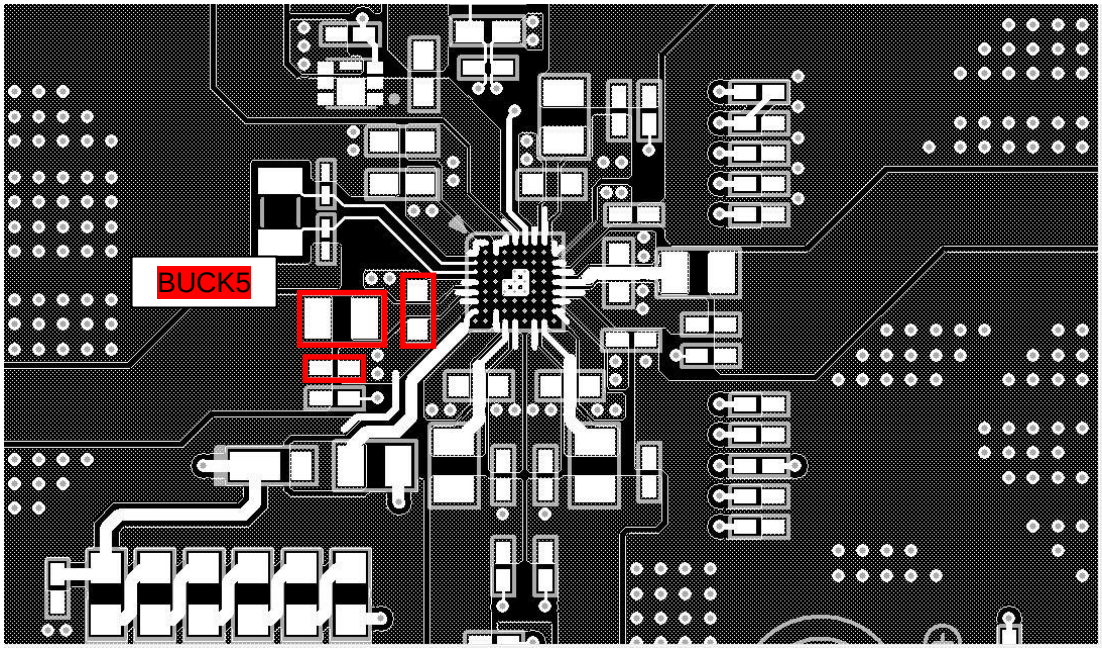

Figure 4-3-5-2 BUCK5 Layout Example (Top Layer)

4.3.6 LED Driver

4.3.6.1 Schematic Example

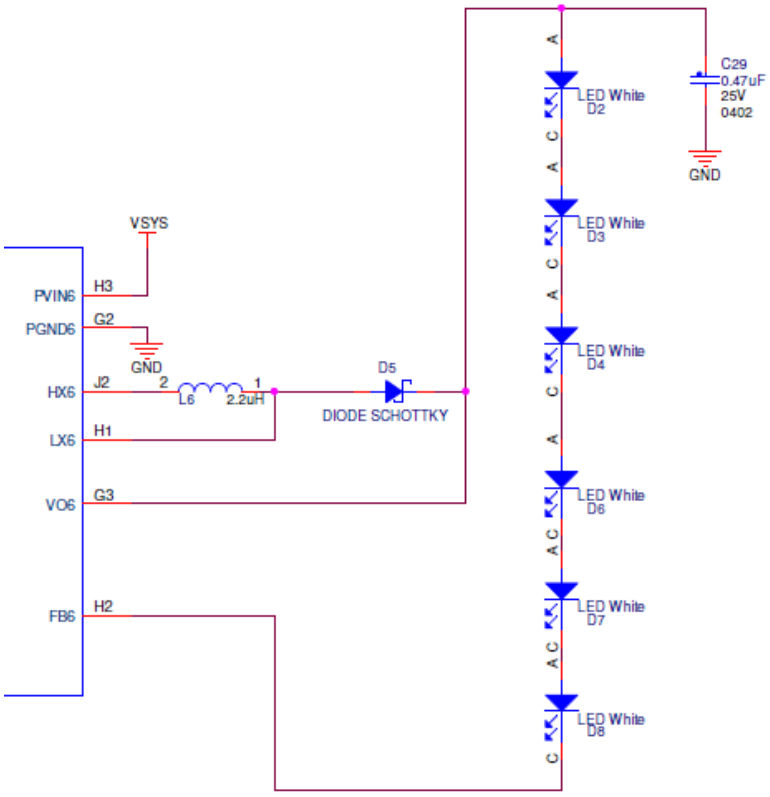

Figure 4-3-6-1 LED Driver Schematic Example

4.3.6.2 Schematic checklist

Table4-3-6-2 LED Driver schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
LED Driver			
PVIN6	I	Connect to VSYS.	
PGND6	I	Connect to Power GND.	
HX6 / LX6	O	Connect **One** 2.2uH inductor to HX6 / LX6.	
		Connect Shottky Diode between LX6 and VO6. **<Recommended Part>** RB550VA-30TR (ROHM)	
VO6	O	Connect LEDs between VO6 and FB6 up to a maximum of 6pcs.	
FB6	I		

4.3.6.2 Layout

An input capacitor dedicated to PVIN6 is not needed if the trace of PVIN6 is merged with the one of PVIN3 since PVIN6 can share the input capacitor of PVIN3.

4.4 Linear VR

4.4.1 LDO1-5 / VODVREF / SNVSC

4.4.1.1 Schematic Examples

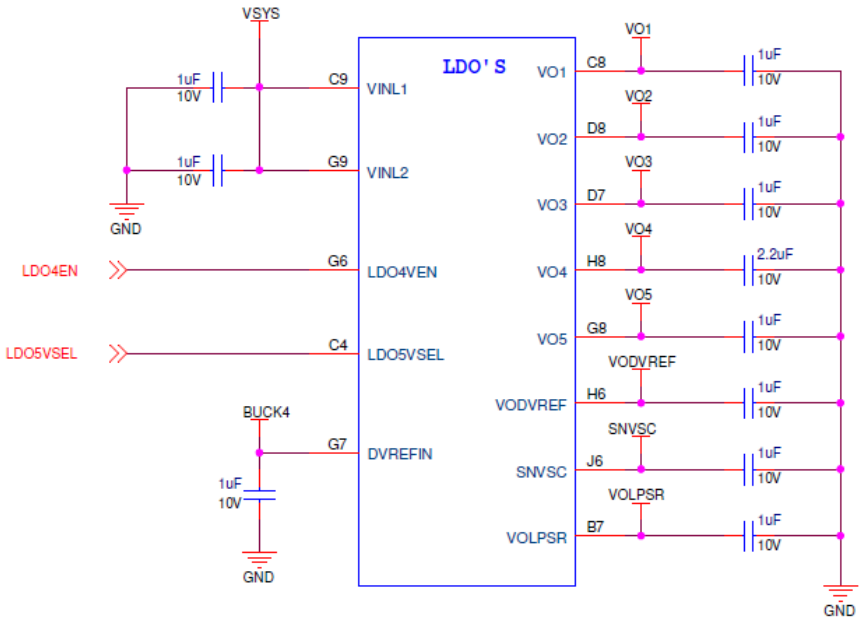

Figure 4-4-1 LDO1-3 Schematic Example

4.4.1.2 Schematic checklist

Table4-4-1 LDO1-3 schematic checklist

Pin Names	Dir.	Notes (Unit of parts size : inch)	Check
LDO1-3 (Linear VR)			
VINL1	I	Connect to VSYS.	
		As decoupling capacitors, use **one** 1.0μF.	
VO1	O	As output capacitors, use **one** 1.0uF capacitor.	
VO2	O	As output capacitors, use **one** 1.0uF capacitor.	
VO3	O	As output capacitors, use **one** 1.0uF capacitor.	
LDO for SD Card (Linear VR)			
VINL2	I	Connect to VSYS.	
		As decoupling capacitors, use **one** 1.0μF.	
VO4	O	As output capacitors, use **one** 2.2uF capacitor.	
VO5	O	As output capacitors, use **one** 1.0uF capacitor.	
LDO for DDR Reference Voltage (Linear VR)			
DVREFIN	I	Connect to BUCK4	
		As decoupling capacitors, use **one** 1.0μF.	
VODVREF	O	As output capacitors, use **one** 1.0uF capacitor.	
LDO for Secure Non-Volatile Storage (Linear VR)			
SNVSC	O	As output capacitors, use **one** 1.0uF capacitor.	
		Connect a Coin cell backup battery via current limit resistor.	
LDO for Low-Power State Retention (Linear VR)			
VOLPSR	O	As output capacitors, use one 1.0uF capacitor.	

4.5 Interfaces

4.5.1 I2C

Table4-5-1 Schematic checklist of I2C

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
I2C						
DVDD	I			-	Connect to BUCK3 (1.8V) or LDO2 (3.3V) depending on system requirement	
SCL	I	DVDD	2.2K Ohm pull-up to DVDD	-	Connect to SOC	
SDA	I/O	DVDD	2.2K Ohm pull-up to DVDD	-	Connect to SOC	

4.5.2 GPO

Table4-5-2 Schematic checklist of GPO

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
GPO						
GPO1	O	SNVSC	Needed for open drain mode (default)	NC		

4.5.3 Charger, Coulomb counter, OVP

Table4-5-3 Schematic checklist of Charger, Coulomb counter, OVP

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
Charger, Coulomb counter, OVP						
DCIN[2:0]	I			-	As a decoupling capacitor, use one 1.0μF.	
VSYS[1:0]	O			-	As an output capacitor, use one 10μF.	
VBAT	I/O			-	As an output capacitor, use one 10μF.	
PGATE	O			-	Connect to gate of Pch MOSFET between VSYS and VBAT. 0.1uF cap is requested to insert between PGATE and the source of Pch MOSFET. **<Recommended Part>** RF4C050AP (ROHM)	
CHGLED	O			NC	Connect to LED via current limit resistor	
CHGGND	I			GND	Connect to Power GND.	
CHGREF	O			NC	Connect to a thermistor via 10kΩ resistor	
TS	I		5.1K Ohm pull-up to CHGREF (NTC=10K Ohm)	NC	Connect to Battery Thermistor	
BATTP	I			GND	Connect to a current sense resistor (10mΩ) individually for accurate sensing. 0.1uF cap is requested to insert between BATTP and BATTM.	
BATTM	I			GND	Connect to a current sense resistor (10mΩ) individually for accurate sensing. 0.1uF cap is requested to insert between BATTP and BATTM.	

Note;
An input capacitor dedicated to VIN is not needed if the trace of VIN is merged with the one of VSYS since VIN can share the output capacitor of VSYS.

4.5.3.1 Schematic Example

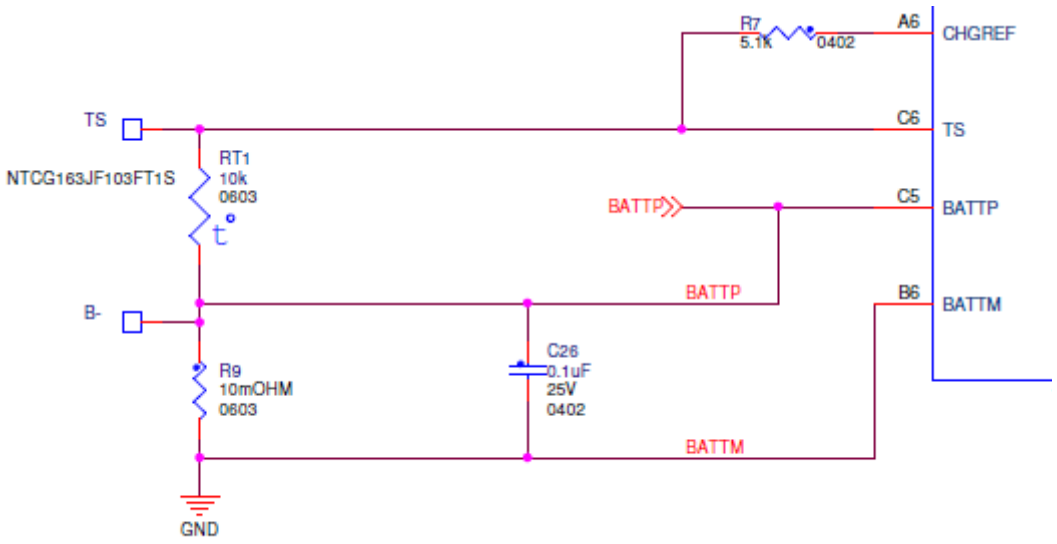

Figure 4-5-3-1 Charger Layout Example (Top Layer and 4th layer)

4.5.3.2 Layout Example

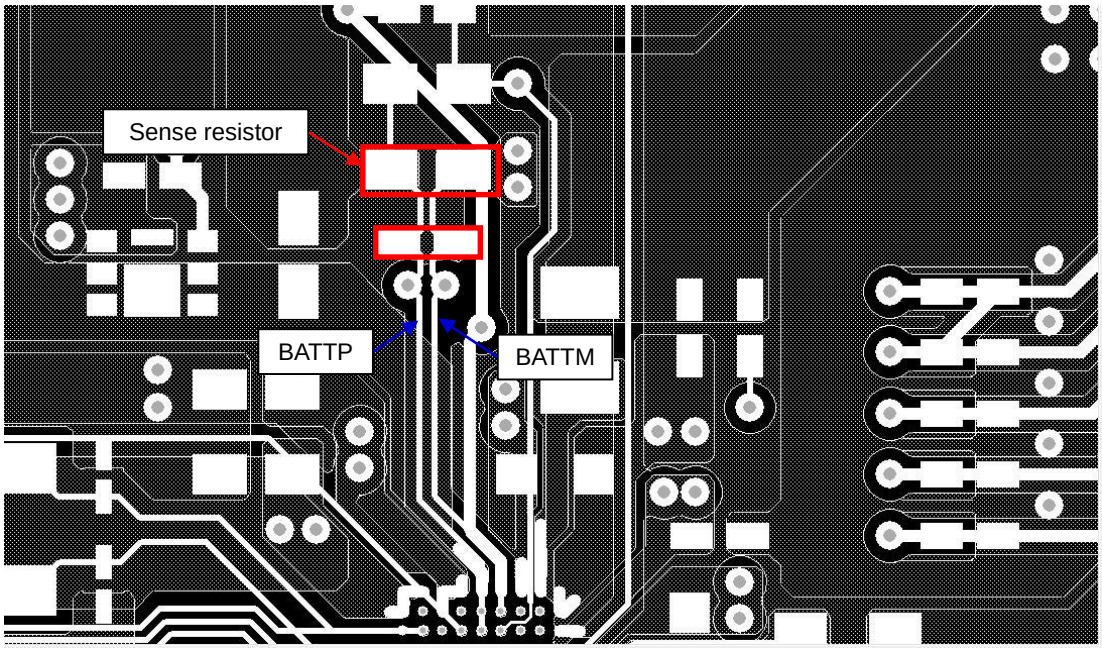

Figure 4-5-3-2 Charger Layout Example (Top Layer and 4th layer)

Note;
Routings of BATTP and BATTM between PMIC and the sense resistor has to be independent for accurate sensing. To avoid any influence of common impedance of soldering, connecting BATTP and BATTM to inside pads of the sense resistor is recommended.

4.5.4 RTC

Table4-5-4 Schematic checklist of RTC

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
RTC						
XIN	I			-	Connect to a crystal oscillator	
					[SEIKO EPSON: FC-135 is chosen for a crystal oscillator] As input capacitor, use **one** 22pF. **[Other crystal oscillator is chosen]** Please set the input capacitor value on enough matching validation.	
XOUT	O			-	Connect to a crystal oscillator	
					[SEIKO EPSON: FC-135 is chosen for a crystal oscillator] As output capacitor, use **one** 22pF. **[Other crystal oscillator is chosen]** Please set the output capacitor value on enough matching validation.	
CLK32KOUT	O		Needed for open drain mode (default)	NC		

4.5.5 System Control signals

Table4-5-5 Schematic checklist of System Control signals

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
System Control - Reset, Power, and Control Signals						
RESETINB	I		Internal 10K Ohm pull-up to SNVSC	NC		
PWRON	I		Internal 1.5M Ohm pull-down	-	Connect to SoC	
STANDBY	I			-	Connect to SoC	
LDO4EN	I			-	Connect to SoC	
LDO5SEL	I			-	Connect to SoC	
INTB	O		Needed pull-up resistor to DVDD	-	Connect to SoC	
POR	O		Needed pull-up resistor to DVDD	-	Connect to SoC	
WDOGB	I		Needed pull-up resistor to DVDD	-	Connect to SoC	
READY	O		Needed pull-up resistor to DVDD	-	Connect to SoC	

4.5.6 MISC

Table4-5-6 Schematic checklist of MISC

Pin Names	Dir.	Signal Voltage Level	System Pull-up/Pull-down (RTT)	Termination if it is not used	Notes	Check
MISC						
GND[11:0]	I	GND		-	Connect to GND plane	