

**PI6CB18801**

**Very Low Power 8-Output PCIe Clock Buffer With On-chip Termination**

**Features**

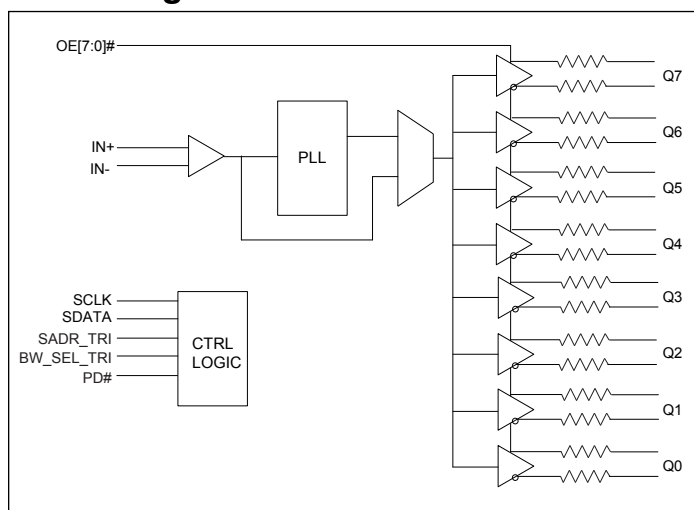
- 1.8V supply voltage
- HCSL input: 100MHz, also support 50MHz or 125MHz via SMBus
- 8 differential low power HCSL outputs with on-chip termination
- Individual output enable
- Programmable Slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Strapping pins or SMBus for configuration;
- 3.3V tolerant SMBus interface support
- Very low jitter outputs
  - Differential cycle-to-cycle jitter <50ps
  - Differential output-to-output skew <50ps
  - PCIe Gen1/Gen2/Gen3/Gen4 compliant
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/contact-us) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green): 48-lead 6x6mm TQFN

**Description**

The PI6CB18801 is an 8-output very low power PCIe Gen1/Gen2/Gen3/Gen4 clock buffer. It takes an reference input to fanout eight 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 32 external resistors and make layout easier. Individual OE pin for each output provides easier power management.

It uses Diodes proprietary PLL design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4 requirements. Other than PCIe 100MHz support, this device also support Ethernet application with 50MHz or 125MHz via SMBus. It provides various options such as different slew rate and amplitude through strapping pins or SMBUS so that users can configure the device easily to get the optimized performance for their individual boards.

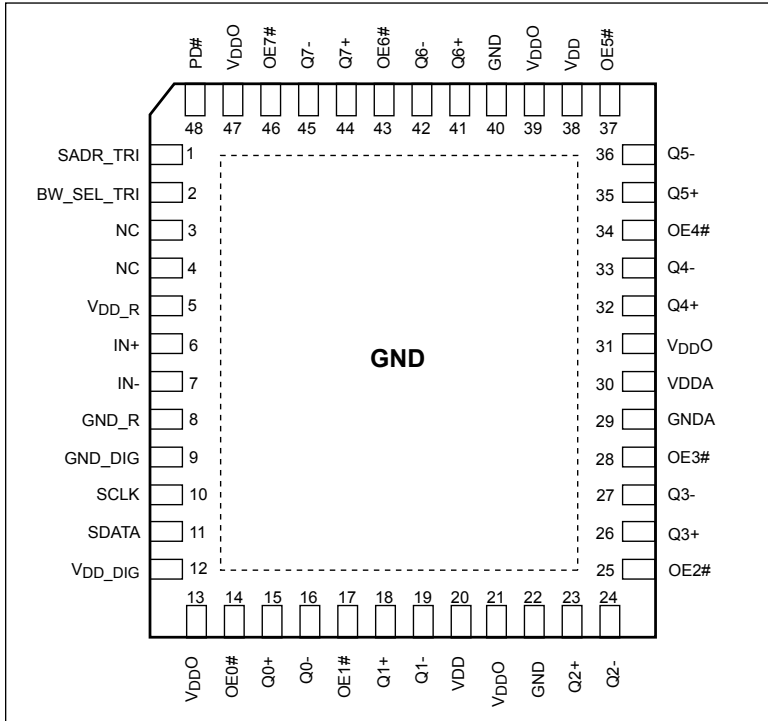
**Block Diagram**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Description

Pin Number	Pin Name	Type		Description
1	SADR_TRI	Input	Tri-level	Latch to select SMBus Address. This pin has an internal pull-down
2	BW_SEL_TRI	Input	Tri-level	Latch to select low loop bandwidth, bypass PLL, and high loop bandwidth. This pin has both internal pull-up and pull-down
3	NC			Internal connected for feedback loop. Do not connect this pin
4	NC			Internal connected for feedback loop. Do not connect this pin
5	VDD_R	Power		Power supply for input differential buffers
6	IN+	Input		Differential true clock input
7	IN-	Input		Differential complementary clock input
8	GND_R	Power		Ground for input differential buffers
9	GND_DIG	Power		Ground for digital circuitry
10	SCLK	Input	CMOS	SMBUS clock input, 3.3V tolerant
11	SDATA	Input/ Output	CMOS	SMBUS Data line, 3.3V tolerant
12	VDD_DIG	Power		Power supply for digital circuitry, nominal 1.8V
13, 21, 31, 39, 47	VDDO	Power		Power supply for differential outputs
14	OE0#	Input	CMOS	Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
15	Q0+	Output	HCSL	Differential true clock output

### Pin Description Cont.

Pin Number	Pin Name	Type		Description
16	Q0-	Output	HCSL	Differential complementary clock output
17	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	Q1+	Output	HCSL	Differential true clock output
19	Q1-	Output	HCSL	Differential complementary clock output
20, 38	V <sub>DD</sub>	Power		Power supply, nominal 1.8V
22, 40	GND	Power		Ground
23	Q2+	Output	HCSL	Differential true clock output
24	Q2-	Output	HCSL	Differential complementary clock output
25	OE2#	Input	CMOS	Active low input for enabling Q2 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
26	Q3+	Output	HCSL	Differential true clock output
27	Q3-	Output	HCSL	Differential complementary clock output
28	OE3#	Input	CMOS	Active low input for enabling Q3 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
29	GNDA	Power		Ground for analog circuitry
30	V <sub>DDA</sub>	Power		Power supply for analog circuitry
32	Q4+	Output	HCSL	Differential true clock output
33	Q4-	Output	HCSL	Differential complementary clock output
34	OE4#	Input	CMOS	Active low input for enabling Q4 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
35	Q5+	Output	HCSL	Differential true clock output
36	Q5-	Output	HCSL	Differential complementary clock output
37	OE5#	Input	CMOS	Active low input for enabling Q5 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
41	Q6+	Output	HCSL	Differential true clock output
42	Q6-	Output	HCSL	Differential complementary clock output
43	OE6#	Input	CMOS	Active low input for enabling Q6 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
44	Q7+	Output	HCSL	Differential true clock output
45	Q7-	Output	HCSL	Differential complementary clock output
46	OE7#	Input	CMOS	Active low input for enabling Q7 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
48	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
49	EPAD	Power		Connect to Ground

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### SMBus Address Selection Table

	SADR	Address	+Read/Write Bit
State of SADR on first application of PD#	0	1101011	X
	M	1101100	X
	1	1101101	X

### Power Management Table

PD#	IN	SMBus OE bit	OEn#	Qn+	Qn-	PLL Status
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On <sup>(1)</sup>
1	Running	1	0	Running	Running	On <sup>(1)</sup>
1	Running	1	1	Low	Low	On <sup>(1)</sup>

Note:

1. If PLL Bypass mode is selected, the PLL will be off and outputs will be running.

### PLL Operating Mode Select Table

BW_SEL_TRI	Operating Mode	Byte1 [7:6] Readback	Byte1 [4:3] Readback
0	PLL with low Bandwidth	00	00
M	PLL Bypass	01	01
1	PLL with high Bandwidth	11	11

### Frequency Select table

Freq. Select Byte 3 [4:3]	IN (MHz)	Qn (MHz)
00 (default)	100	100
01	50	50
10	125	125
11	Reserved	Reserved

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential, $V_{DDxx}$ .....	-0.5V to +2.5V
Input Voltage .....	-0.5V to $V_{DD}+0.5V$ , not exceed 2.5V
SMBus, Input High Voltage .....	3.6V
ESD Protection (HBM) .....	2000 V
Junction Temperature .....	125 °C max

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Operating Conditions

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$V_{DD}, V_{DDA}, V_{DD\_R}, V_{DD\_DIG}$	Power Supply Voltage		1.7	1.8	1.9	V
$V_{DDO}$	Output Power Supply Voltage		0.9975	1.05-1.8	1.9	V
$I_{DDA}$	Analog Power Supply Current	$V_{DDA} + V_{DD\_R}$ , PLL mode, All outputs active @100MHz		11	15	mA
$I_{DD}$	Power Supply Current	$V_{DD} + V_{DD\_DIG}$ , All outputs active @100MHz		8	10	mA
$I_{DDO}$	Power Supply Current for Outputs	All outputs active @100MHz		28	35	mA
$I_{DDA\_PD}$	Analog Power Supply Power Down <sup>(1)</sup> Current	$V_{DDA} + V_{DD\_R}$ , PLL mode, All outputs active @100MHz		0.7	1	mA
$I_{DD\_PD}$	Power Supply Power Down <sup>(1)</sup> Current	$V_{DD} + V_{DD\_DIG}$ , All outputs LOW/LOW		1.2	2	mA
$I_{DDO\_PD}$	Power Supply Current Power Down <sup>(1)</sup> for Outputs	$V_{DDO}$ , All outputs LOW/LOW		0	0.01	mA
$T_A$	Ambient Temperature	Industrial grade	-40		85	°C

**Note:**

1. Input clock is not running.

## Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$R_{pu}$	Internal pull up resistance			120		K $\Omega$
$R_{dn}$	Internal pull down resistance			120		K $\Omega$
$L_{PIN}$	Pin inductance				7	nH

### SMBus Electrical Characteristics

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$V_{DDSMB}$	Nominal bus voltage		1.7		3.6	V
$V_{IHSMB}$	SMBus Input High Voltage	SMBus, $V_{DDSMB} = 3.3V$	2.1		3.6	V
		SMBus, $V_{DDSMB} < 3.3V$	0.65 $V_{DDSMB}$			
$V_{ILSMB}$	SMBus Input Low Voltage	SMBus, $V_{DDSMB} = 3.3V$			0.6	V
		SMBus, $V_{DDSMB} < 3.3V$			0.6	
$I_{SMBSINK}$	SMBus sink current	SMBus, at $V_{OLSMB}$	4			mA
$V_{OLSMB}$	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
$f_{MAXSMB}$	SMBus operating frequency	Maximum frequency			400	kHz
$t_{RMSB}$	SMBus rise time	(Max $V_{IL} - 0.15$ ) to (Min $V_{IH} + 0.15$ )			1000	ns
$t_{FMSB}$	SMBus fall time	(Min $V_{IH} + 0.15$ ) to (Max $V_{IL} - 0.15$ )			300	ns

### LVC MOS DC Electrical Characteristics

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage	Single-ended inputs, except SMBus	0.75 $V_{DD}$		$V_{DD}$ +0.3	V
$V_{IM}$	Input Mid Voltage	SADR_TRI, BW_SEL_TRI	0.4 $V_{DD}$	0.5 $V_{DD}$	0.6 $V_{DD}$	V
$V_{IL}$	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25 $V_{DD}$	V
$I_{IH}$	Input High Current	Single-ended inputs, $V_{IN} = V_{DD}$			20	$\mu A$
$I_{IL}$	Input Low Current	Single-ended inputs, $V_{IN} = 0V$	-20			$\mu A$
$I_{IH}$	Input High Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = V_{DD}$			220	$\mu A$
$I_{IL}$	Input Low Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = 0V$	-220			$\mu A$
$C_{IN}$	Input Capacitance		1.5		5	pF

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## LVCMOS AC Electrical Characteristics

 Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$t_{OELAT}$	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion	1		3	clocks
$t_{PDLAT}$	PD# de-assertion	Differential outputs enable after PD# de-assertion		20	300	us

## HCSL Input Characteristics<sup>(1)</sup>

 Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$V_{IHDIF}$	Diff. Input High Voltage <sup>(3)</sup>	IN+, IN-, single-end measurement	600	800	1150	mV
$V_{ILDIF}$	Diff. Input Low Voltage <sup>(3)</sup>	IN+, IN-, single-end measurement	-300	0	300	mV
$V_{COM}$	Diff. Input Common Mode Voltage		150		1000	mV
$V_{SWING}$	Diff. Input Swing Voltage	Peak to peak value ( $V_{IHDIF} - V_{ILDIF}$ )	300		1450	mV
$f_{INBP}$	Input Frequency	PLL Bypass mode	1		200	MHz
$f_{IN100}$	Input Frequency	100MHz PLL	60	100	110	MHz
$f_{IN125}$	Input Frequency	125MHz PLL	75	125	137.5	MHz
$f_{IN156}$	Input Frequency	50MHz PLL	30	50	65	MHz
$t_{STAB}$	Clock stabilization	From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1.0	ms
$t_{RF}$	Diff. Input Slew Rate <sup>(2)</sup>	Measured differentially	0.4			V/ns
$I_{IN}$	Diff. Input Leakage Current	$V_{IN} = V_{DD}, V_{IN} = GND$	-5	0.01	5	uA
$t_{DC}$	Diff. Input Duty Cycle	Measured differentially	45		55	%
$t_{j-c-c}$	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

### Note:

- Guaranteed by design and characterization, not 100% tested in production
- Slew rate measured through +/-75mV window centered around differential zero
- The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the  $V_{bias}$ , where  $V_{bias}$  is  $(V_{IH}-V_{IL})/2$

## HCSL Output Characteristics

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
$V_{OH}$	Output Voltage High <sup>(1)</sup>	Statistical measurement on single-ended signal using oscilloscope math function	660	774	900	mV
$V_{OL}$	Output Voltage Low <sup>(1)</sup>		-150		150	mV
$V_{OMAX}$	Output Voltage Maximum <sup>(1)</sup>	Measurement on single ended signal using absolute value		821	1150	mV
$V_{OMIN}$	Output Voltage Minimum <sup>(1)</sup>		-300	-15		mV
$V_{OSWING}$	Output Swing Voltage <sup>(1,2,3)</sup>	Scope averaging off	300	1536		mV
$V_{OC}$	Output Cross Voltage <sup>(1,2,4)</sup>		250	430	550	mV
$DV_{OC}$	$V_{OC}$ Magnitude Change <sup>(1,2,5)</sup>			12	140	mV

### Note:

1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where  $Q+ = Q-$  measured on a component test board and only applied to the differential rising edge
5. The total variation of all  $V_{cross}$  measurements in any particular system. This is a subset of  $V_{cross\_min/max}$  allowed.

## HCSL Output AC Characteristics

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
$f_{OUT}$	Output Frequency			100		MHz
BW	PLL bandwidth <sup>(1,8)</sup>	-3dB point in High Bandwidth Mode	2	2.7	4	MHz
		-3dB point in Low Bandwidth Mode	1	1.4	2	MHz
$t_{jpeak}$	PLL Jitter Peaking	Peak pass band gain		1.2	2	dB
$t_{RF}$	Slew rate <sup>(1,2,3)</sup>	Scope averaging on fast setting	2.2	3	6	V/ns
		Scope averaging on slow setting	0.4	2	3	V/ns
$D_{tRF}$	Slew rate matching <sup>(1,2,4)</sup>	Scope averaging on		7	20	%
$t_{SKEW}$	Output Skew <sup>(1,2)</sup>	Averaging on, $V_T = 50\%$		43	50	ps
$t_{PDELAY}$	Propagation delay	PLL Bypass mode, $V_T = 50\%$	3000	3600	4500	ps
		PLL mode, $V_T = 50\%$	0	90	200	ps
$t_{j-c-c}$	Cycle to cycle jitter <sup>(1,2)</sup>			14	50	ps
$t_{jPHASE}$	Integrated phase jitter (RMS) <sup>(1,5,6)</sup>	PCIe Gen 1	20	22	86	ps
		PCIe Gen 2 Low Band, $10kHz < f < 1.5MHz$	0.2	0.3	3.0	ps
		PCIe Gen 2 High Band, $1.5MHz < f < Nyquist (50MHz)$	1.6	2.0	3.1	ps
		PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.3	0.35	1.0	ps
		125MHz, 1.5MHz to 20MHz, -20dB/decade Rollover < 1.5MHz, -40dB/decade rolloff > 10MHz <sup>9</sup>		1.9	2	ps



### HCSL Output AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t <sub>JPHASEA</sub>	Additive Integrated phase jitter (RMS) <sup>(1,5,10)</sup>	PCIe Gen 1		0.6	5	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz		0.1	0.3	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)		0.05	0.1	ps
		PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)		0.05	0.1	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz) (BW_SEL_TRI=M)		0.03	0.05	ps
		125MHz, 1.5MHz to 20MHz, -20dB/decade Rollover < 1.5MHz, -40dB/decade rolloff > 10MHz		0.15	0.3	ps
t <sub>DC</sub>	Duty Cycle <sup>(1,2)</sup>	Measured differentially, PLL Mode	45	50	55	%
t <sub>DGD</sub>	Duty Cycle Distortion <sup>(1,7)</sup>	Measured differentially, PLL Bypass Mode at 100MHz	-1	0	1	%
t <sub>STARTUP</sub>	Start up time				10	ms
t <sub>LOCK</sub>	PLL lock time				20	ms

**Note:**

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. See <http://www.pcisig.com> for complete specs
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10<sup>-12</sup>
7. Duty cycle distortion is the difference in duty cycle between the out and input clock when the device is operated in the PLL bypass mode
8. The Min and Max values of each BW setting track each other, low BW max will never occur with high BW min
9. Applies to all differential outputs
10. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>]

## SMBus Serial Data Interface

PI6CB18801 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

### Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	See SBMbus Address Selection table			1/0

Note: SMBus address is latched on SADR pin

### How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop bit

### How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

										8 bits	1 bit	1 bit
.....										Data Byte (N+X-1)	NAck	Stop bit

### Byte 0: Output Enable Register<sup>(1)</sup>

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q7_OE	Q7 output enable	RW	1	Low/Low	Enabled
6	Q6_OE	Q6 output enable	RW	1	Low/Low	Enabled
5	Q5_OE	Q5 output enable	RW	1	Low/Low	Enabled
4	Q4_OE	Q4 output enable	RW	1	Low/Low	Enabled
3	Q3_OE	Q3 output enable	RW	1	Low/Low	Enabled
2	Q2_OE	Q2 output enable	RW	1	Low/Low	Enabled
1	Q1_OE	Q1 output enable	RW	1	Low/Low	Enabled
0	Q0_OE	Q0 output enable	RW	1	Low/Low	Enabled

**Note:**

1. A low on these bits will override the OE# pins and force the differential outputs to Low/Low states

### Byte 1: PLL Operating Mode and Output Amplitude Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	PLLMODERB1	PLL Mode Readback Bit1	R	Latch	See PLL Operating Mode Table	
6	PLLMODERB0	PLL Mode Readback Bit0	R	Latch		
5	PLLMODE_SWCTR	Enable SW control of PLL Mode	RW	0	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode
4	PLLMODE1	PLL Mode control Bit1	RW <sup>(1)</sup>	0	See PLL Operating Mode Table	
3	PLLMODE0	PLL Mode control Bit0	RW <sup>(1)</sup>	0		
2	Reserved			1		
1	Amplitude1	Control output amplitude	RW	1	'00' = 0.6V, '01' = 0.7V, '10' = 0.8V, '11' = 0.9V	
0	Amplitude0		RW	0		

**Note:**

1. B1[5] must be set to a 1 for these bits to have any effect on the part

### Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	SLEWRATECTR_Q7	Control slew rate of Q7	RW	1	Slow setting	Fast setting
6	SLEWRATECTR_Q6	Control slew rate of Q6	RW	1	Slow setting	Fast setting
5	SLEWRATECTR_Q5	Control slew rate of Q5	RW	1	Slow setting	Fast setting
4	SLEWRATECTR_Q4	Control slew rate of Q4	RW	1	Slow setting	Fast setting
3	SLEWRATECTR_Q3	Control slew rate of Q3	RW	1	Slow setting	Fast setting
2	SLEWRATECTR_Q2	Control slew rate of Q2	RW	1	Slow setting	Fast setting
1	SLEWRATECTR_Q1	Control slew rate of Q1	RW	1	Slow setting	Fast setting
0	SLEWRATECTR_Q0	Control slew rate of Q0	RW	1	Slow setting	Fast setting

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**Byte 3: Frequency Select Control Register**

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			1		
5	FREQ_SEL_EN	Enable SW selection of frequency	RW	0	SW Freq. selection disabled	SW Freq. selection enabled
4	FSEL1	Freq. Select Bit 1	RW <sup>1</sup>	0	See Frequency Select Table	
3	FSEL0	Freq. Select Bit 0	RW <sup>1</sup>	0		
2	Reserved			1		
1	Reserved			1		
0	SLEWRATESEL FB	Adjust Slew Rate of Feedback signal	RW	1	2.0V/ns	3.0V/ns

**Note:**

1. B1[5] must be set to a 1 for these bits to have any effect on the part

**Byte 4: Reserved**

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:0	Reserved			1		

**Byte 5: Revision and Vendor ID Register**

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Pericom = 0011	
2	PVID3		R	0		
1	PVID3		R	1		
0	PVID3		R	1		

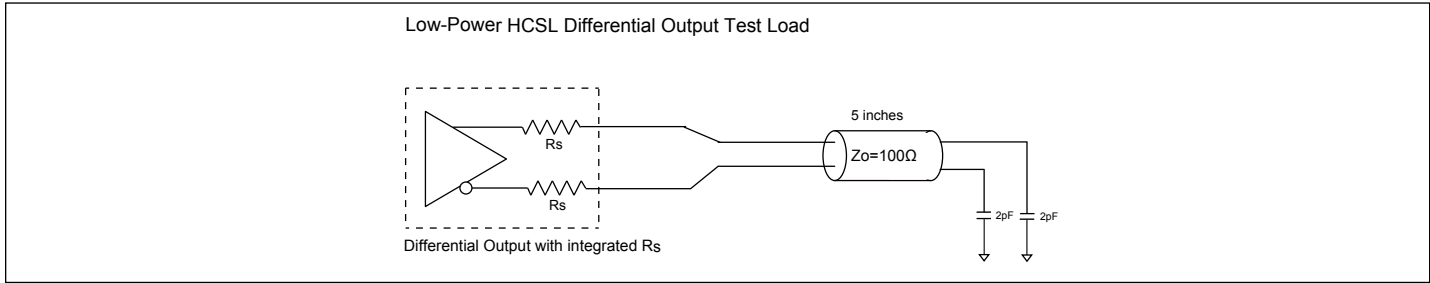
### Byte 6: Device Type/Device ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DTYPE1	Device type	R	0	'00' = CG, '01' = ZDB, '10' = Reserve, '11' = ZDB	
6	DTYPE0		R	1		
5	DID5	Device ID	R	0	001000 binary, 08Hex	
4	DID4		R	0		
3	DID3		R	1		
2	DID2		R	0		
1	DID1		R	0		
0	DID0		R	0		

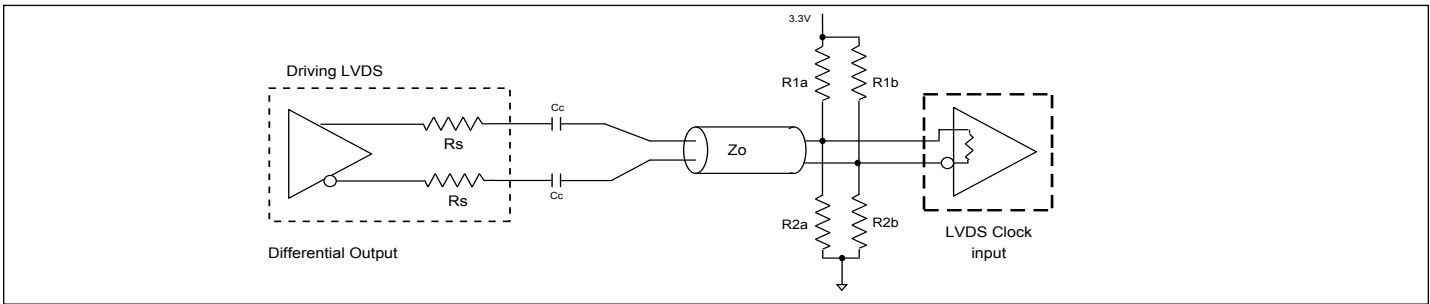
### Byte 7: Byte Count Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

**PI6CB18801**



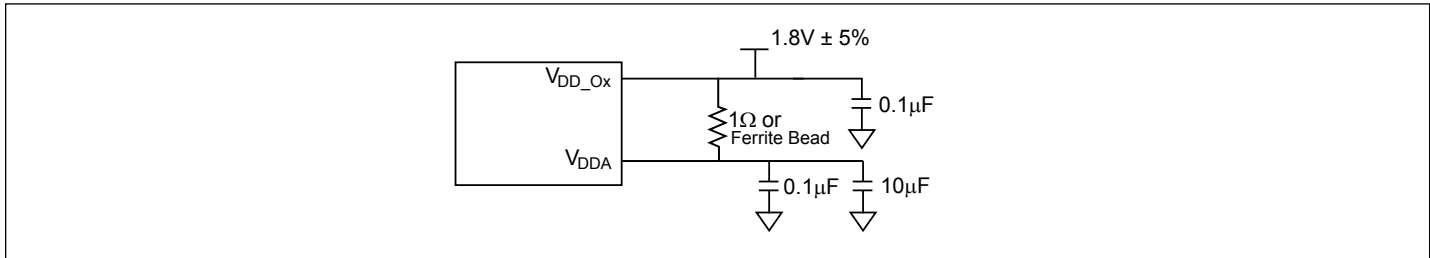
**Figure 1. Low Power HCSL Test Circuit**



**Figure 2. Differential Output driving LVDS**

**Alternate Differential Output Terminations**

Component	Receiver with termination	Receiver without termination	Unit
$R_{1a}, R_{1b}$	10,000	140	$\Omega$
$R_{2a}, R_{2b}$	5,600	75	$\Omega$
$C_c$	0.1	0.1	$\mu F$
$V_{CM}$	1.2	1.2	V



**Figure 3. Power Supply Filter**

**Part Marking**



Y: Die Rev  
YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

**PI6CB18801**

**Packaging Mechanical: 48-TQFN (ZL)**

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e	0.40 BSC		
K	0.35 REF.		
D2	4.45	4.50	4.55
E2	4.45	4.50	4.55
L	0.35	0.40	0.45

**NOTE :**  
 1. ALL DIMENSIONS ARE IN mm, ANGLES IN DEGREES.  
 2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.  
 3. REFER JEDEC MO-220  
 4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.  
 5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

	DATE: 10/26/15
DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZL (ZL48)	
DOCUMENT CONTROL #: PD-2201	REVISION: A

15-0244

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Ordering Code	Package Code	Package Description	Pin 1 Location
PI6CB18801ZLIEEX	ZL	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	Top Right Corner
PI6CB18801ZLIEEX-13R	ZL	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	Top Left Corner

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: <https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf>

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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