

# SA58670A

## 2.1 W/channel stereo class-D audio amplifier

Rev. 02 — 23 October 2008

Product data sheet

### 1. General description

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The SA58670A is a stereo, filter-free class-D audio amplifier which is available in an HVQFN20 package with the exposed Die Attach Paddle (DAP).

The SA58670A features independent shutdown controls for each channel. The gain may be set at 6 dB, 12 dB, 18 dB or 24 dB with gain select pins G0 and G1. Improved immunity to noise and RF rectification is increased by high PSRR and differential circuit topology. Fast start-up time and small package makes it an ideal choice for both cellular handsets and PDAs.

The SA58670A delivers 1.4 W/channel at 5.0 V and 720 mW/channel at 3.6 V into 8  $\Omega$ . It delivers 2.1 W/channel at 5.0 V into 4  $\Omega$ . The maximum power efficiency is excellent at 70 % to 74 % into 4  $\Omega$  and 84 % to 88 % into 8  $\Omega$ . The SA58670A provides thermal and short-circuit shutdown protection.

### 2. Features

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- Output power:
  - ◆ 2.1 W/channel into 4  $\Omega$  at 5.0 V
  - ◆ 1.4 W/channel into 8  $\Omega$  at 5.0 V
  - ◆ 720 mW/channel into 8  $\Omega$  at 3.6 V
- Supply voltage: 2.5 V to 5.5 V
- Independent shutdown control for each channel
- Selectable gain: 6 dB, 12 dB, 18 dB and 24 dB
- High SVRR: -77 dB at 217 Hz
- Fast start-up time: 3.5 ms
- Low supply current
- Low shutdown current
- Short-circuit and thermal protection
- Space savings with 4 mm  $\times$  4 mm HVQFN20 package
- Low junction to ambient thermal resistance of 24 K/W with exposed DAP

### 3. Applications

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- Wireless and cellular handset and PDA
- Portable DVD player
- USB speaker
- Notebook PC
- Portable radio and gaming

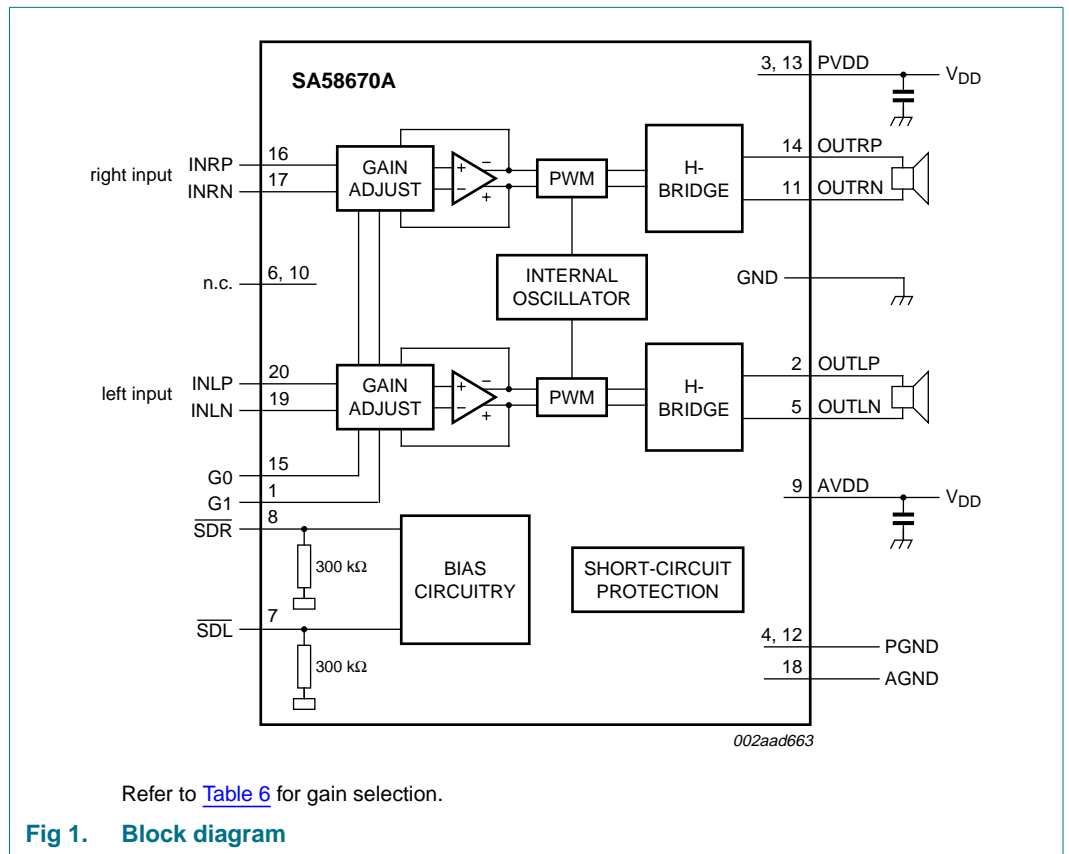
■ Educational toy

### 4. Ordering information

Table 1. Ordering information

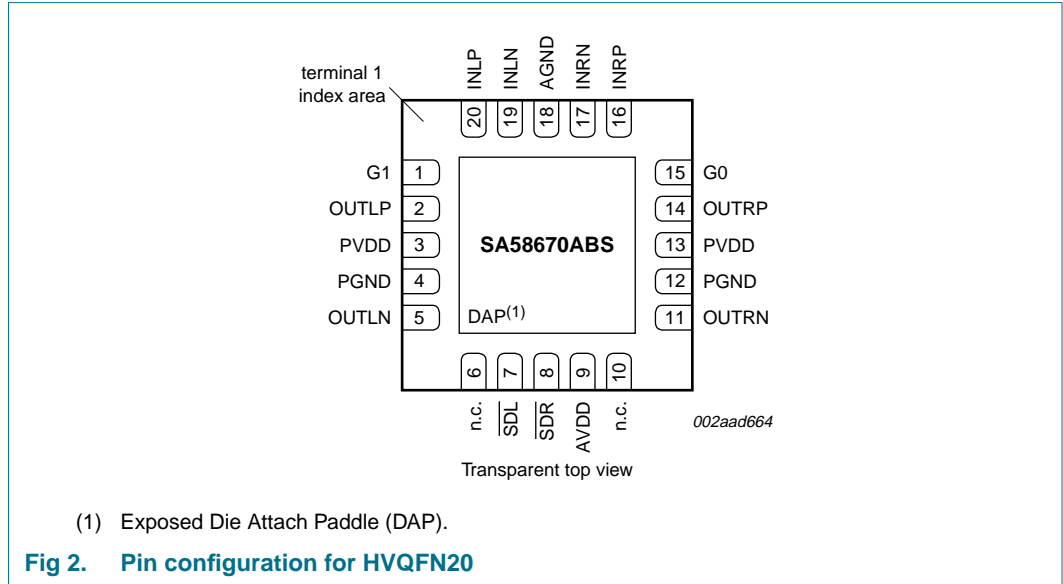
| Type number | Package |  | Version  |
|-------------|---------|--|----------|
|             | Name    | Description  |          |
| SA58670ABS  | HVQFN20 | plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 × 4 × 0.85 mm | SOT917-1 |

### 5. Block diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

| Symbol           | Pin | Description                                |
|------------------|-----|--|
| G1               | 1   | gain select input 1                        |
| OUTLP            | 2   | left channel positive output               |
| PVDD             | 3   | power supply voltage (level same as AVDD)  |
| PGND             | 4   | power ground                               |
| OUTLN            | 5   | left channel negative output               |
| n.c.             | 6   | not connected                              |
| $\overline{SDL}$ | 7   | left channel shutdown input (active LOW)   |
| $\overline{SDR}$ | 8   | right channel shutdown input (active LOW)  |
| AVDD             | 9   | analog supply voltage (level same as PVDD) |
| n.c.             | 10  | not connected                              |
| OUTRN            | 11  | right channel negative output              |
| PGND             | 12  | power ground                               |
| PVDD             | 13  | power supply voltage (level same as AVDD)  |
| OUTRP            | 14  | right channel positive output              |
| G0               | 15  | gain select input 0                        |
| INRP             | 16  | right channel positive input               |
| INRN             | 17  | right channel negative input               |
| AGND             | 18  | analog ground                              |

Table 2. Pin description ...continued

| Symbol | Pin   | Description  |
|--------|-------|--|
| INLN   | 19    | left channel negative input                                      |
| INLP   | 20    | left channel positive input                                      |
| -      | (DAP) | exposed die attach paddle; connect to ground plane heat spreader |

## 7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

| Symbol           | Parameter                       | Conditions                | Min   | Max                   | Unit |
|------------------|---------------------------------|---------------------------|-------|-----------------------|------|
| V <sub>DD</sub>  | supply voltage                  | Active mode               | -0.3  | +6.0                  | V    |
|                  |                                 | Shutdown mode             | -0.3  | +7.0                  | V    |
| V <sub>I</sub>   | input voltage                   | pin SD $\bar{L}$          | GND   | V <sub>DD</sub>       | V    |
|                  |                                 | pin SDR                   | GND   | V <sub>DD</sub>       | V    |
|                  |                                 | other pins                | -0.3  | V <sub>DD</sub> + 0.3 | V    |
| P                | power dissipation               | derating factor 41.6 mW/K |       |                       |      |
|                  |                                 | T <sub>amb</sub> = 25 °C  | -     | 5.2                   | W    |
|                  |                                 | T <sub>amb</sub> = 75 °C  | -     | 3.12                  | W    |
|                  |                                 | T <sub>amb</sub> = 85 °C  | -     | 2.7                   | W    |
| T <sub>amb</sub> | ambient temperature             | operating in free air     | -40   | +85                   | °C   |
| T <sub>j</sub>   | junction temperature            | operating                 | -40   | +150                  | °C   |
| T <sub>stg</sub> | storage temperature             |                           | -65   | +85                   | °C   |
| V <sub>esd</sub> | electrostatic discharge voltage | human body model          | ±2000 | -                     | V    |
|                  |                                 | machine model             | ±200  | -                     | V    |

[1] V<sub>DD</sub> is the supply voltage on pins PVDD and pin AVDD.  
GND is the voltage ground on pins PGND and pin AGND.

## 8. Static characteristics

**Table 4. Static characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified<sup>[1]</sup>.

| Symbol                                    | Parameter                        | Conditions   | Min  | Typ | Max            | Unit             |
|---|----------------------------------|--|------|-----|----------------|------------------|
| $V_{DD}$                                  | supply voltage                   | operating  | 2.5  | -   | 5.5            | V                |
| $I_{DD}$                                  | supply current                   | $V_{DD} = 2.5\text{ V}$ ; no load  | -    | 4   | 6              | mA               |
|   |                                  | $V_{DD} = 3.6\text{ V}$ ; no load  | -    | 5   | 7.5            | mA               |
|   |                                  | $V_{DD} = 5.5\text{ V}$ ; no load  | -    | 6   | 9              | mA               |
| $I_{DD(sd)}$                              | shutdown mode supply current     | no input signal;<br>$V_{SDR} = V_{SDL} = \text{GND}$   | -    | 10  | 1000           | nA               |
| PSRR                                      | power supply rejection ratio     | $V_{DD} = 2.5\text{ V}$ to $5.5\text{ V}$  | -    | -75 | -55            | dB               |
| $V_{i(cm)}$                               | common-mode input voltage        |  | 0.5  | -   | $V_{DD} - 0.8$ | V                |
| CMRR                                      | common mode rejection ratio      | inputs are shorted together;<br>$V_{DD} = 2.5\text{ V}$ to $5.5\text{ V}$  | -    | -69 | -50            | dB               |
| $V_{IH}$                                  | HIGH-level input voltage         | $V_{DD} = 2.5\text{ V}$ to $5.5\text{ V}$ ;<br>pins SDL, SDR, G0, G1   | 1.3  | -   | $V_{DD}$       | V                |
| $V_{IL}$                                  | LOW-level input voltage          | $V_{DD} = 2.5\text{ V}$ to $5.5\text{ V}$ ;<br>pins SDL, SDR, G0, G1   | 0    | -   | 0.35           | V                |
| $I_{IH}$                                  | HIGH-level input current         | $V_{DD} = 5.5\text{ V}$ ; $V_I = V_{DD}$   | -    | -   | 50             | $\mu\text{A}$    |
| $I_{IL}$                                  | LOW-level input current          | $V_{DD} = 5.5\text{ V}$ ; $V_I = 0\text{ V}$   | -    | -   | 5              | $\mu\text{A}$    |
| $f_{sw}$                                  | switching frequency              | $V_{DD} = 2.5\text{ V}$ to $5.5\text{ V}$  | 250  | 300 | 350            | kHz              |
| $G_{v(cl)}$                               | closed-loop voltage gain         | $V_{G0} = V_{G1} = 0.35\text{ V}$  | 5.5  | 6   | 6.5            | dB               |
|   |                                  | $V_{G0} = V_{DD}$ ; $V_{G1} = 0.35\text{ V}$   | 11.5 | 12  | 12.5           | dB               |
|   |                                  | $V_{G0} = 0.35\text{ V}$ ; $V_{G1} = V_{DD}$   | 17.5 | 18  | 18.5           | dB               |
|   |                                  | $V_{G0} = V_{G1} = V_{DD}$   | 23.5 | 24  | 24.5           | dB               |
| <b>Pins OUTLP, OUTLN, OUTRP and OUTRN</b> |                                  |  |      |     |                |                  |
| $R_{DSon}$                                | drain-source on-state resistance | $V_{DD} = 2.5\text{ V}$  | -    | 700 | -              | $\text{m}\Omega$ |
|   |                                  | $V_{DD} = 3.6\text{ V}$  | -    | 570 | -              | $\text{m}\Omega$ |
|   |                                  | $V_{DD} = 5.5\text{ V}$  | -    | 500 | -              | $\text{m}\Omega$ |
| $ V_{O(offset)} $                         | output offset voltage            | measured differentially; inputs<br>AC grounded; $G_{v(cl)} = 6\text{ dB}$ ;<br>$V_{DD} = 2.5\text{ V}$ to $5.5\text{ V}$ | -    | 5   | 10             | mV               |
| $Z_{o(sd)}$                               | shutdown mode output impedance   | $V_{SDR} = V_{SDL} = 0.35\text{ V}$  | -    | 2   | -              | $\text{k}\Omega$ |

[1]  $V_{DD}$  is the supply voltage on pins PVDD and pin AVDD.

GND is the ground supply voltage on pins PGND and pin AGND.

## 9. Dynamic characteristics

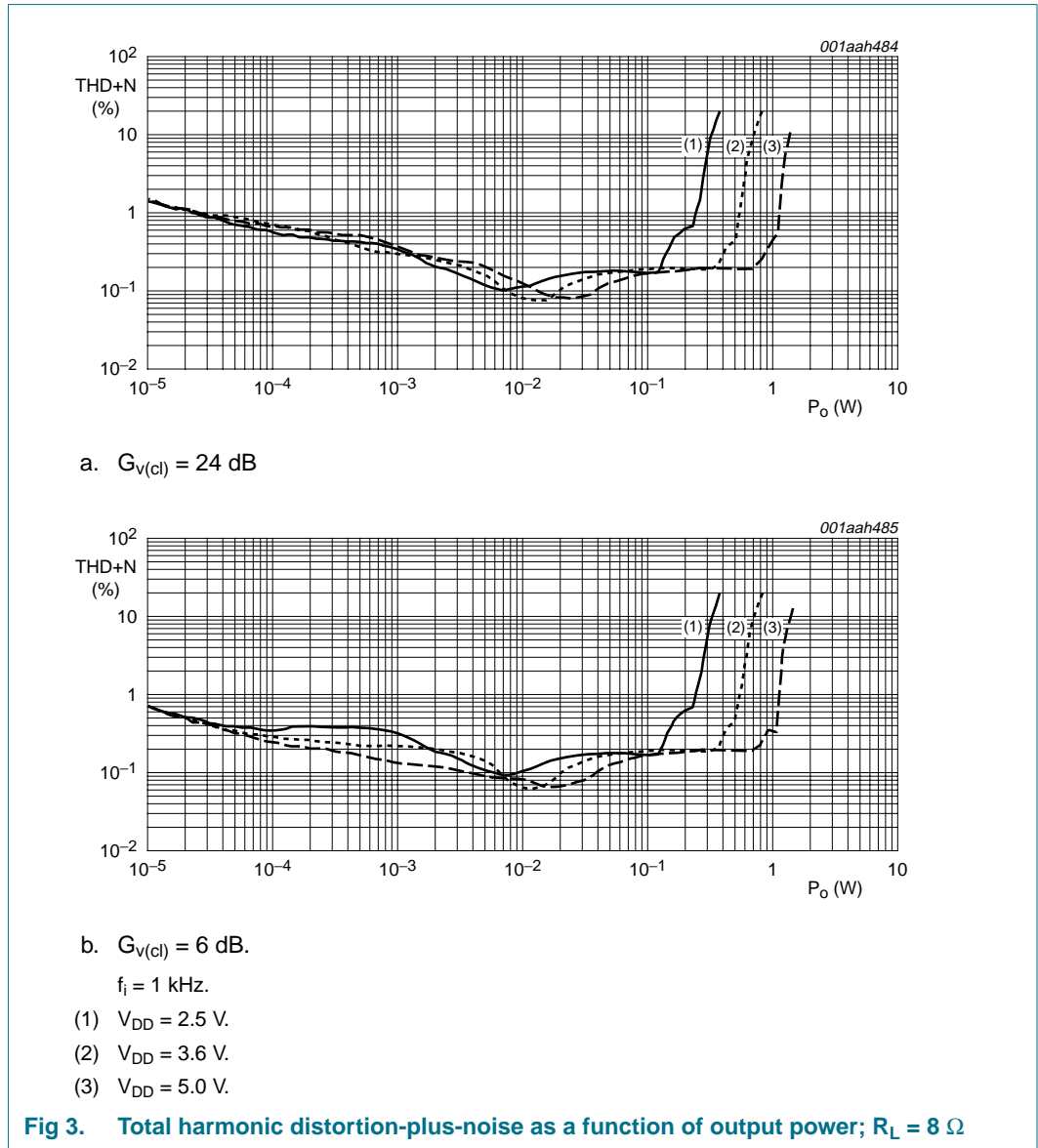
**Table 5. Dynamic characteristics**

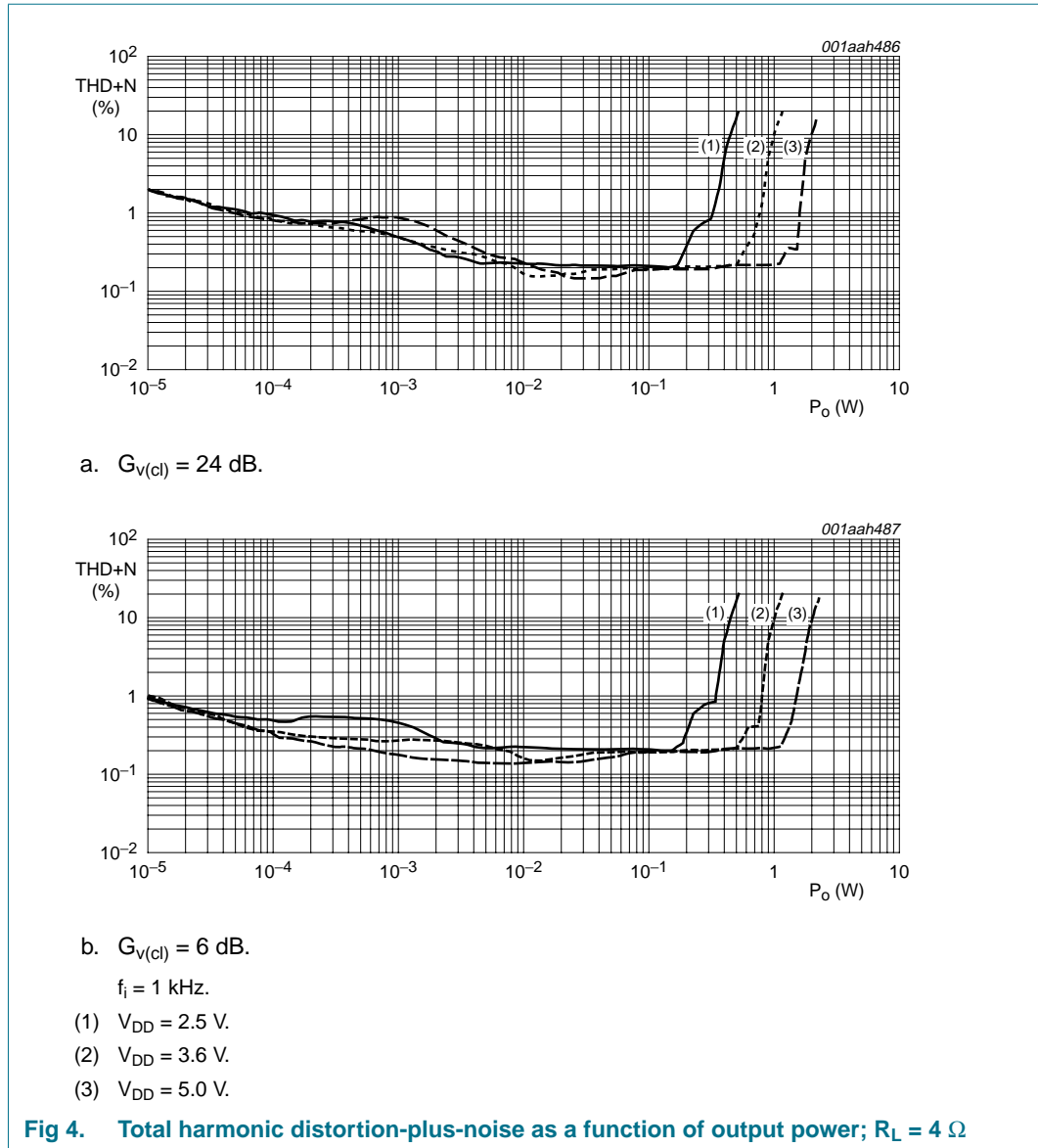
$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $R_L = 8\ \Omega$ ; unless otherwise specified<sup>[1]</sup>.

| Symbol              | Parameter                            | Conditions   | Min | Typ  | Max | Unit          |
|---------------------|--------------------------------------|--|-----|------|-----|---------------|
| $P_o$               | output power                         | per channel; $f = 1\text{ kHz}$ ; THD+N = 10 %   |     |      |     |               |
|                     |                                      | $R_L = 8\ \Omega$ ; $V_{DD} = 3.6\text{ V}$  | -   | 0.72 | -   | W             |
|                     |                                      | $R_L = 8\ \Omega$ ; $V_{DD} = 5.0\text{ V}$  | -   | 1.4  | -   | W             |
|                     |                                      | $R_L = 4\ \Omega$ ; $V_{DD} = 5.0\text{ V}$  | -   | 2.1  | -   | W             |
| THD+N               | total harmonic distortion-plus-noise | $V_{DD} = 5.0\text{ V}$ ; $G_{V(cl)} = 6\text{ dB}$ ; $f = 1\text{ kHz}$                 |     |      |     |               |
|                     |                                      | $P_o = 0.5\text{ W}$   | -   | 0.11 | -   | %             |
|                     |                                      | $P_o = 1.0\text{ W}$   | -   | 0.14 | -   | %             |
| SVRR                | supply voltage ripple rejection      | $G_{V(cl)} = 6\text{ dB}$ ; $f = 217\text{ Hz}$  |     |      |     |               |
|                     |                                      | $V_{DD} = 3.6\text{ V}$  | -   | -73  | -   | dB            |
|                     |                                      | $V_{DD} = 5.0\text{ V}$  | -   | -77  | -   | dB            |
| CMRR                | common mode rejection ratio          | $V_{DD} = 5.0\text{ V}$ ; $G_{V(cl)} = 6\text{ dB}$ ; $f = 217\text{ Hz}$                | -   | -69  | -   | dB            |
| $Z_i$               | input impedance                      | $G_{V(cl)} = 6\text{ dB}$  | -   | 28.1 | -   | k $\Omega$    |
|                     |                                      | $G_{V(cl)} = 12\text{ dB}$   | -   | 17.3 | -   | k $\Omega$    |
|                     |                                      | $G_{V(cl)} = 18\text{ dB}$   | -   | 9.8  | -   | k $\Omega$    |
|                     |                                      | $G_{V(cl)} = 24\text{ dB}$   | -   | 5.2  | -   | k $\Omega$    |
| $t_{d(sd-startup)}$ | delay time from shutdown to start-up | $V_{DD} = 3.6\text{ V}$  | -   | 3.5  | -   | ms            |
| $V_{n(o)}$          | output noise voltage                 | $V_{DD} = 3.6\text{ V}$ ; $f = 20\text{ Hz}$ to $20\text{ kHz}$ ; inputs are AC grounded |     |      |     |               |
|                     |                                      | no weighting   | -   | 35   | -   | $\mu\text{V}$ |
|                     |                                      | A weighting  | -   | 27   | -   | $\mu\text{V}$ |

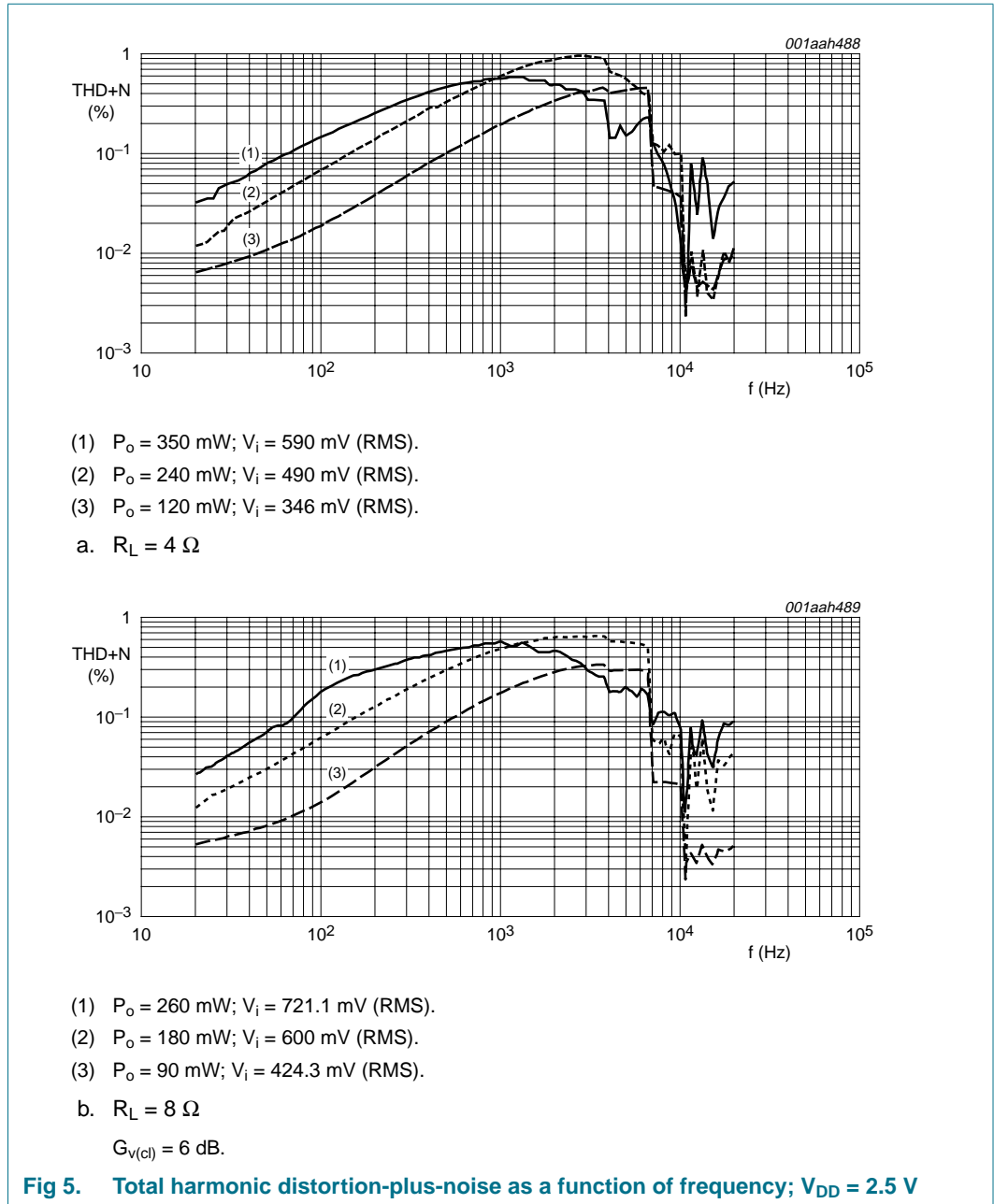
[1]  $V_{DD}$  is the supply voltage on pins PVDD and pin AVDD.

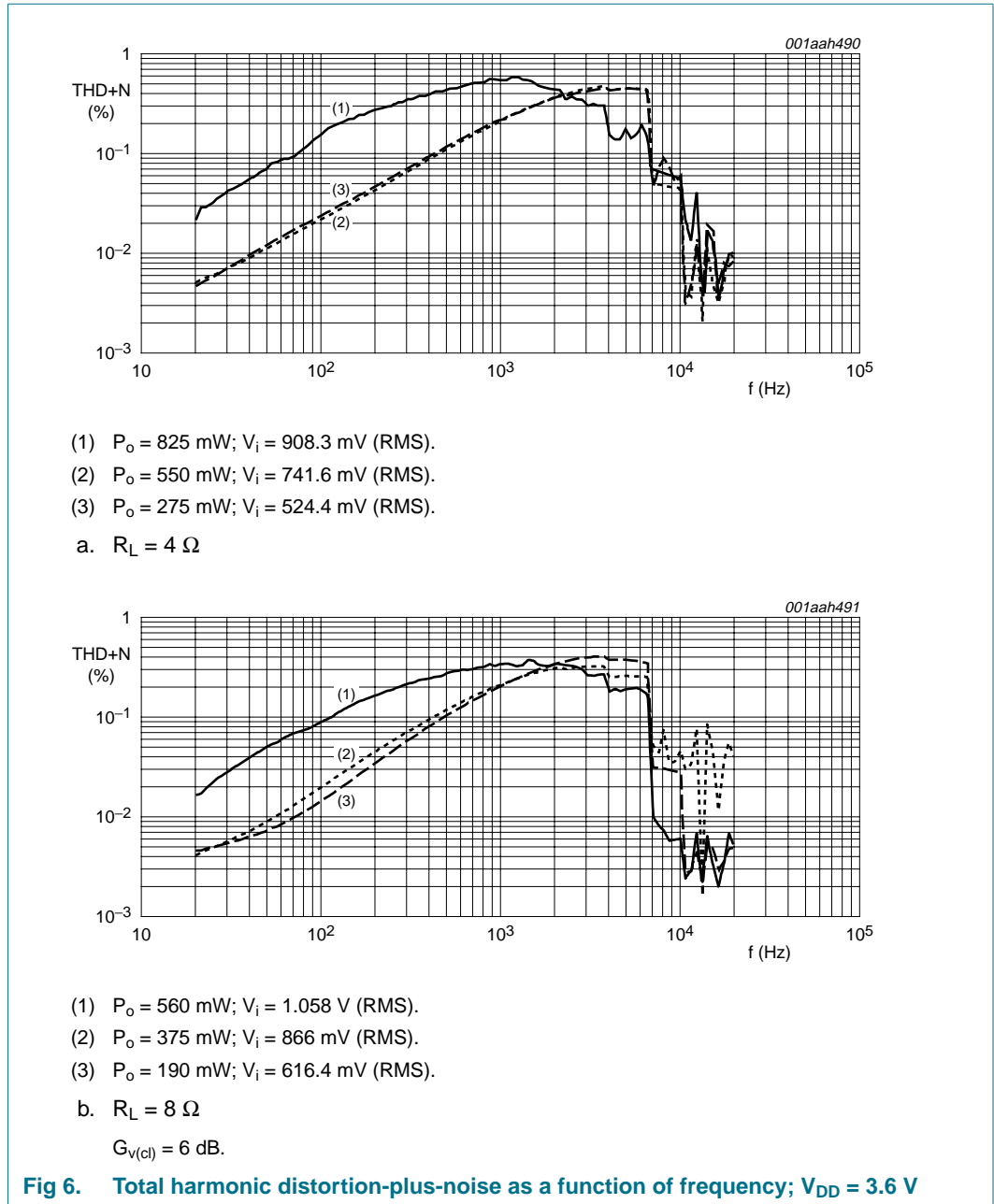
10. Typical performance curves

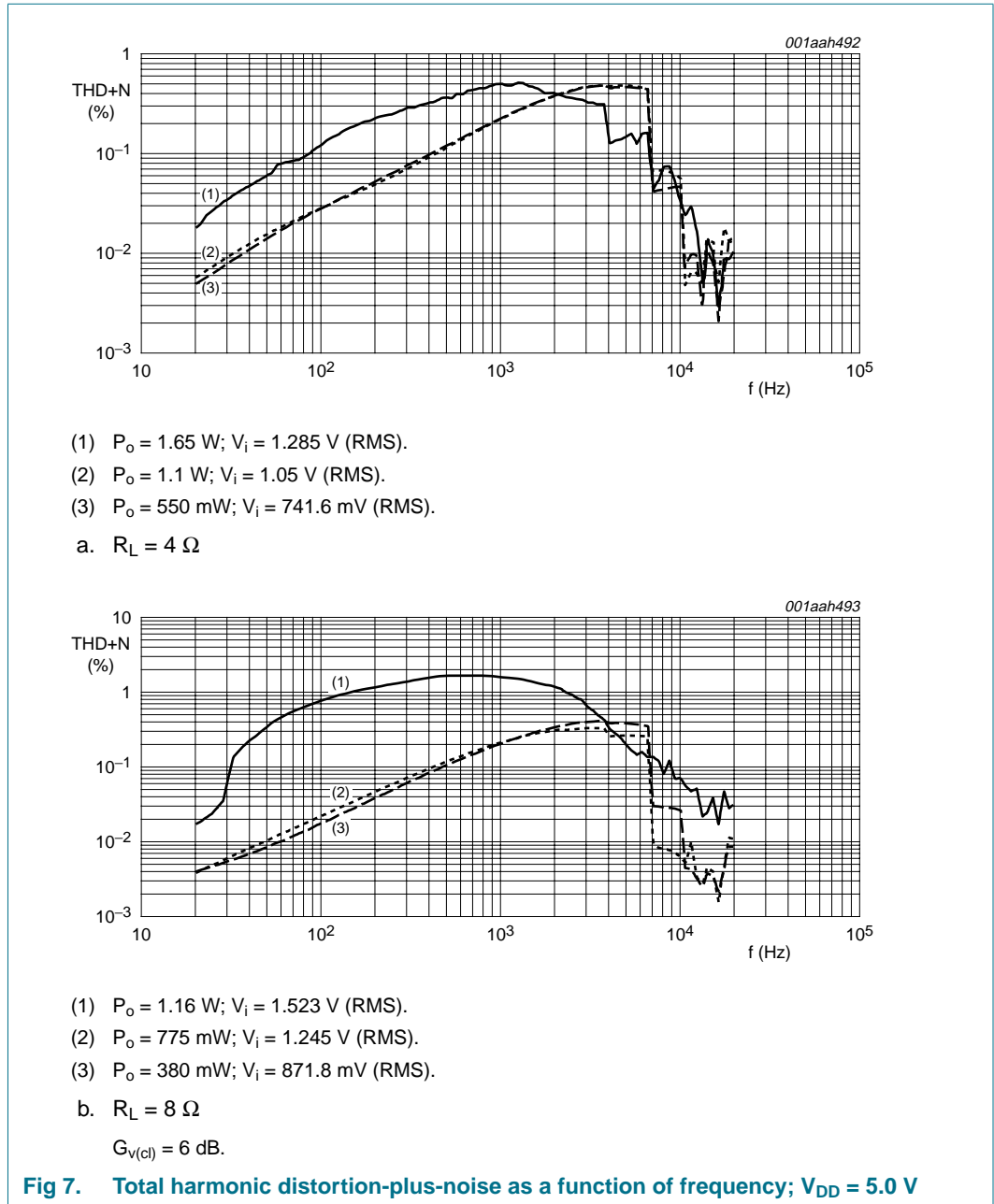


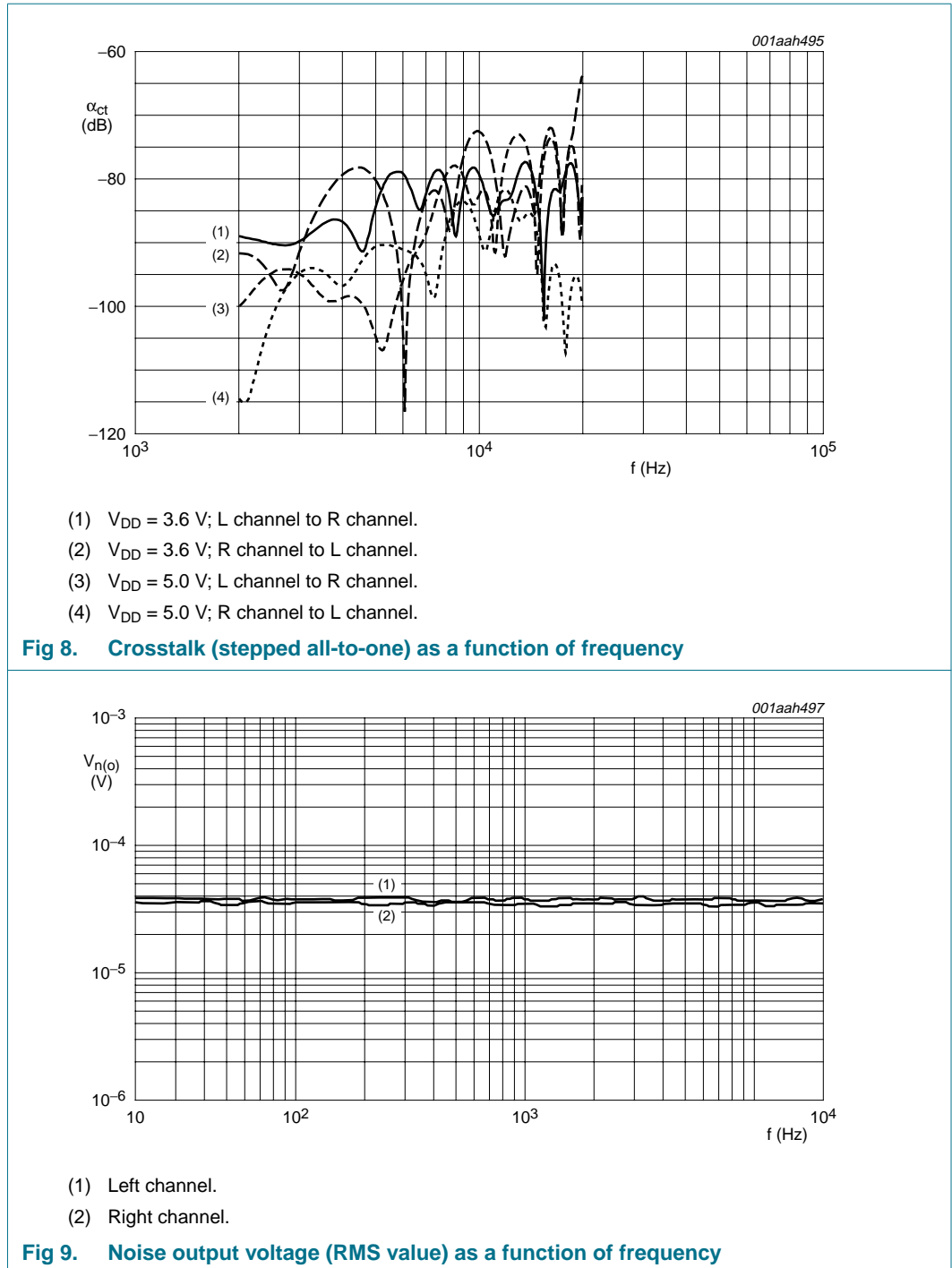


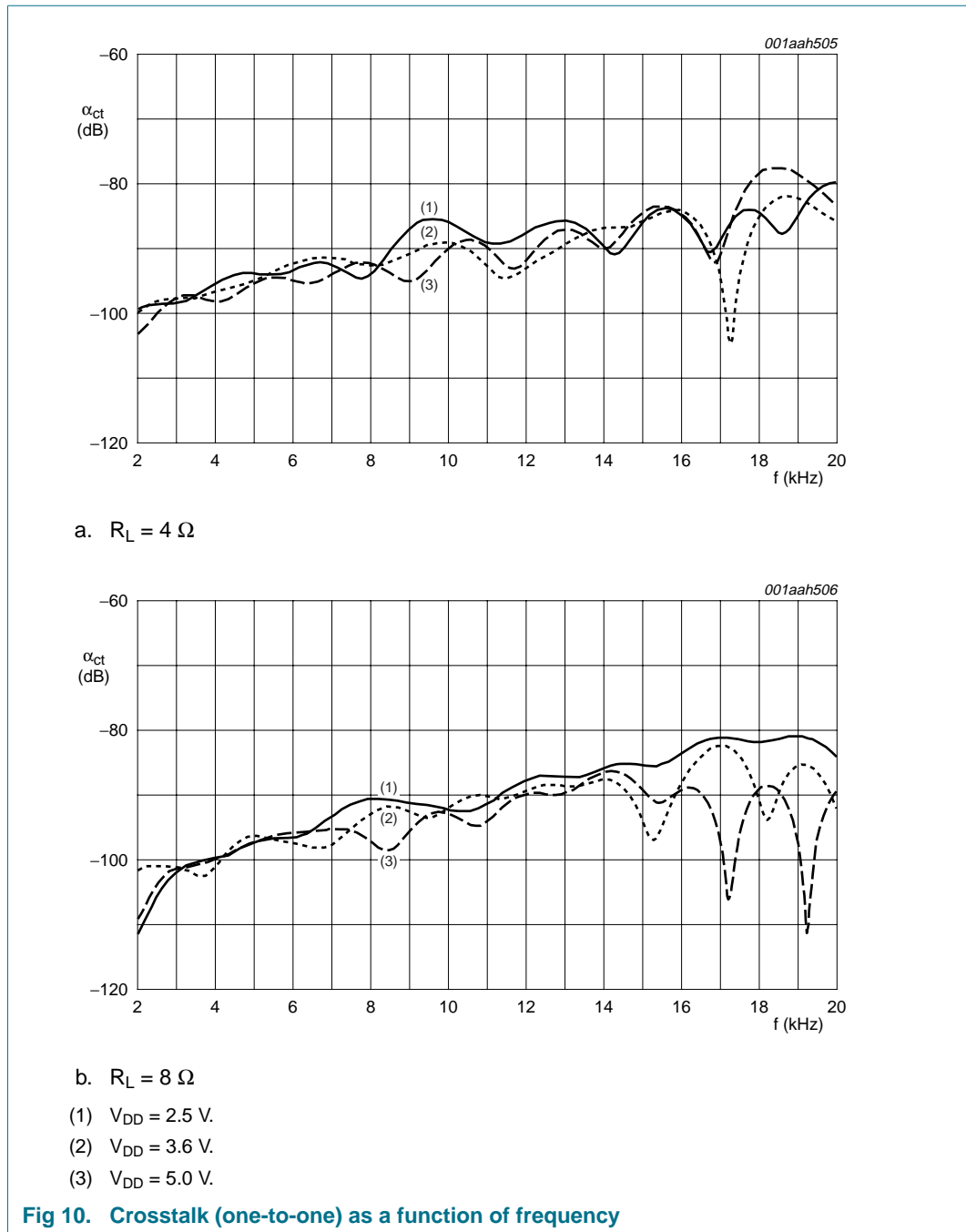












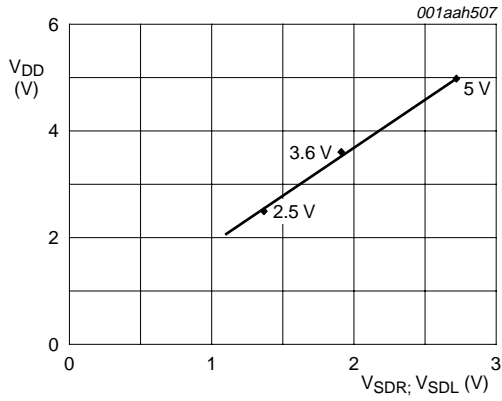
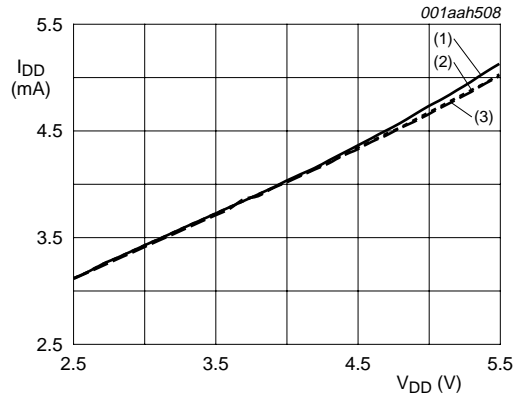
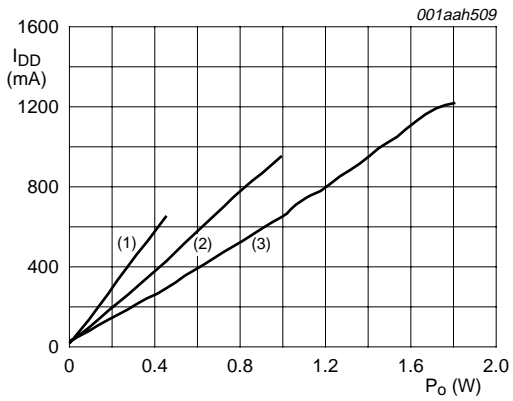


Fig 11. Supply voltage as a function of shutdown voltage



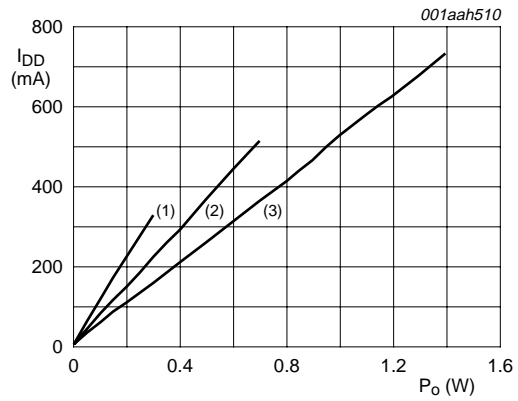
- (1) left channel;  $R_L = 8 \Omega$ .
- (2) right channel;  $R_L = 4 \Omega$ .
- (3) right channel;  $R_L = 8 \Omega$ .

Fig 12. Supply current as a function of supply voltage



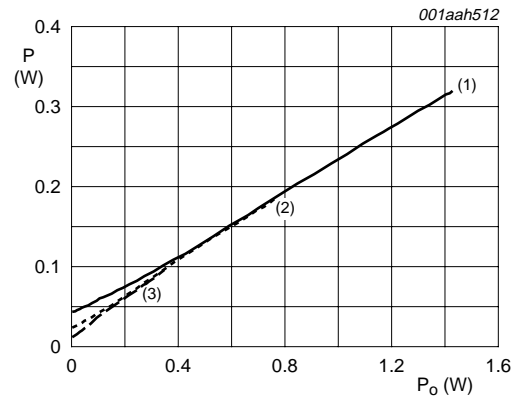
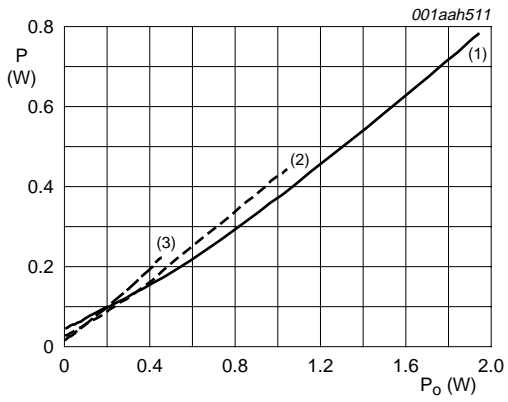
a.  $R_L = 4 \Omega$

- (1)  $V_{DD} = 2.5 \text{ V}$ .
- (2)  $V_{DD} = 3.6 \text{ V}$ .
- (3)  $V_{DD} = 5.0 \text{ V}$ .



b.  $R_L = 8 \Omega$

Fig 13. Supply current as a function of output power



a.  $R_L = 4 \Omega$

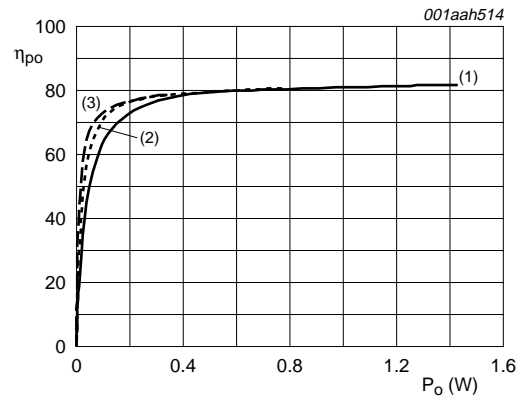
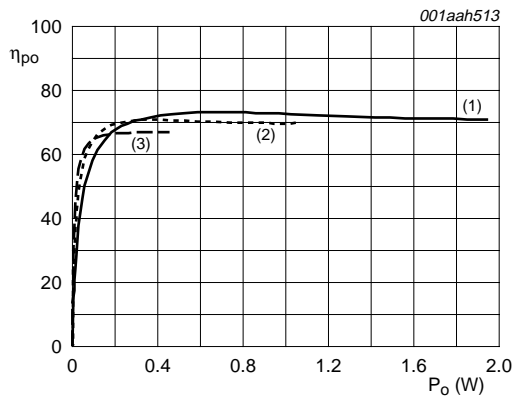
(1)  $V_{DD} = 5.0 \text{ V}$ .

(2)  $V_{DD} = 3.6 \text{ V}$ .

(3)  $V_{DD} = 2.5 \text{ V}$ .

b.  $R_L = 8 \Omega$

Fig 14. Power dissipation as a function of output power



a.  $R_L = 4 \Omega$

(1)  $V_{DD} = 5.0 \text{ V}$ .

(2)  $V_{DD} = 3.6 \text{ V}$ .

(3)  $V_{DD} = 2.5 \text{ V}$ .

b.  $R_L = 8 \Omega$

Fig 15. Output power efficiency as a function of output power

## 11. Application information

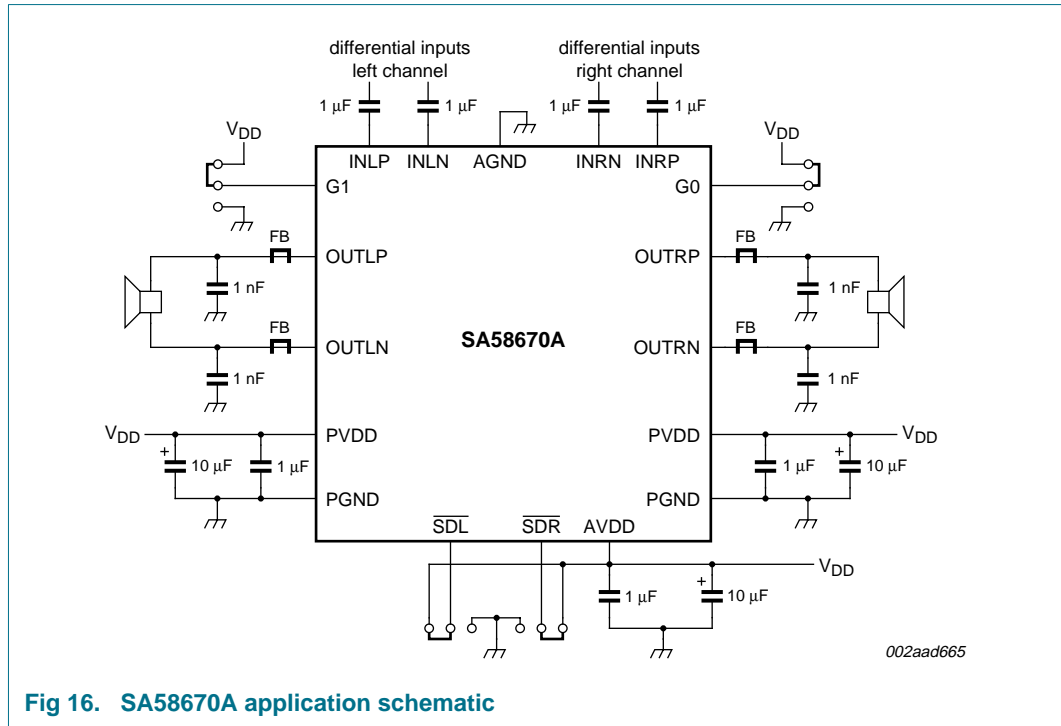


Fig 16. SA58670A application schematic

### 11.1 Power supply decoupling considerations

The SA58670A is a stereo class-D audio amplifier that requires proper supply voltage decoupling to ensure the rated performance for THD+N and power efficiency. To decouple high frequency transients, supply voltage spikes and digital noise on the supply voltage bus line, a low Equivalent Series Resistance (ESR) capacitor of typically 1  $\mu\text{F}$  is placed as close as possible to the PVDD pins of the SA58670A. It is important to place the decoupling capacitor at the supply voltage pins of the SA58670A because any resistance or inductance in the PCB trace between the SA58670A and the capacitor can cause a loss in efficiency. Additional decoupling using a larger capacitor, 4.7  $\mu\text{F}$  or greater, may be done on the supply voltage connection on the PCB to filter low frequency signals. Usually this is not required due to high PSRR of the SA58670A.

### 11.2 Input capacitor selection

The SA58670A does not require input coupling capacitors when used with a differential audio source that is biased from 0.5 V to  $V_{\text{DD}} - 0.8$  V. In other words, the input signal must be biased within the common-mode input voltage ( $V_{i(\text{cm})}$ ) range. If high-pass filtering is required or if it is driven using a single-ended source, input coupling capacitors are required.

The 3 dB cut-off frequency created by the input coupling capacitor and the input resistors (see [Table 6](#)) is calculated by [Equation 1](#):

$$f_{-3\text{dB}} = \frac{1}{2\pi \times R_i \times C_i} \tag{1}$$



**Table 6. Gain selection**

| G1   | G0   | Gain (V/V) | Gain (dB) | Input impedance (kΩ) |
|------|------|------------|-----------|----------------------|
| LOW  | LOW  | 2          | 6         | 28.1                 |
| LOW  | HIGH | 4          | 12        | 17.3                 |
| HIGH | LOW  | 8          | 18        | 9.8                  |
| HIGH | HIGH | 16         | 24        | 5.2                  |

Since the value of the input decoupling capacitor and the input resistance determined by the gain setting affects the low frequency performance of the audio amplifier, it is important to consider this during the system design. Small speakers in wireless and cellular phones usually do not respond well to low frequency signals, so the 3 dB cut-off frequency may be increased to block the low frequency signals to the speakers. Not using input coupling capacitors may increase the output offset voltage.

[Equation 2](#) is solved for  $C_i$ :

$$C_i = \frac{I}{2\pi \times R_i \times f_{-3dB}} \tag{2}$$

### 11.3 PCB layout considerations

Component location is very important for performance of the SA58670A. Place all external components very close to the SA58670A. Placing decoupling capacitors directly at the power supply voltage pins increases efficiency because the resistance and inductance in the trace between the SA58670A power supply voltage pins and the decoupling capacitor causes a loss in power efficiency.

The trace width and routing are also very important for power output and noise considerations.

For high current pins (PVDD, PGND and audio output), the trace widths should be maximized to ensure proper performance and output power. Use at least 500 μm wide traces.

For the input pins (INRP, INRN, INLP and INLN), the traces must be symmetrical and run side-by-side to maximize common-mode cancellation.

### 11.4 Filter-free operation and ferrite bead filters

A ferrite bead low-pass filter can be used to reduce radio frequency emissions in applications that have circuits sensitive to frequencies greater than 1 MHz. A ferrite bead low-pass filter functions well for amplifiers that must pass FCC unintentional radiation requirements for frequencies greater than 30 MHz. Choose a bead with high-impedance at high frequencies and very low-impedance at low frequencies. In order to prevent distortion of the output signal, select a ferrite bead with adequate current rating.

For applications in which there are circuits that are EMI sensitive to low frequencies (< 1 MHz) and there are long leads from amplifier to speaker, it is necessary to use an LC output filter.

11.5 Efficiency and thermal considerations

The maximum ambient operating temperature depends on the heat transferring ability of the heat spreader on the PCB layout. In [Table 3 "Limiting values"](#), the power derating factor is given as 41.6 mW/K. The device thermal resistance,  $R_{th(j-a)}$  is the reciprocal of the power derating factor. Convert the power derating factor to  $R_{th(j-a)}$  by [Equation 3](#):

$$R_{th(j-a)} = \frac{1}{\text{derating factor}} = \frac{1}{0.0416} = 24 \text{ K/W} \tag{3}$$

For a maximum allowable junction temperature  $T_j = 150 \text{ }^\circ\text{C}$  and  $R_{th(j-a)} = 24 \text{ K/W}$  and a maximum device dissipation of 1.5 W (750 mW per channel) and for 2.1 W per channel output power, 4  $\Omega$  load, 5 V supply, the maximum ambient temperature is calculated using [Equation 4](#):

$$T_{amb(max)} = T_{j(max)} - (R_{th(j-a)} \times P_{max}) = 150 - (24 \times 1.5) = 114 \text{ }^\circ\text{C} \tag{4}$$

The maximum ambient temperature is 114  $^\circ\text{C}$  at maximum power dissipation for 5 V supply and 4  $\Omega$  load. If the junction temperature of the SA58670A rises above 150  $^\circ\text{C}$ , the thermal protection circuitry turns the SA58670A off; this prevents damage to IC. Using speakers greater than 4  $\Omega$  further enhances thermal performance and battery lifetime by reducing the output load current and increasing amplifier efficiency.

11.6 Additional thermal information

The SA58670A HVQFN20 package incorporates an exposed DAP that is designed to solder the mount directly to the PCB heat spreader. By the use of thermal vias, the DAP may be soldered directly to a ground plane or special heat sinking layer designed into the PCB. The thickness and area of the heat spreader may be maximized to optimize heat transfer and achieve lowest package thermal resistance.

12. Test information

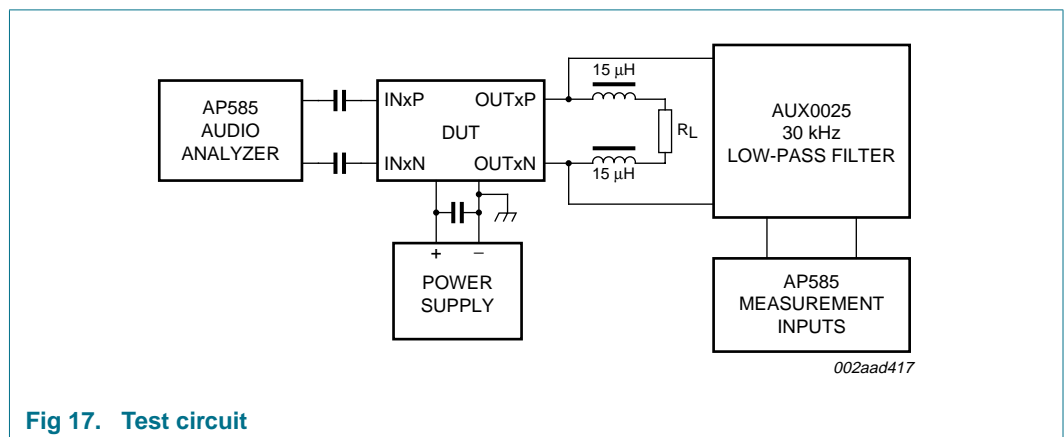


Fig 17. Test circuit

13. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 x 4 x 0.85 mm

SOT917-1

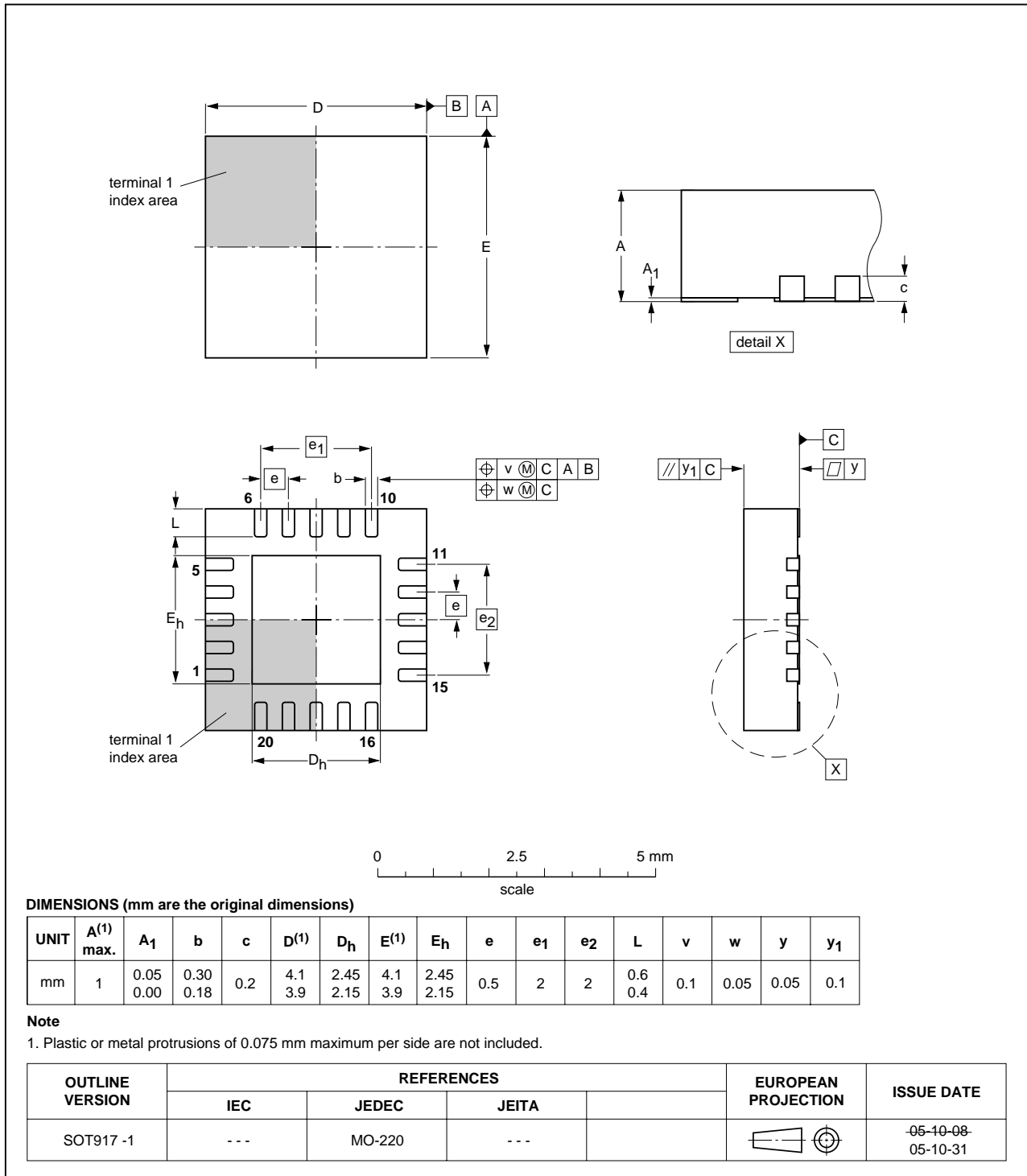


Fig 18. Package outline SOT917-1 (HVQFN20)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 7](#) and [8](#)

**Table 7. SnPb eutectic process (from J-STD-020C)**

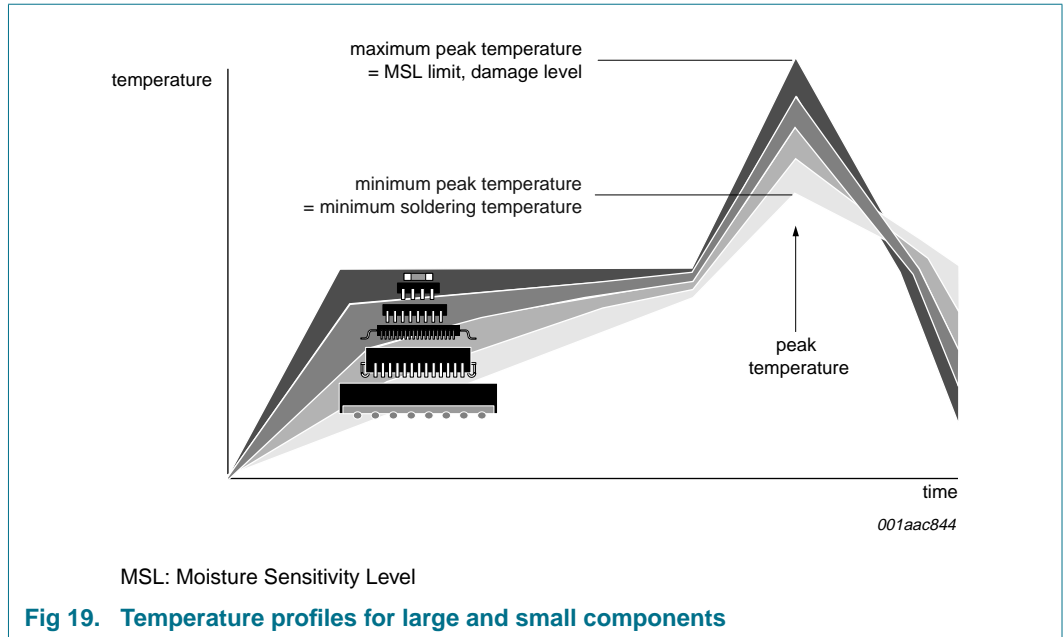
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 8. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15. Abbreviations

**Table 9. Abbreviations**

| Acronym | Description                  |
|---------|------------------------------|
| DAP     | Die Attach Paddle            |
| DVD     | Digital Video Disc           |
| EMI     | ElectroMagnetic Interference |
| ESR     | Equivalent Series Resistance |
| LC      | inductor-capacitor filter    |
| PC      | Personal Computer            |
| PCB     | Printed-Circuit Board        |
| PDA     | Personal Digital Assistant   |
| PWM     | Pulse Width Modulator        |
| USB     | Universal Serial Bus         |

## 16. Revision history

**Table 10. Revision history**

| Document ID    | Release date   | Data sheet status  | Change notice | Supersedes |
|----------------|--|--------------------|---------------|------------|
| SA58670A_2     | 20081023   | Product data sheet | -             | SA58670A_1 |
| Modifications: | <ul style="list-style-type: none"> <li>• <a href="#">Table 4 “Static characteristics”</a>:                             <ul style="list-style-type: none"> <li>– added <math>I_{DD(sd)}</math> specification</li> </ul> </li> </ul> |                    |               |            |
| SA58670A_1     | 20080220   | Product data sheet | -             | -          |

## 17. Legal information

### 17.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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