



# X-PHY® Cyber Secure PCIe M.2 2280 Specification

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# 1. GENERAL DESCRIPTION

## 1.1. INTRODUCTION

FLEXXON X-PHY® CYBER SECURE SSD is the AI-embedded, software-free data protection solution that offers elite-level end-to-end data protection in the forms of a cost effective, standalone SSD that's reliable, predictable and dependable.

Built on advanced AI engine, FLEXXON X-PHY® CYBER SECURE SSD monitors and protects user data in real time and stops security threats including system attacks, physical attacks and ransomware attacks.

## 1.2. PRODUCT OVERVIEW

### ◆ Flash

- ◆ 3D NAND

### ◆ Capacity

- ◆ 512GB ~ 1TB

### ◆ PCIe Interface

- ◆ Compliant with NVMe 1.3
- ◆ Compatible with PCIe I/II/III x4 interface

### ◆ ECC Scheme

- ◆ LDPC (Low Density Parity Check)  
of ECC algorithm

### ◆ GPIO

### ◆ UART

### ◆ Dynamic and Static Wear Leveling

### ◆ Support SMART and TRIM commands

### ◆ Power Loss Protection Algorithm

### ◆ Temperature Range

- ◆ Operation : 0°C ~ 70°C
- ◆ Storage: -40°C ~ 85°C

### ◆ RoHS Compliant



FLEXXON X-PHY® CYBER SECURE PCIe M.2 has PCIe Gen 3x4 interface, and is fully compliant with NVMe 1.3 industrial standard.

## 2. PRODUCT FEATURES

### 2.1. XPHY STREAM PROTECTION™

Lock down the data streams with XPHY STREAM PROTECTION™ – the smart, practical solution to secure the most sensitive communication signals. XPHY STREAM PROTECTION™ monitors data sent through signal communications while giving added layers of physical and cyber security.

Any attempted breach of the data stream will activate the build-in data security system.

### 2.2. XPHY FACTOR ENCRYPTION™

XPHY FACTOR ENCRYPTION™ provides the encryption and 2-factor tools to keep the information safe and secure.

It locks down the data behind advanced 2-factor verification that requires the pairing of multiple unique keys before data can be accessed. It prevents keys from being stolen and used independently to access sensitive data.

It keeps the encryption keys and data safe from cyberattacks by disabling and blocking attacks at the source rendering the secured accounts safe and inaccessible to any users who attempt to login without approved encryption keys.



It disables firmware update attacks and maintains the security of the firmware by only allowing updates that have been approved for the firmware's unique number.

## 2. PRODUCT FEATURES

### 2.3. XPHY GUARD™

XPHY GUARD™ keeps data secure by keeping SSD free and clear from virus, malware and ransomware.

It uses AI algorithms to detect and stop different types of ransomware from breaching the most secure data. Data transfer is faster and more efficient, reducing the possibility of data leaks during file transfers.

### 2.4. XPHY SITE SECURE™

XPHY SITE SECURE™ is the first and last level of defense against physical attacks on data.

It monitors the power, temperature and motion of SSD, and springs into action at the chance of any threat.



### 2.5. XPHY FORENSIC™

XPHY FORENSIC™ protects the most sensitive data, including cryptocurrency transactions, and keeps user in the know about all of the data that is moving around on SSD.

It uses AI processing at the SSD level to increase the drive endurance and reliability while greatly enhancing file move speed.

## 3. PERFORMANCE

**Table 3-1 Performance of X-PHY PCIe M.2 2280**

| Capacity | Sequential  |              |
|----------|-------------|--------------|
|          | Read (MB/s) | Write (MB/s) |
| 512GB    | 2100        | 1900         |
| 1TB      | 2600        | 2400         |

\*Performance may differ according to flash configuration and platform

## 4. PIN ASSIGNMENT

**Table 4-1 Pin Assignment and Description of X-PHY PCIe M.2 2280**

| Pin No. | PCIe Pin | Description                                                                                                                                                      |
|---------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | GND      | CONFIG_3 = GND                                                                                                                                                   |
| 2       | 3.3V     | 3.3V source                                                                                                                                                      |
| 3       | GND      | Ground                                                                                                                                                           |
| 4       | 3.3V     | 3.3V source                                                                                                                                                      |
| 5       | PETn3    | PCIe TX Differential signal defined by PCI Express M.2 spec                                                                                                      |
| 6       | N/C      | No connect                                                                                                                                                       |
| 7       | PETp3    | PCIe TX Differential signal defined by PCI Express M.2 spec                                                                                                      |
| 8       | N/C      | No connect                                                                                                                                                       |
| 9       | GND      | Ground                                                                                                                                                           |
| 10      | LED1#    | Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. |
| 11      | PERn3    | PCIe RX Differential signal defined by PCI Express M.2 spec                                                                                                      |
| 12      | 3.3V     | 3.3V source                                                                                                                                                      |
| 13      | PERp3    | PCIe RX Differential signal defined by PCI Express M.2 spec                                                                                                      |
| 14      | 3.3V     | 3.3V source                                                                                                                                                      |

## 4. PIN ASSIGNMENT

**Table 4-1 Pin Assignment and Description of X-PHY PCIe M.2 2280**

| Pin No. | PCIe Pin | Description                                                 |
|---------|----------|-------------------------------------------------------------|
| 15      | GND      | Ground                                                      |
| 16      | 3.3V     | 3.3V source                                                 |
| 17      | PETn2    | PCIe TX Differential signal defined by PCI Express M.2 spec |
| 18      | 3.3V     | 3.3V source                                                 |
| 19      | PETp2    | PCIe TX Differential signal defined by PCI Express M.2 spec |
| 20      | N/C      | No connect                                                  |
| 21      | GND      | Ground                                                      |
| 22      | N/C      | No connect                                                  |
| 23      | PERn2    | PCIe RX Differential signal defined by PCI Express M.2 spec |
| 24      | N/C      | No connect                                                  |
| 25      | PERp2    | PCIe RX Differential signal defined by PCI Express M.2 spec |
| 26      | N/C      | No connect                                                  |
| 27      | GND      | Ground                                                      |
| 28      | N/C      | No connect                                                  |
| 29      | PETn1    | PCIe TX Differential signal defined by PCI Express M.2 spec |
| 30      | N/C      | No connect                                                  |
| 31      | PETp1    | PCIe TX Differential signal defined by PCI Express M.2 spec |
| 32      | N/C      | No connect                                                  |
| 33      | GND      | Ground                                                      |
| 34      | N/C      | No connect                                                  |
| 35      | PERn1    | PCIe RX Differential signal defined by PCI Express M.2 spec |
| 36      | N/C      | No connect                                                  |
| 37      | PERp1    | PCIe RX Differential signal defined by PCI Express M.2 spec |

## 4. PIN ASSIGNMENT

**Table 4-1 Pin Assignment and Description of X-PHY PCIe M.2 2280**

| Pin No. | PCIe Pin                | Description                                                                                                                          |
|---------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 38      | N/C                     | No connect                                                                                                                           |
| 39      | GND                     | Ground                                                                                                                               |
| 40      | SMB_CLK (I/O) (0/1.8V)  | SMBus Clock; Open Drain with pull-up on platform                                                                                     |
| 41      | PETn0                   | PCIe TX Differential signal defined by PCI Express M.2 spec                                                                          |
| 42      | SMB_DATA (I/O) (0/1.8V) | SMBus Data; Open Drain with pull-up on platform                                                                                      |
| 43      | PETp0                   | PCIe TX Differential signal defined by PCI Express M.2 spec                                                                          |
| 44      | ALERT#(O) (0/1.8V)      | Alert notification to master; Open Drain with pull-up on platform;<br>Active Low                                                     |
| 45      | GND                     | Ground                                                                                                                               |
| 46      | N/C                     | No connect                                                                                                                           |
| 47      | PERn0                   | PCIe RX Differential signal defined by PCI Express M.2 spec                                                                          |
| 48      | N/C                     | No connect                                                                                                                           |
| 49      | PERp0                   | PCIe RX Differential signal defined by PCI Express M.2 spec                                                                          |
| 50      | PERST#(I)(0/3.3V)       | PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.                                            |
| 51      | GND                     | Ground                                                                                                                               |
| 52      | CLKREQ#(I/O)(0/3.3V)    | Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.      |
| 53      | REFCLKn                 | PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.                                                          |
| 54      | PEWAKE#(I/O)(0/3.3V)    | PCIe PME Wake. Open Drain with pull up on platform; Active low                                                                       |
| 55      | REFCLKp                 | PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.                                                          |
| 56      | Reserved for MFG DATA   | Manufacturing Data Line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform socket.  |
| 57      | GND                     | Ground                                                                                                                               |
| 58      | Reserved for MFG CLOCK  | Manufacturing Clock Line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform socket. |

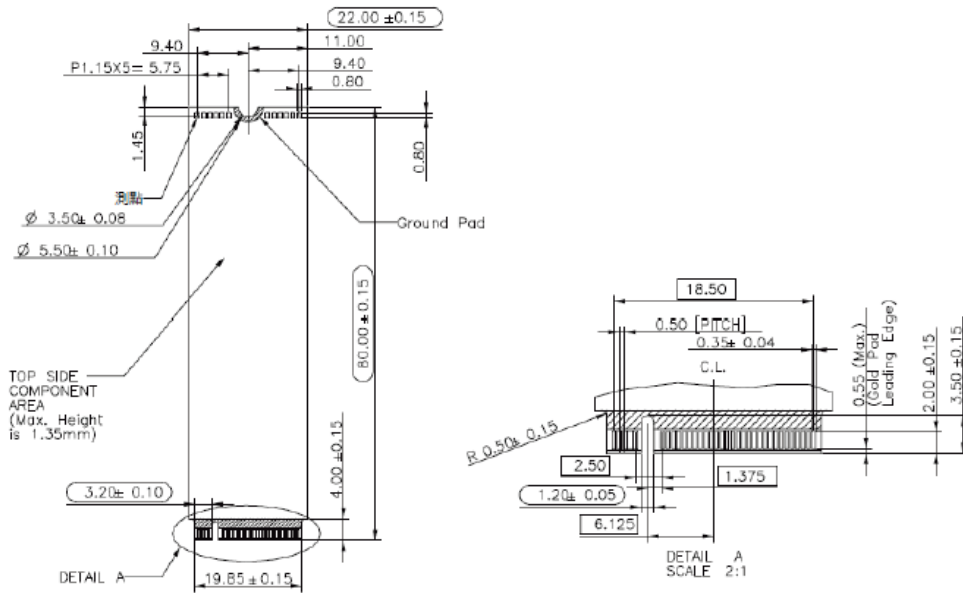
## 4. PIN ASSIGNMENT

**Table 4-1 Pin Assignment and Description of X-PHY PCIe M.2 2280**

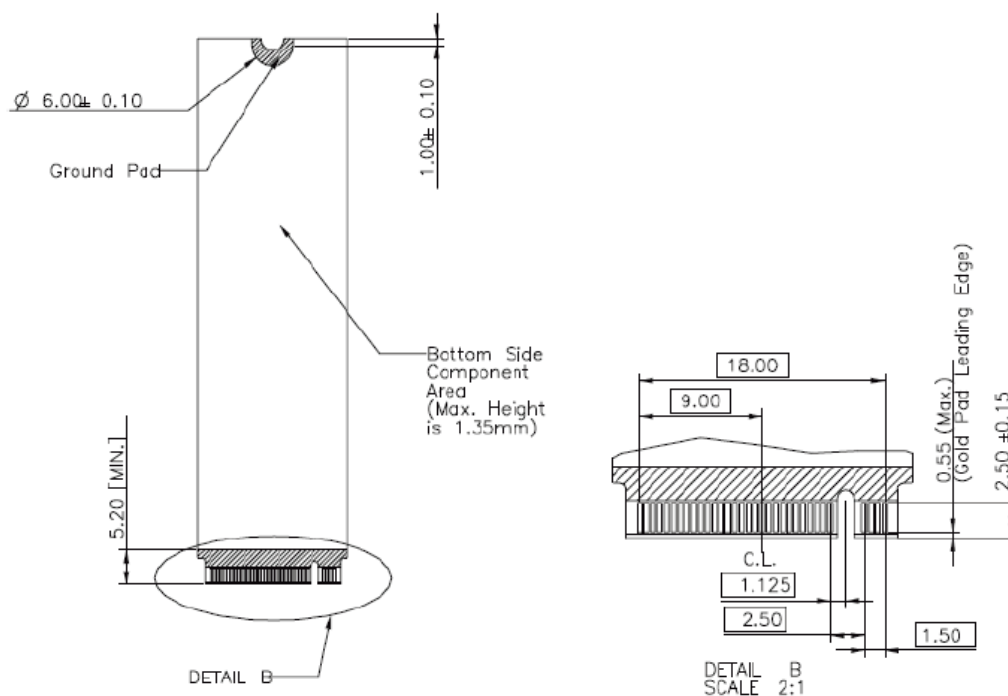
| Pin No. | PCIe Pin     | Description |
|---------|--------------|-------------|
| 59      | Module Key M | Module Key  |
| 60      | Module Key M |             |
| 61      | Module Key M |             |
| 62      | Module Key M |             |
| 63      | Module Key M |             |
| 64      | Module Key M |             |
| 65      | Module Key M |             |
| 66      | Module Key M |             |
| 67      | N/C          | No connect  |
| 68      | SUSCLK       | Not Use     |
| 69      | PEDET        | NC-PCIe     |
| 70      | 3.3V         | 3.3V source |
| 71      | GND          | Ground      |
| 72      | 3.3V         | 3.3 source  |
| 73      | GND          | Ground      |
| 74      | 3.3V         | 3.3V source |
| 75      | GND          | Ground      |

## 5. PHYSICAL DIMENSION

Dimension: 80mm(L) x 22mm(W) x 2.33mm to 3.5mm(H)

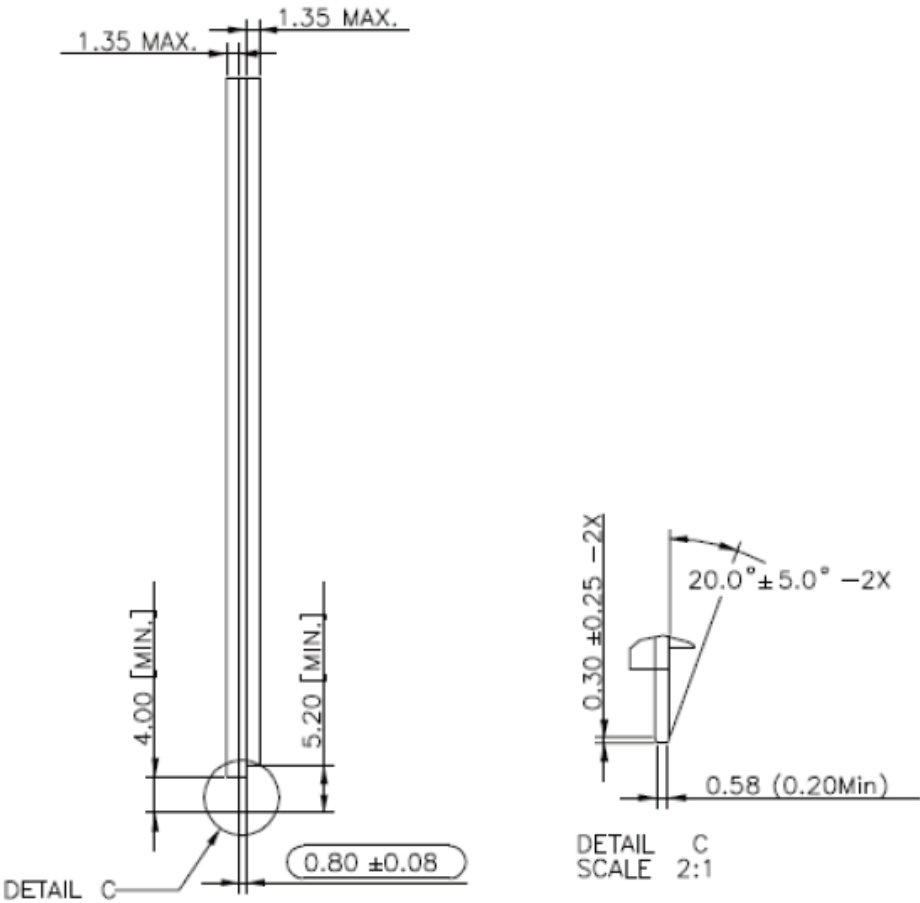


Top View



Bottom View

# 5. PHYSICAL DIMENSION



Side View

## 6. ORDERING INFORMATION

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| Capacity | MPN             |
|----------|-----------------|
| 512GB    | FCS0512GBC-XA00 |
| 1TB      | FCS0001TBC-XA00 |