

AKM

AK5720

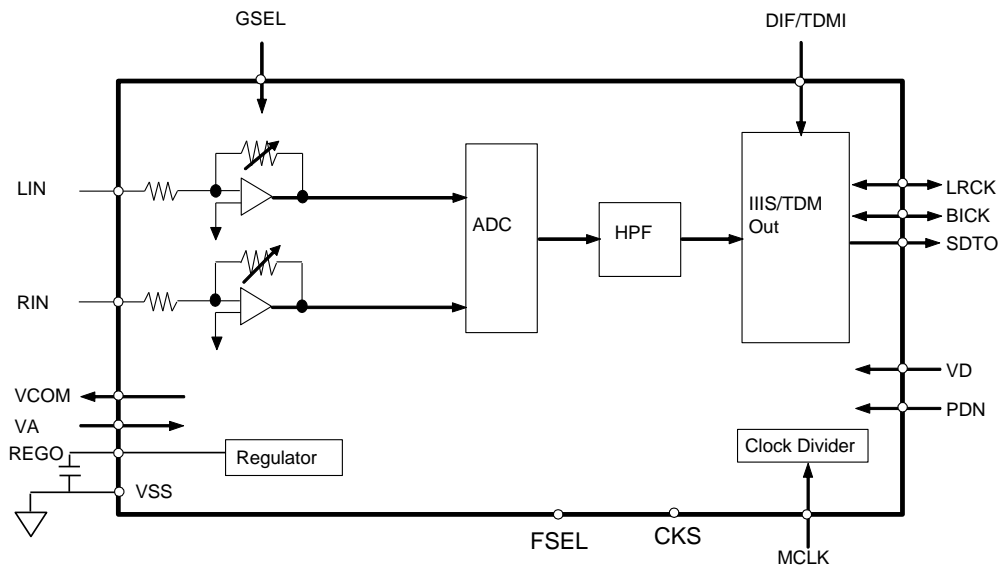
96kHz 24-Bit $\Delta\Sigma$ ADC

1. General Description

The AK5720 is a low voltage 24-bit A/D converter for digital audio systems. The AK5720 includes an Input Gain Amplifier, making it suitable for microphone applications. The analog signal input of the AK5720 is single-ended, eliminating the need for external filters. The AK5720 is housed in a space-saving 16-pin TSSOP package.

2. Features

1. Resolution: 24bits
2. Recording Functions
 - Gain Amplifier (0dB / +15dB)
 - Digital HPF for DC-offset cancellation ($f_c=1.0\text{Hz}@f_s=48\text{kHz}$)
3. ADC Characteristics
 - Single-ended Input
 - Input Level: $1.8\text{Vpp}@V_A=3.0\text{V}$ ($= 0.6 \times V_A$), $3.0\text{Vpp}@V_A=5.0\text{V}$ ($=0.6 \times V_A$)
 - S/(N+D): 94dB
 - DR, S/N: 102dB
4. Master Clock: 256fs/384fs/512fs/768fs
5. Sampling Frequency: 8kHz~ 96kHz
6. Audio Data Format: MSB First, 2's compliment
 - 24-bit MSB justified, I²S and TDM
7. Power Supply
 - V_A, V_D : 2.7 ~ 5.5V (typ. 3V, 5V)
8. Power Supply Current: 6.1mA($V_A-V_D=5.0\text{V}, f_s=48\text{kHz}$)
9. Operating Temperature: $T_a = -40 \sim 105^\circ\text{C}$
10. Package: 16-pin TSSOP



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■ Functions

No.	Pin Name	I/O	Function	Power Down Status
1	VCOM	O	ADC Common Voltage Output Pin	Pull-down to VSS with NMOS (0.5kΩ)
2	RIN	I	Rch Input Pin	Hi-z
3	LIN	I	Lch Input Pin	Hi-z
4	VSS	-	Ground Pin	-
5	VA	-	Analog Power Supply Pin	-
6	VD	-	Digital Power Supply Pin	-
7	GSEL	I	Input Gain Select Pin “L”: 0dB, “H”: +15dB	Hi-z
8	REGO	O	Regulator Output Pin	Pull-down to VSS with 500Ω
9	SDTO	O	Audio Serial Data Output Pin	“L” (VSS)
10	LRCK	I/O	Input/Output Channel Clock Pin	Hi-z
11	MCLK	I	Master Clock Input Pin	Hi-z
12	BICK	I/O	Audio Serial Data Clock Pin	Hi-z
13	PDN	I	Reset & Power Down Pin “L”: Reset & Power down, “H”: Normal operation	Hi-z
14	DIF/TDMI	I	Audio Data Format Select Pin “L”: MSB justified, “H”: I ² S	Hi-z
			TDM Data Input Pin	Hi-z
15	FSEL	I	Digital Filter select Pin “L”: Sharp Roll-Off, “H”: Short Delay Sharp Roll-Off	Hi-z
16	CKS	I	Mode Select Pin Parasitic capacitance of the pin should be less than 20pF.	Hi-z

Note: All digital input pins must not be allowed to float.

Note: The GSEL pin must be fixed to “H” or “L” when the PDN pin = “H” to avoid starting the test mode.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	RIN, LIN	This pin should be open.

5. Absolute Maximum Ratings

(VSS=0V; [Note 1](#))

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pins)		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes. The AK5720 will be damaged if a voltage higher than 2.5V is input to the REGO pin.

6. Recommended Operating Conditions

(VSS=0V; [Note 1](#))

Parameter		Symbol	min	typ	max	Unit
Power Supplies	Analog (VA pin)	VA	2.7	3 or 5	5.5	V
	Digital (VD pin)	VD	2.7	3 or 5	VA	V

Note 1. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

7. Analog Characteristics (VA=VD=5.0V)

(Ta=25°C; VA=VD=5.0V; fs=48kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
ADC Analog Input Characteristics:					
Resolution				24	Bits
Input Voltage (Note 2)	Gain = 0dB	2.7	3.0	3.3	Vpp
	Gain = +15dB	0.48	0.53	0.58	
S/(N+D) (-1.0dBFS)	VA=5V	84	94		dB
	Gain = 0dB	-	92		dB
	VA=5V	74	84		dB
	Gain = +15dB	-	80		dB
DR (-60dBFS)	VA=5V	94	102		dB
	Gain = 0dB	-	99		dB
	VA=5V	83	91		dB
	Gain = +15dB	-	86		dB
S/N	VA=5V	94	102		dB
	Gain = 0dB	-	99		dB
	VA=5V	83	91		dB
	Gain = +15dB	-	86		dB
Input Resistance	Gain = 0dB	29	41		kΩ
		-	28		kΩ
	Gain = +15dB	15	22		kΩ
		-	13		kΩ
Interchannel Isolation (RIN, LIN)	Gain = 0dB	90	110		dB
	Gain = +15dB		90		dB
Interchannel Gain Mismatch (RIN, LIN)			0	0.5	dB
Gain Drift			100	-	ppm/°C
Power Supply Rejection		-	50		dB
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
VA			3.8	5.7	mA
VD	(fs=48kHz)		2.3	3.5	mA
VD	(fs=96kHz)		4.4	6.7	mA
Power down mode (PDN pin = "L") (Note 4)					
VA+VD			10	100	μA

Note 2. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage.
 $V_{in} = 0.6 \times V_A$ (Vpp).

Note 3. PSR is applied to VA and VD with 1kHz, 50mVpp.

Note 4. All digital input pins and CKS1 pin are held VD or VSS.

8. Analog Characteristics (VA=VD=3.0V)

(Ta=25°C; VA=VD=5.0V; fs=48kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
ADC Analog Input Characteristics:					
Resolution				24	Bits
Input Voltage (Note 2)	Gain = 0dB	1.65	1.8	1.95	Vpp
	Gain = +15dB	0.29	0.32	0.35	
S/(N+D) (-1.0dBFS)	VA=3V Gain = 0dB	fs=48kHz, 84	94		dB
		fs=96kHz -	92		dB
	VA=3V Gain = +15dB	fs=48kHz 71	81		dB
		fs=96kHz -	77		dB
DR (-60dBFS)	VA=3V Gain = 0dB	fs=48kHz, A-weighted 90	98		dB
		fs=96kHz -	95		dB
	VA=3V Gain = +15dB	fs=48kHz, A-weighted -	86		dB
		fs=96kHz -	81		dB
S/N	VA=3V Gain = 0dB	fs=48kHz, A-weighted 90	98		dB
		fs=96kHz -	95		dB
	VA=3V Gain = +15dB	fs=48kHz, A-weighted -	86		dB
		fs=96kHz -	81		dB
Input Resistance	Gain = 0dB	fs=48kHz 29	41		kΩ
		fs=96kHz -	28		kΩ
	Gain = +15dB	fs=48kHz 15	22		kΩ
		fs=96kHz -	13		kΩ
Interchannel Isolation		Gain = 0dB	90	110	dB
		Gain = +15dB		90	dB
Interchannel Gain Mismatch			0	0.5	dB
Gain Drift			100	-	ppm/°C
Power Supply Rejection (Note 3)		-	50		dB
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
VA			3.4	5.1	mA
VD	(fs=48kHz)		1.9	2.9	mA
VD	(fs=96kHz)		3.7	5.6	mA
Power down mode (PDN pin = "L") (Note 4)					
VA+VD			10	100	μA

Note 2. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage.
 $V_{in} = 0.6 \times V_A$ (Vpp).

Note 3. PSR is applied to VA and VD with 1kHz, 50mVpp.

Note 4. All digital input pins and CKS1 pin are held VD or VSS.

9. Filter Characteristics (fs=48kHz)

(Ta=25°C; VA=VD=2.7 ~ 5.5V, fs=48kHz)

Parameter	Symbol	min	typ	max	Unit	
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF(FSEL pin="L")						
Passband (Note 5)	±0.16dB	PB	0	-	18.8	kHz
	-0.28dB		-	20.0	-	kHz
	-3.0dB		-	22.8	-	kHz
Stopband (Note 5)	SB	28.4	-	-	kHz	
Stopband Attenuation	SA	71	-	-	dB	
Group Delay Distortion 0 ~ 20.0kHz	ΔGD	-	0	-	1/fs	
Group Delay (Note 6)	GD	-	15.5	-	1/fs	
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER(FSEL pin="H")						
Passband (Note 5)	±0.16dB	PB	0	-	18.8	kHz
	-0.28dB		-	20.0	-	kHz
	-3.0dB		-	22.8	-	kHz
Stopband (Note 5)	SB	28.4		-	kHz	
Stopband Attenuation	SA	72		-	dB	
Group Delay Distortion 0 ~ 20.0kHz	ΔGD	-	-	2.4	1/fs	
Group Delay (Note 6)	GD	-	5.5	-	1/fs	
ADC Digital Filter (HPF):						
Frequency Response	-3.0dB	FR	-	1.0	-	Hz
	-0.5dB		-	2.5	-	Hz
	(Note 5) -0.1dB		-	6.5	-	Hz

Note 5. The passband and stopband frequencies scale with fs.

For example, PB=0.45 × fs(@-0.1dB).

Note 6. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the output register.

10. Filter Characteristics (fs=96kHz)

(Ta=25°C; VA=VD=2.7 ~ 5.5V; fs=96kHz)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF(FSEL pin="L")						
Passband (Note 5)	±0.16dB	PB	0	-	37.6	kHz
	-0.28dB		-	40.0	-	kHz
	-3.0dB		-	45.6	-	kHz
Stopband (Note 5)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	71	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 6)		GD	-	15.5	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER(FSEL pin="H")						
Passband (Note 5)	±0.16dB	PB	0	-	37.6	kHz
	-0.28dB		-	40.0	-	kHz
	-3.0dB		-	45.6	-	kHz
Stopband (Note 5)		SB	56.8	-	-	kHz
Stopband Attenuation		SA	72	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.4	1/fs
Group Delay (Note 6)		GD	-	5.5	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 5)	-3.0dB	FR	-	2.0	-	Hz
	-0.5dB		-	5.0	-	Hz
	-0.1dB		-	-	13.0	-

Note 5. The passband and stopband frequencies scale with fs.

For example, PB=0.45 × fs(@-0.1dB).

Note 6. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the output register.

11. DC Characteristics

(Ta=25°C, VA=VD=2.7 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
High-Level Input Voltage		VIH	75% VD	-	-	V
Low-Level Input Voltage		VIL	-	-	25% VD	V
High-Level Output Voltage (Iout=-80μA)		VOH	VD-0.4	-	-	V
Low-Level Output Voltage (Iout=80μA)		VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

12. Switching Characteristics

(Ta=-40°C ~ 105°C; VA=VD=2.7 ~ 5.5V; CL=20pF, unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit	
Master Clock Timing						
Master Clock	256fs:	fCLK	2.048	12.288	24.576	MHz
	Pulse Width Low	tCLKL	16			ns
	Pulse Width High	tCLKH	16			ns
384fs:	fCLK	3.072	18.432	36.864	MHz	
	Pulse Width Low	tCLKL	11			ns
	Pulse Width High	tCLKH	11			ns
512fs:	fCLK	4.096	24.576	24.576	MHz	
	Pulse Width Low	tCLKL	16			ns
	Pulse Width High	tCLKH	16			ns
768fs:	fCLK	6.144	36.864	36.864	MHz	
	Pulse Width Low	tCLKL	11			ns
	Pulse Width High	tCLKH	11			ns
LRCK Timing (Slave Mode)						
Normal mode						
LRCK Frequency	fs	8		96	kHz	
Duty Cycle	Duty	45		55	%	
TDM256 MODE						
LRCK Frequency	fs	8		96	kHz	
“H” time	tLRH	1/256fs			ns	
“L” time	tLRL	1/256fs			ns	
LRCK Timing (Master Mode)						
Normal mode						
LRCK Frequency	fs	8		96	kHz	
Duty Cycle	Duty		50		%	
TDM256 MODE						
LRCK Frequency	fs	8		96	kHz	
“H” time	tLRH		1/8fs		ns	

Note 7. It will be “L” time in I²S format.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Normal mode					
BICK Period	tBCK	160			ns
BICK Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
LRCK Edge to BICK “↑” (Note 8)	tLRB	30			ns
BICK “↑” to LRCK Edge (Note 8)	tBLR	30			ns
LRCK to SDTO (MSB) (Except I ² S mode)	tLRS			35	ns
BICK “↓” to SDTO	tBSD			35	ns
TDM256 mode					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK “↑” (Note 8)	tLRB	10			ns
BICK “↑” to LRCK Edge (Note 8)	tBLR	10			ns
SDTO Setup time BICK “↑”	tBSS	7			ns
SDTO Hold BICK “↑”	tBSH	6			ns
TDMI Hold Time	tSDH	4			ns
TDMI Setup Time	tSDS	5			ns
Audio Interface Timing (Master mode)					
Normal mode					
BICK Frequency	fBCK		64fs		Hz
BICK Duty	dBCK		50		%
BICK “↓” to LRCK	tMBLR	-20		20	ns
BICK “↓” to SDTO	tBSD	-40		40	ns
TDM256 mode					
BICK Frequency	fBCK		256fs		Hz
BICK Duty (Note 9)	dBCK		50		%
BICK “↓” to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK “↑”	tBSS	7			ns
SDTO Hold BICK “↑”	tBSH	6			ns
TDMI Hold Time	tSDH	4			ns
TDMI Setup Time	tSDS	5			ns
Power-Down & Reset Timing					
PDN Pulse Width (Note 10)	tPD	150		30	ns
PDN Reject Pulse Width (Note 10)	tRPD		4129		ns
PDN “↑” to SDTO valid (Note 11)	tPDV				1/fs

Note 8. BICK rising edge must not occur at the same time as LRCK edge.

Note 9. In the case of MCLK duty cycle is 50%.

Note 10. The AK5720 can be reset by setting the PDN pin to “L” upon power-up. The PDN pin must held “L” for more than 150ns for a certain reset. The AK5720 is not reset by the “L” pulse less than 30ns.

Note 11. This is the count of LRCK “↑” from the PDN pin = “H”.

■ Timing Diagram

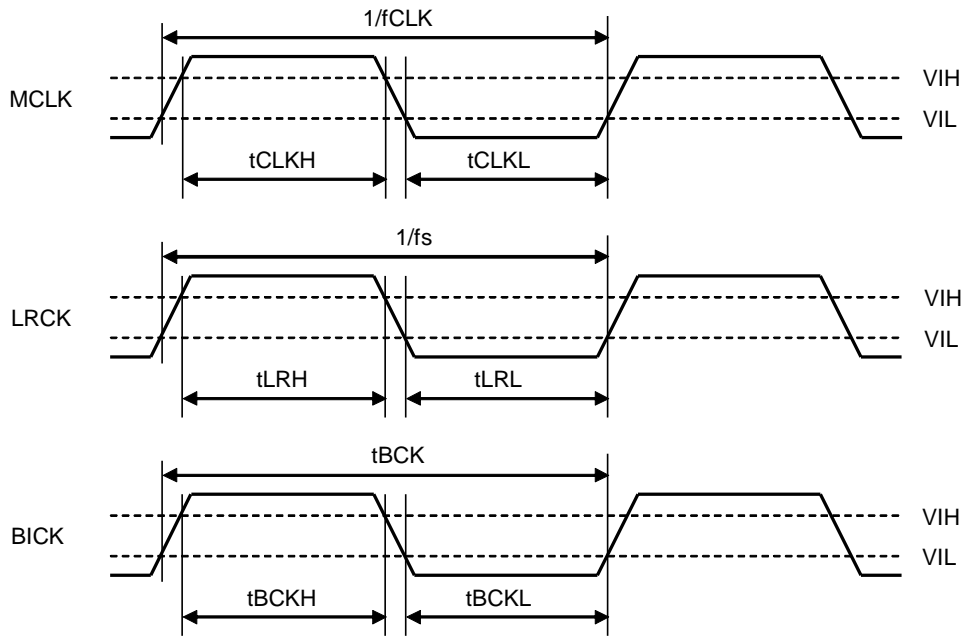


Figure 1. Clock Timing (Slave mode)

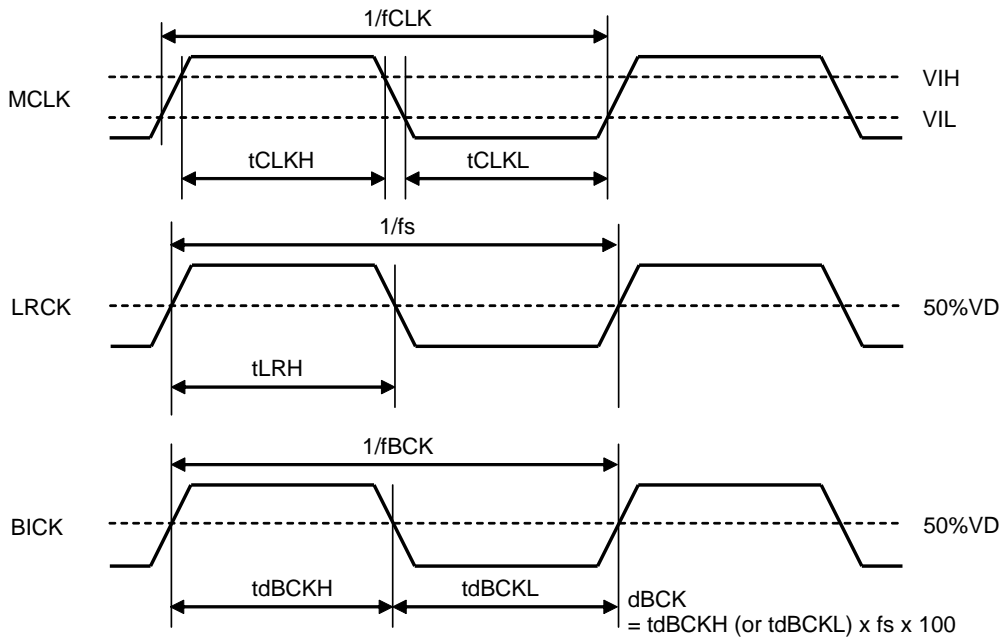


Figure 2. Clock Timing (Master mode)

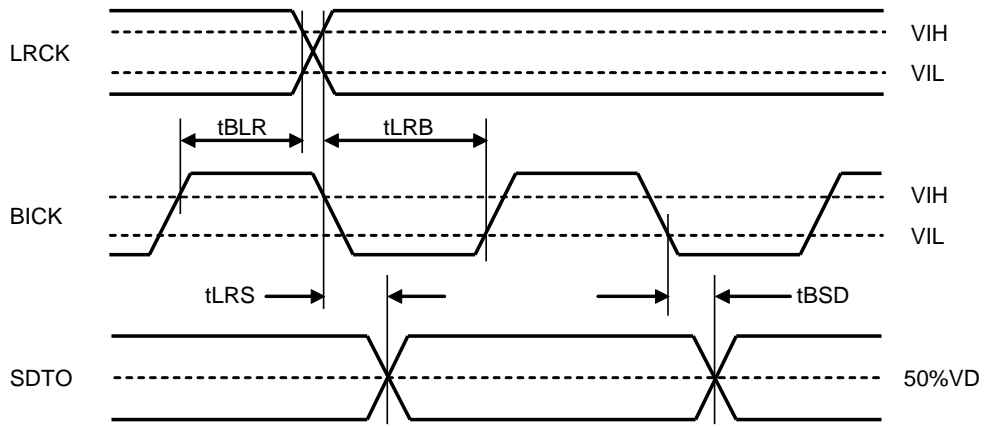


Figure 3. Audio Interface Timing (Normal mode & Slave mode)

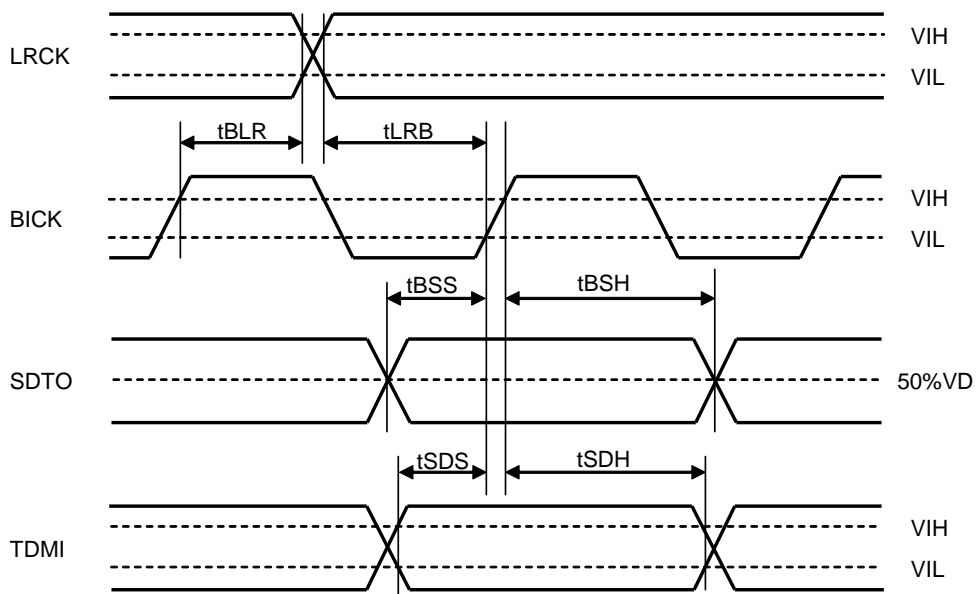


Figure 4. Audio Interface Timing (TDM mode & Slave mode)

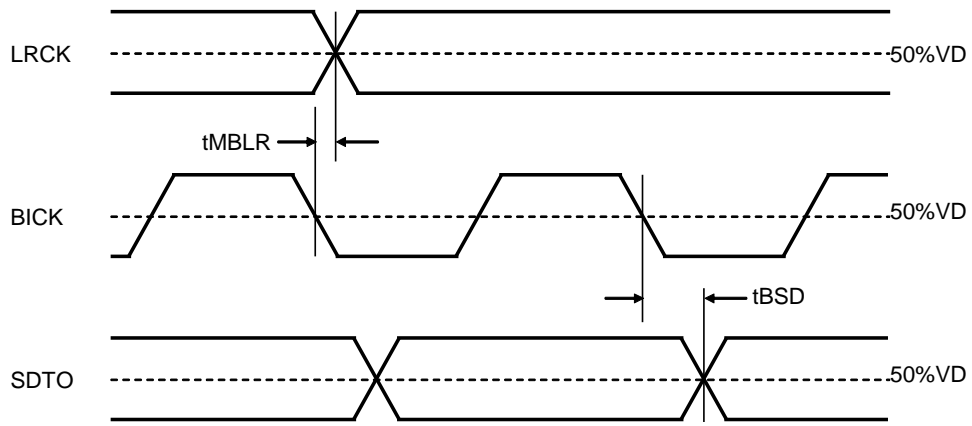


Figure 5. Audio Interface Timing (Normal mode & Master mode)

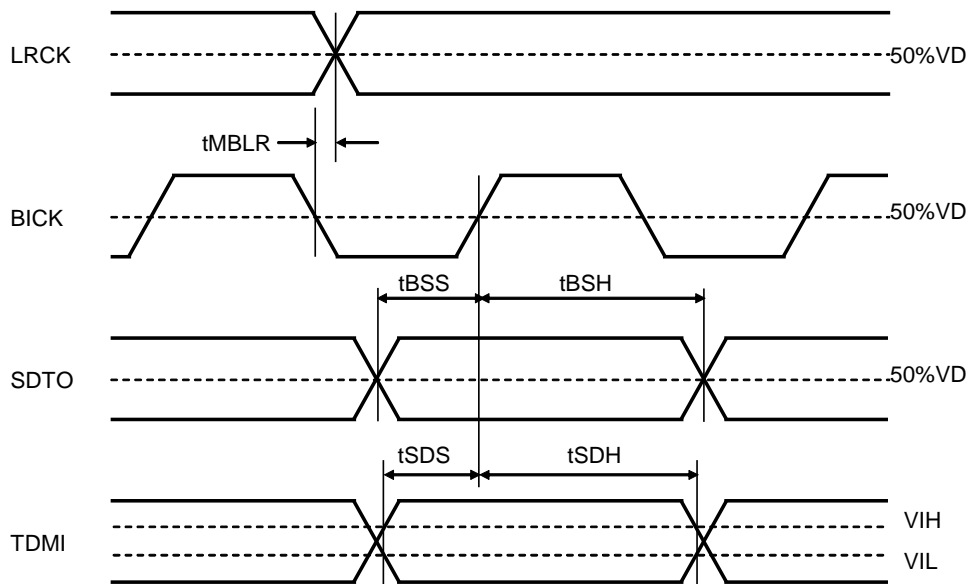


Figure 6. Audio Interface Timing (TDM mode & Master mode)

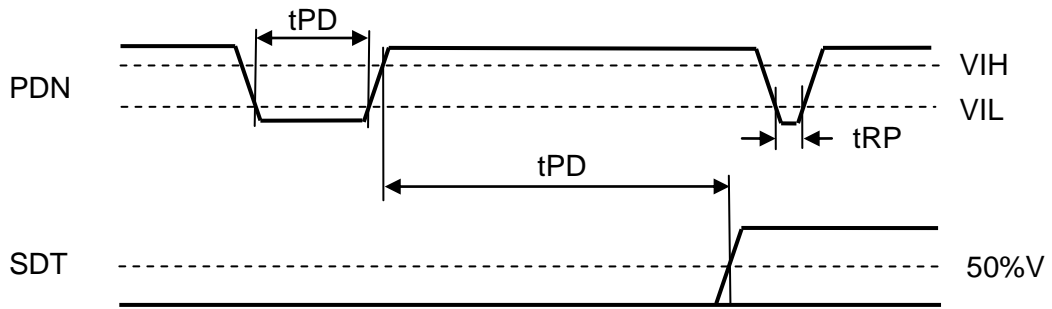


Figure 7. Power-down & Reset Timing

13. Functional Descriptions

■ System Clock

MCLK, BICK and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. All external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = "L". If the external clocks are not present, place the AK5720 in power-down mode (PDN pin = "L"). In master mode, the master clock (MCLK) must be provided unless PDN pin = "L".

fs	MCLK					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	8.192MHz	12.288MHz	16.384MHz	24.576MHz
44.1kHz	N/A	N/A	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz
48kHz	N/A	N/A	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	36.864MHz	N/A	N/A

Table 1. System Clock Example

■ Audio Interface Format

MCLK frequency, the relationship of BICK frequency and fs, and master/slave mode are set by external resistance value of the CKS pin and the CKS pin connection as shown in Table 2.

When the CKS pin is connected to GND or VA directly, or via an external 4.7kΩ resistor (Normal mode), the DIF/TDMI pin becomes an audio data format select pin. Two kinds of data formats: 24bit MSB justified and I²S formats can be chosen by the DIF pin. The audio data is output on the falling edge of BICK from the SDTO pin. The audio interface supports both master and slave modes. In master mode, BICK and LRCK are output and they are input in slave mode. In master mode, LRCK frequency is fixed to 1fs and the BICK frequency is fixed to 64fs.

When the CKS pin is connected to GND or the VA pin via an external resistor of 18kΩ or 82kΩ (TDM mode), the DIF/TDMI pin becomes a TDM data input pin. In TDM mode, the audio data is output on a rising edge of BICK from the SDTO pin. When inputting the SDTO output data to the TDMI pin, this SDTO data has a delay which fills set-up or hold time of BICK rising .

Mode	CKS	DIF /TDMI	SDTO	Master /Slave	MCLK	LRCK	BICK
0	< 10Ω to GND (Short to GND)	L	MSB	Slave	256/384fs (8k≤fs≤96k) 512/768fs (8k≤fs≤48k)	H/L	≥ 48fs or 32fs
1		H	I ² S			L/H	
2	< 10Ω to VA (Short to VA)	L	MSB	Master	256fs (8k≤fs≤96k)	H/L	64fs
3		H	I ² S			L/H	
4	4.7kΩ±10% to GND	L	MSB	Master	384fs (8k≤fs≤96k)	H/L	64fs
5		H	I ² S			L/H	
6	4.7kΩ±10% to VA	L	MSB	Master	512fs (8k≤fs≤48k)	H/L	64fs
7		H	I ² S			L/H	
8	18kΩ±10% to GND	TDMI	MSB	Master	256fs (8k≤fs≤96k)	↑	256fs
9	18kΩ±10% to VA	TDMI	MSB	Slave	256fs (8k≤fs≤96k)	↑	256fs
10	82kΩ±10% to GND	TDMI	I ² S	Master	256fs (8k≤fs≤96k)	↓	256fs
11	82kΩ±10% to VA	TDMI	I ² S	Slave	256fs (8k≤fs≤96k)	↓	256fs

Table 2. Operation Mode Select

Note 12. SDTO outputs 16-bit data when BICK=32fs.

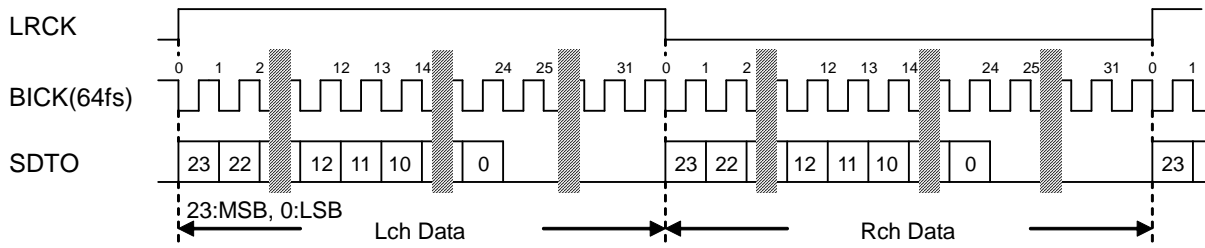


Figure 8. Mode 0, 2, 4, 6 Timing (Normal mode, MSB justified)

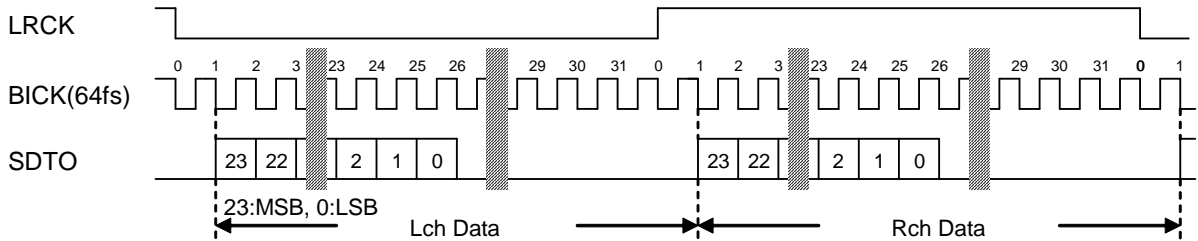


Figure 9. Mode 1, 3, 5, 7 Timing (Normal mode, I²S Compatible)

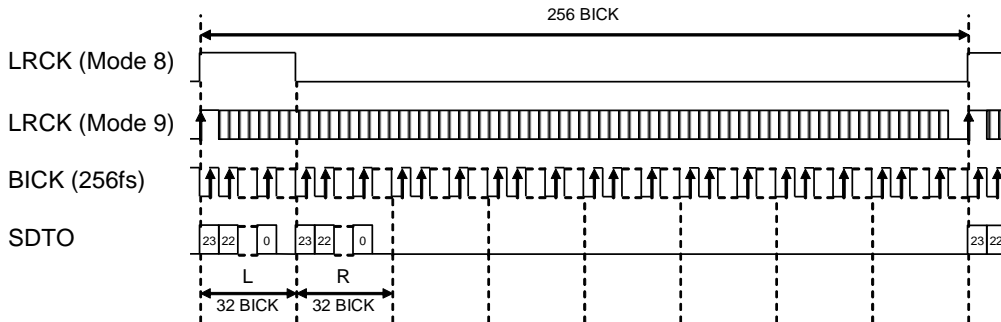


Figure 10. Mode 8, 9 Timing (TDM256 mode, MSB justified)

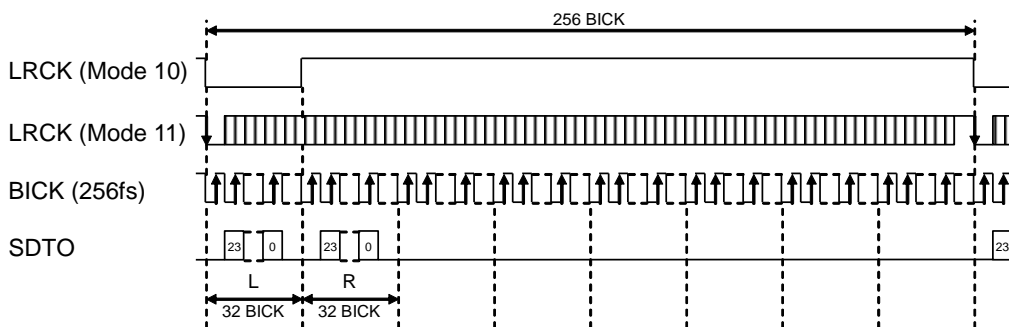


Figure 11. Mode 10, 11 Timing (TDM256 mode, I²S Compatible)

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@ $f_s=48\text{kHz}$) and scales with sampling rate (f_s).

■ Power Down

The AK5720 is placed in the power-down mode by bringing the PDN pin to “L”. The digital filter is also reset at the same time. This reset should always be executed upon power-up. In power-down mode, VCOM becomes VSS level. The AK5720 will be in analog initialization cycle after exiting the power-down mode. Therefore, the SDTO output data becomes valid after 4129 cycles of LRCK clock in master mode or 4132 cycles of LRCK clock in slave mode when power up the AK5720. During initialization, both L and R channels of ADC digital data outputs are forced to “0” in 2’s complement. The ADC outputs settle as a data corresponding to the input signals after the end of initialization (this settling takes approximately group delay time).

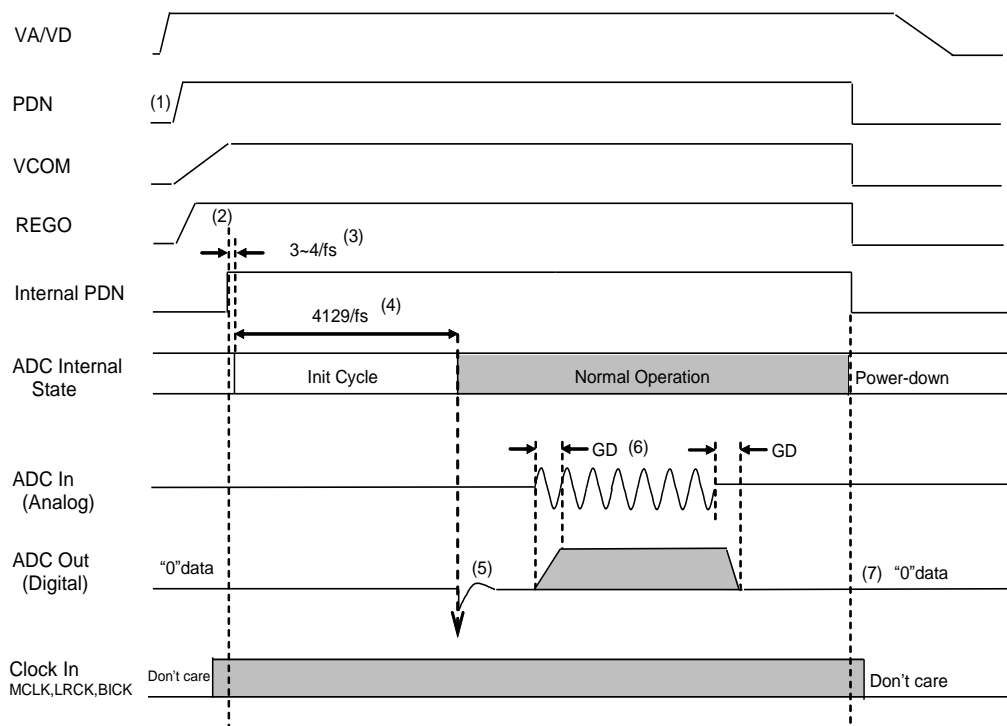


Figure 12. Power-down/up Timing Example

Notes:

- (1) The PDN pin must be “L” when power up the AK5720 and set to “H” after all poweres are supplied.
- (2) The internal power-down state is released after 147456/ MCLK cycles.
- (3) There is a delay about 3~4 f_s from internal power-up to the start of initialization cycle.
- (4) Digital block of the ADC is initialized after internal power-down is released.
When start-up the AK5720, ADC input voltage should be operation common voltage.
A charge-up time of DC cut capacitor is necessary to wait until the RIN and LIN pins settle to the common voltage. When the external capacitor is 10 μF , the status of these pin settles in $\tau=400\text{ms}$ (typ).
- (5) Click noise occurs at the end of initialization in the digital part. Mute the ADC output externally if the click noise influences system applications.
- (6) Digital output corresponds to analog input has group delay (GD).
- (7) ADC outputs “0” data in power-down state.

■ System Reset

The AK5720 should be reset once by bringing the PDN pin to “L” after power-up. In slave mode, reset and power-down are released on the rising edge (falling edge in I²C compatible mode) of LRCK after setting the PDN pin = “H”. In master mode, reset and power-down are released by MCLK input after setting the PDN pin = “H”.

■ TDM Cascade Mode

TDM256mode

Four or less devices can be connected in cascades at the TDM256 mode. In Figure 13, the SDTO pin of device #1/#2/#3 is connected with the TDMI pin of device #2/#3/#4. It is possible to output 8 channel TDM data from the SDTO pin of device #4 as shown in Figure 14.

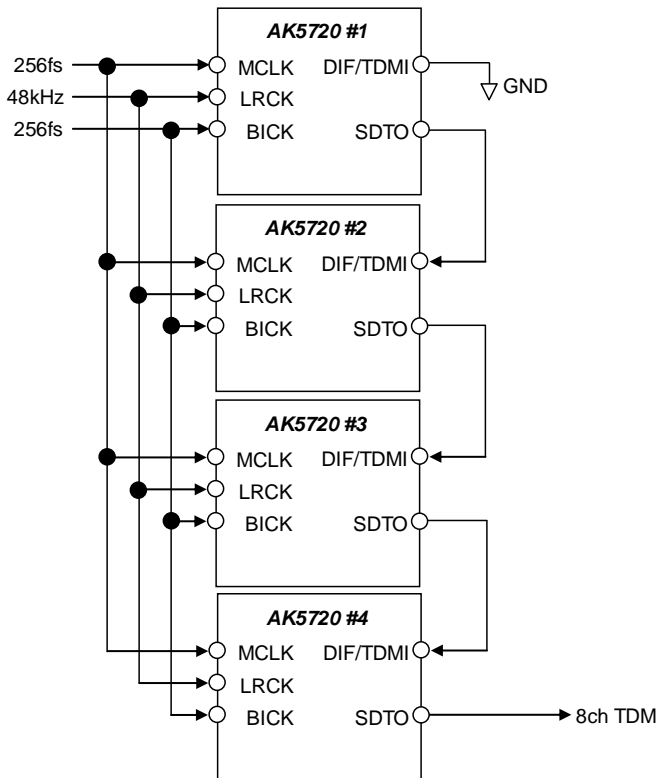


Figure 13. Cascade TDM Connection Diagram

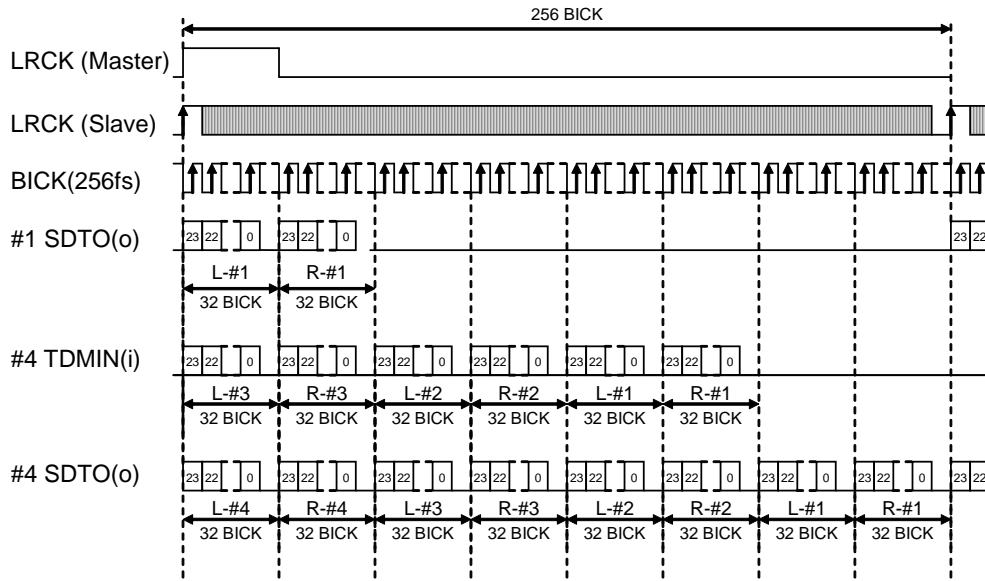
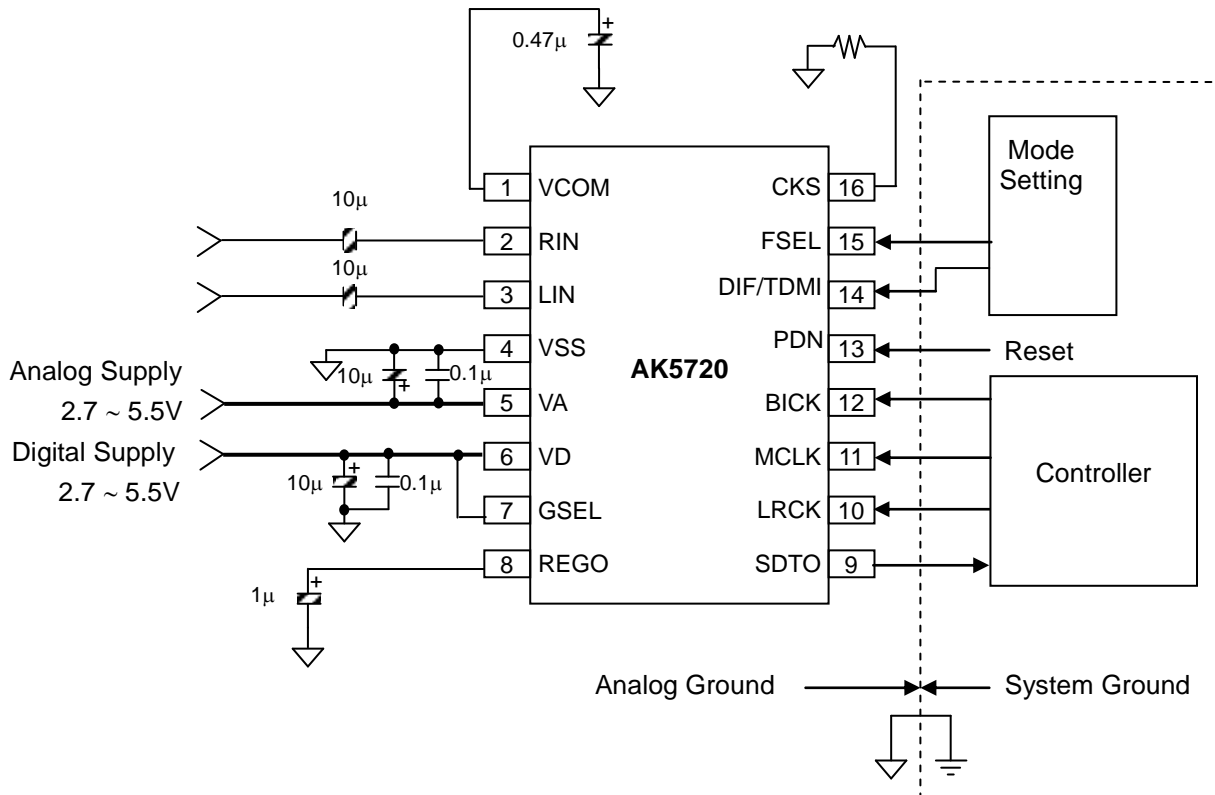


Figure 14. Cascade TDM Timing (TDM256 Mode (Left Justified))

14. Recommended External Circuits

Figure 15 shows the system connection diagram. An evaluation board (AKD5720) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:
 - All digital input pins should not be left floating.

Figure 15. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK5720 requires careful attention to power supply and grounding arrangements. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. VSS of the AK5720 must be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5720 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The voltage input to VA sets the analog input range. VCOM is 50% VA and used as the common voltage of analog signals. The VCOM pin is connected to VSS. A 0.47 μ F ceramic capacitor should be connected as close to the VCOM pin as possible between VSS and the VCOM pin. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5720.

3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (50% VA) with 41k Ω (typ@fs=48kHz) resistance. The input signal range scales with the supply voltage and nominally 0.6 \times VA Vpp (typ). The ADC output data format is 2's complement. The internal HPF removes the DC offset (includes the DC offset that is caused by the ADC).

The AK5720 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK5720 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

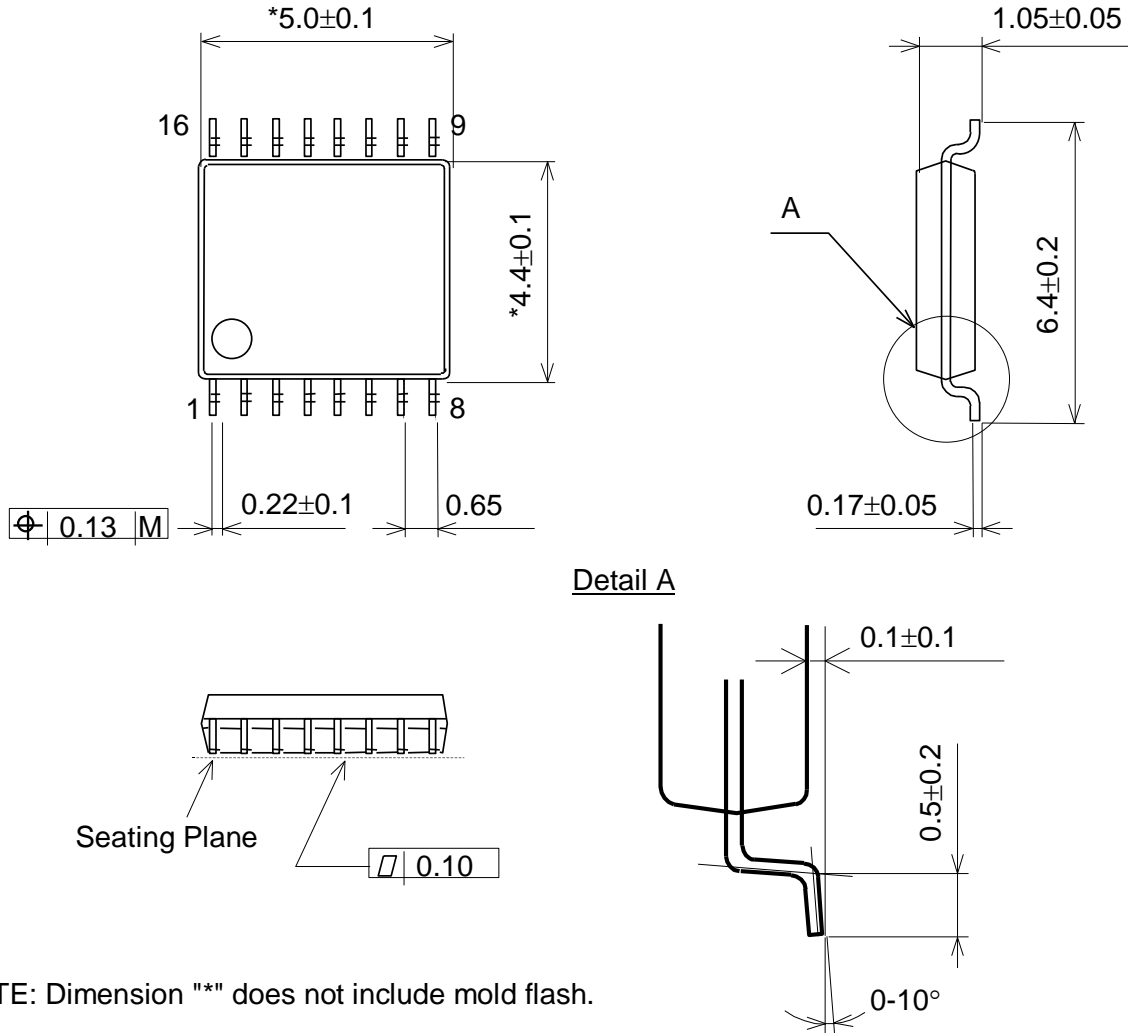
4. External Resistor of the CKS pin

The external resistor of the CKS pin should be close as possible to the pin and kept away from the signal lines to prevent noises into the CKS pin.

15. Package

■ Outline Dimensions

16pin TSSOP (Unit: mm)

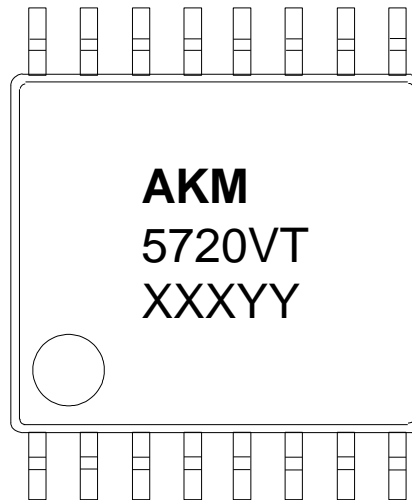


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead Finish

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate

■ Marking



- 1) Pin #1 indication
- 2) Date Code: XXXYY (5 digits)
 XXX: Week Code
 YY: Factory Control Code
- 3) Marketing Code : 5720VT
- 4) Asahi Kasei Logo

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
14/04/17	00	First Edition		
14/10/17	01	Error Correction	22	3. Analog Inputs The AK5720 samples the analog inputs at 64fs(@fs=48kHz). → The AK5720 samples the analog inputs at 64fs.
14/12/18	02	Error Correction	16	Table 2 Mode 8-11 The tolerances of resistors were corrected. ±5% →±10%
		Description Change	16	Table 2 and Table 3 were combined.

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