NCP81250

Voltage Regulator, Single-Phase, SVID Interface for Computing Apps

High Switching Frequency, High Efficiency, Integrated Power MOSFETs

The NCP81250, a single−phase synchronous buck regulator, integrates power MOSFETs to provide a high−efficiency and compact−footprint power management solution for new generation computing CPUs. The device is able to deliver up to 14 A TDC output current on an adjustable output with SVID interface. Operating in high switching frequency up to 1.2 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. Current−mode RPM control with feedforward from both input power supply and output voltage ensures stable operation over wide operation condition. The NCP81250 is in a QFN48 6 x 6 mm package.

Features

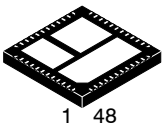
- Meets Intel® Server Specifications
- 5 V to 20 V Input Voltage Range
- 0.9 V/1.35 V Fixed Boot Voltage
- Adjustable Output Voltage with SVID Interface
- Integrated Gate Driver and Power MOSFETs
- Up to 14 A TDC Output Current
- 500 kHz ~ 1.2 MHz Switching Frequency
- Current−Mode RPM Control
- Programmable SVID Address and ICCMax
- Programmable DVID Feed−Forward to Support Fast DVID
- Feedforward Operation for Input Supply Voltage and Output Voltage
- Output Over−Voltage and Under−Voltage Protections
- External Current Limitation Programming with Inductor Current Sense
- QFN48, 6 x 6 mm, 0.4 mm Pitch Package
- This is a Pb−Free Device

Typical Applications

- Server Applications

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QFN48
CASE 485CJ

MARKING DIAGRAM



NCP81250	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81250MNTXG	QFN48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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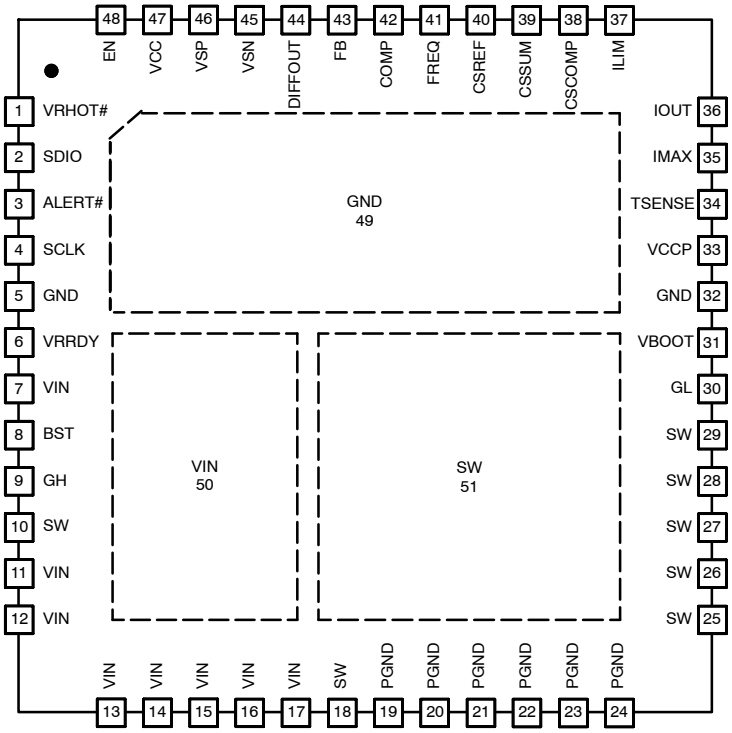


Figure 1. Pin Configuration
(Top View)

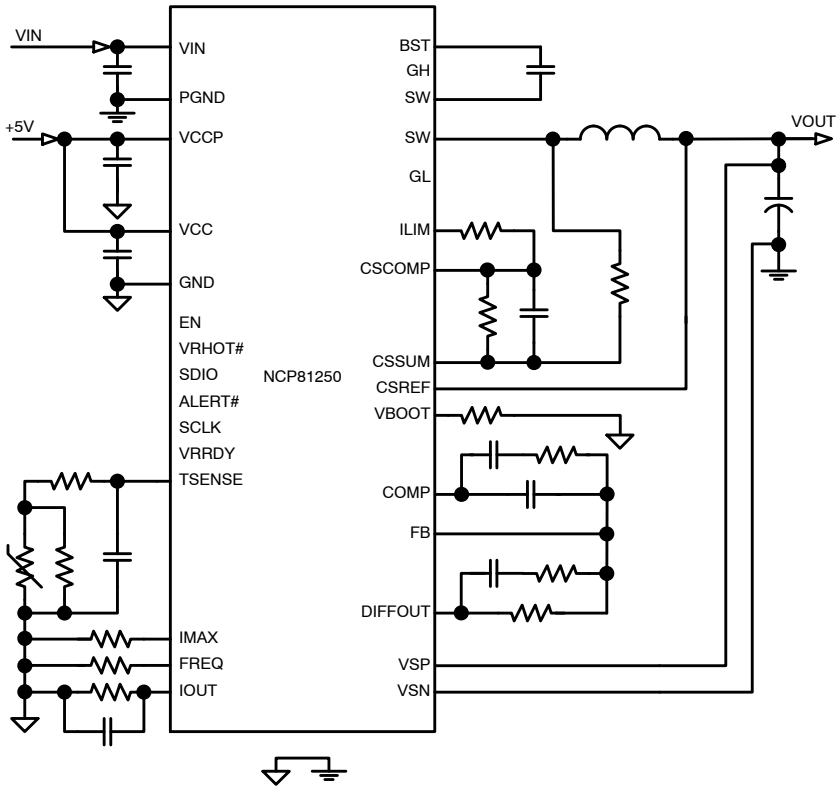


Figure 2. Typical Application Circuit

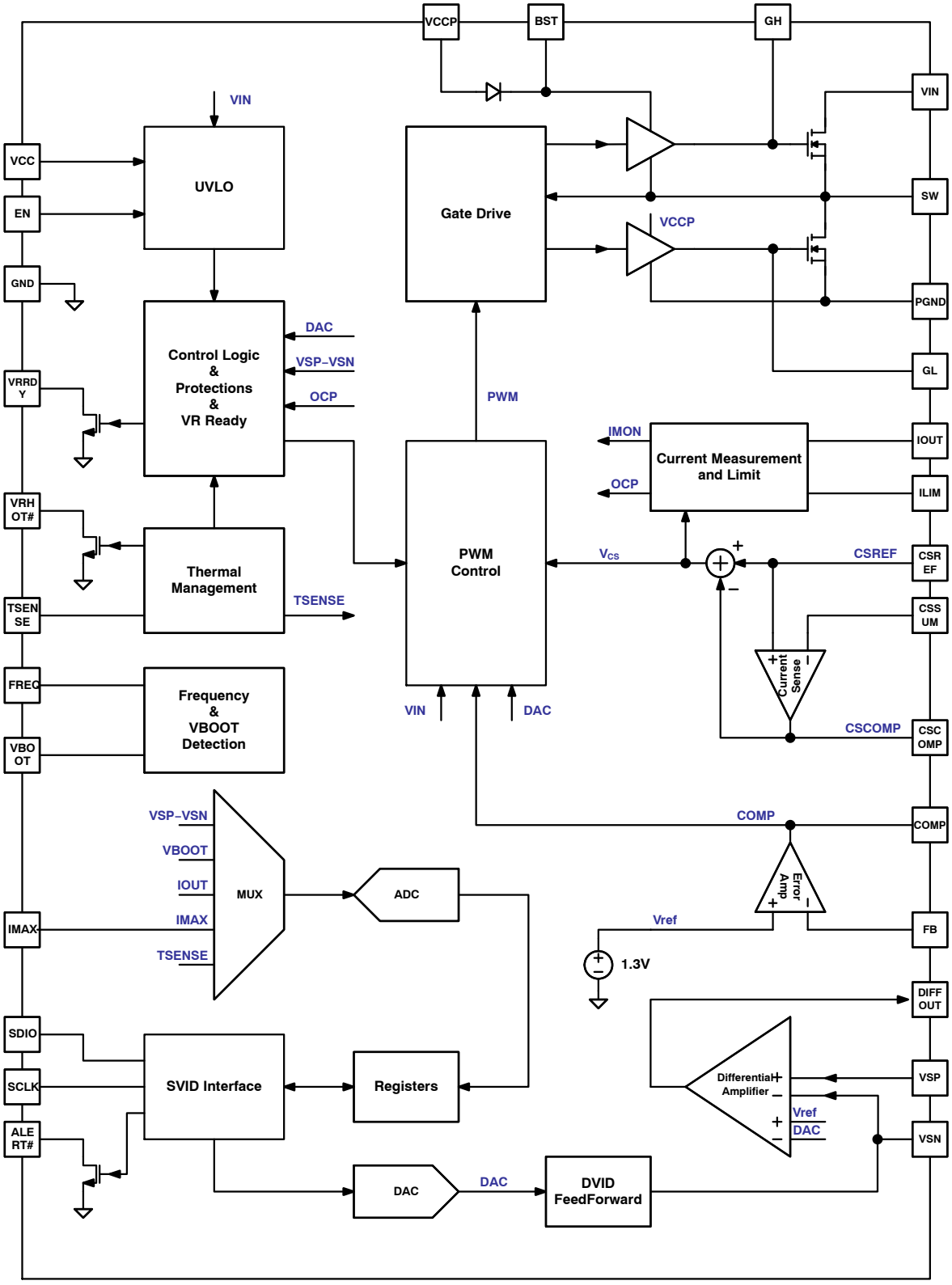


Figure 3. Functional Block Diagram

Table 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	VRHOT#	Logic Output	**VR HOT.** Logic low output represents over temperature.
2	SDIO	Logic Bidirectional	**Serial Data IO Port.** Data port of SVID interface.
3	ALERT#	Logic Output	**ALERT.** Open−drain output. Provides a logic low valid alert signal of SVID interface.
4	SCLK	Logic Input	**Serial Clock.** Clock input of SVID interface.
5, 32, 49	GND	Analog Ground	**Analog Ground.** Ground of internal control circuits. Must be connected to the system ground.
6	VRRDY	Logic Output	**Voltage Regulator Ready.** Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
7, 11−17, 50	VIN	Power Input	**Power Supply Input.** These pins are the power supply input pins of the device, which are connected to drain of internal high−side power MOSFET. 22 μF or more ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to these pins.
8	BST	Power Bidirectional	**Bootstrap.** Provides bootstrap voltage for the high−side gate driver. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to SW (pin 10). A 1 − 2 Ω resistor may be employed in series with the BST cap to reduce switching noise and ringing when needed.
9	GH	Analog Output	**Gate of High−Side MOSFET.** Directly connected with the gate of the high−side power MOSFET.
10	SW	Power Return	**Switching Node.** Provides a return path for integrated high−side gate driver. It is internally connected to source of high−side MOSFET.
18, 25−29, 51	SW	Power Output	**Switch Node.** Pins to be connected to an external inductor. These pins are interconnection between internal high−side MOSFET and low−side MOSFET.
19−24	PGND	Power Ground	**Power Ground.** These pins are the power supply ground pins of the device, which are connected to source of internal low−side power MOSFET. Must be connected to the system ground.
30	GL	Analog Output	**Gate of Low−Side MOSFET.** Directly connected with the gate of the low−side power MOSFET.
31	VBOOT	Analog Input	**Boot−Up Voltage.** A resistor from this pin to ground programs SVID address.
33	VCCP	Analog Power	**Voltage Supply of Gate Driver.** Power supply input pin of internal gate driver. A 4.7 μF or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
34	TSENSE	Analog	**Temperature Sense.** An external temperature sense network is connected to this pin.
35	IMAX	Analog Input	**Current Maximum.** A resistor from this pin to ground programs IMAX.
36	IOUT	Analog Output	**OUT Current Monitor.** Provides output signal representing output current by connecting a resistor from this pin to ground. Shorting this pin to ground disables IMON function.
37	ILIM	Analog Output	**Limit of Current.** A resistor from this pin to CSCOMP programs over−current threshold with inductor current sense.
38	CSCOMP	Analog Output	**Current Sense COMP.** Output pin of current sense amplifier.
39	CSSUM	Analog Input	**Current Sense SUM.** Inverting input of current sense amplifier.
40	CSREF	Analog Input	**Current Sense Reference.** Non−Inverting input of current sense amplifier.
41	FREQ	Analog Input	**Frequency.** A resistor from this pin to ground programs switching frequency.
42	COMP	Analog	**Compensation.** Output pin of error amplifier.
43	FB	Analog Input	**Feedback.** Inverting input to error amplifier.
44	DIFFOUT	Analog Output	**Differential Amplifier Output.** Output pin of differential voltage sense amplifier.
45	VSN	Analog Input	**Voltage Sense Negative Input.** Inverting input of differential voltage sense amplifier. It is also used for DVID feed forward function with an external resistor.
46	VSP	Analog Input	**Voltage Sense Positive Input.** Non−inverting input of differential voltage sense amplifier.
47	VCC	Analog Power	**Voltage Supply of Controller.** Power supply input pin of control circuits. A 1 μF or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
48	EN	Logic Input	**Enable.** Logic high enables the device and logic low makes the device in standby mode.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage to PGND	V_{VIN}		30	V
Switch Node to PGND	V_{SW}		30	V
Analog Supply Voltage to GND	V_{CC}, V_{CCP}	−0.3	6.5	V
BST to PGND	BST_PGND	−0.3	33 38 (<50 ns)	V
BST to SW	BST_SW	−0.3	6.5	V
GH to SW	GH	−0.3 −2 (<200 ns)	BST+0.3	V
GL to GND	GL	−0.3 −2 (<200 ns)	VCCP+0.3	V
VSN to GND	VSN	−0.3	0.3	V
IOUT	IOUT	−0.3	2.5	V
PGND to GND	PGND	−0.3	0.3	V
Other Pins		−0.3	VCC+0.3	V
Latch up Current: (Note 1) All pins, except digital pins Digital pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	125	°C
Storage Temperature Range	T_{STG}	−40	150	°C
Thermal Resistance Junction to Board (Note 2)	$R_{\theta JB}$	8.2		°C/W
Thermal Resistance Junction to Ambient (Note 2)	$R_{\theta JA}$	21.8		°C/W
Power Dissipation at T_A = 25°C (Note 3)	P_D	4.59		W
Moisture Sensitivity Level (Note 4)	MSL	3		–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Latch up Current per JEDEC standard: JESD78 class II.
2. The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4−layer FR−4 PCB board, which has two, 1−ounce copper internal power and ground planes and 2−ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors etc.)
3. The maximum power dissipation (PD) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on T_{JMAX} = 125°C and $R_{\theta JA}$ = 21.8°C/W.
4. Moisture Sensitivity Level (MSL): 3 per IPC/JEDEC standard: J−STD−020D.1.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = V_{CCP} = 5 V, V_{OUT} = 1.0 V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −40°C to 125°C. unless otherwise noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
Supply Voltage V_{IN} Range	(Note 5)	V_{IN}		12		V
Supply Voltage V_{CC} Range	(Note 5)	V_{CC}	4.75	5	5.25	V
Supply Voltage V_{CCP} Range	(Note 5)	V_{CCP}	4.75	5	5.25	V
SUPPLY VOLTAGE MONITOR						
V_{IN} UVLO	Falling Threshold	V_{INUV-}	3.0	3.25	3.5	V
	Hysteresis	V_{INHYS}		650	–	mV
V_{CC} UVLO	Falling Threshold	V_{CCUV-}	3.8	4.08	–	V
	Rising Threshold	V_{CCUV+}	–	4.34	4.5	V
	Hysteresis	V_{CCHYS}	–	260	–	mV
SUPPLY CURRENT						
V_{IN} Quiescent Supply Current (Power MOSFETs)	EN high, no load, PS0,1,2 Modes EN high, no load, PS3 Mode EN high, PS4 Mode (Note 6)	I_Q	– – –	1.5 1.5 –	3 3 1	mA mA μA
V_{IN} Shutdown Current	EN low (Note 6)	I_{SD}	–	–	1	μA
V_{CC} Quiescent Supply Current (Controller)	EN high, no load, PS0,1,2 Modes EN high, no load, PS3 Mode EN high, PS4 Mode (Note 6)	I_{QCC}	– – –	8.0 7.5 170	12 12 194	mA mA μA
V_{CC} Shutdown Current	EN low (Note 6)	I_{SDCC}	–	–	100	μA
V_{CCP} Quiescent Supply Current (Gate Driver)	EN high, no load, PS0,1,2 Modes EN high, no load, PS3 Mode EN high, PS4 Mode	I_{QCCP}	– – –	0.7 0.7 –	1.25 1.25 2	mA mA μA
V_{CCP} Shutdown Current	EN low	I_{SDCCP}	–	–	2	μA
OUTPUT VOLTAGE						
Output Voltage Range	(Note 5)	V_{OUT}	0	–	2.3	V
REGULATION ACCURACY						
System Voltage Accuracy	0.25 V < DAC < 0.8 V 0.8 V < DAC < 1.0 V 1.0 V < DAC < 1.52 V		−8 −10 −0.9		+8 +10 +0.9	mV mV %
DVID						
Fast Slew Rate	Default	FSR		14		mV/μs
Soft Start Slew Rate		SSSR		FSR/4		mV/μs
Slow Slew Rate		SSR		FSR/2 FSR/4 (default) FSR/8 FSR/16		mV/μs
DIFFERENTIAL VOLTAGE−SENSE AMPLIFIER						
DC Gain	VSP−VSN = 0.5 V to 2.3 V	GAIN_DVA		1.0		V/V
−3 dB Gain Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND (Note 5)	BW_DVA		10		MHz
VSP Input Voltage Range	(Note 5)	VSP	−0.3	–	3.0	V
VSN Input Voltage Range	(Note 5)	VSN	−0.3	–	0.3	V
Input Bias Current	VSP,CSREF = 1.3 V	I_{VSP} I_{VSN}	−15 −100		15 100	μA nA

5. Guaranteed by design, not tested in production.
6. T_J = 25°C.

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
DIFFERENTIAL CURRENT−SENSE AMPLIFIER						
DC Gain	(Note 5)	GAIN_DCA		80		dB
−3dB Gain Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND (Note 5)	BW_DCA		10		MHz
Input Offset Voltage		V_{OS_CS}	−300	–	300	μV
Input Bias Current	CSSUM = CSREF = 1.2 V	I_{CSSUM} I_{CSREF}	−7.5 −10		7.5 10	nA μA
ERROR AMPLIFIER						
DC Gain	CL = 20 pF to GND, RL = 10 kΩ to GND (Note 5)	GAIN_EA		80		dB
Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND (Note 5)	BW_EA		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 1.5 V − 2.5 V, CL = 20 pF to GND, RL = 10 kΩ to GND (Note 5)	SR_EA		25		V/μs
Output Voltage Swing	Isource_EA = 2 mA	Vmax_EA	3.5	–	–	V
	Isink_EA = 2 mA	Vmin_EA	–	–	1	
FB Voltage		V_{FB}		1.3		V
Input Bias Current	VFB = 1.3 V	I_{FB}	−1.5		1.5	μA
SWITCHING FREQUENCY						
Normal Operation Frequency (Programmed by a resistor at FREQ pin)	(Note 5)	FSW	500		1200	kHz
FREQ Output Voltage		VFREQ	1.95	2.0	2.05	V
CONTROL LOGIC						
ENABLE Input High Voltage		VEN_H	0.8	–	–	V
ENABLE Input Low Voltage		VEN_L	–	–	0.3	V
ENABLE Input Hysteresis		VEN_HYS	–	300	–	mV
ENABLE Input Bias Current		IEN_BIAS	–		1.0	μA
TSENSE						
Alert# Assert Threshold				491		mV
Alert# De−assert Threshold				513		mV
VR_HOT# Assert Threshold				472		mV
VR_HOT# De−assert Threshold				494		mV
TSENSE Bias Current	V_{TSENSE} = 0.4 V		112	120	128	μA
VBOOT						
Sensing Current	V_{VBOOT} = GND			10		μA
IMAX						
Sensing Current	V_{IMAX} = GND			10		μA

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
ADC						
Voltage Range			0		2.0	V
Total Unadjusted Error (TUE)			−1		1	%
Differential Nonlinearity (DNL)	8−bit				1	LSB
Power Supply Sensitivity				±1		%
Conversion Time				30		μs
Round Robin				90		μs
VR_READY (VRRDY Output)						
Rise Time	External 1 kΩ pull−up to 3.3 V, CTOT = 45 pF, ΔVo = 10% to 90%			120		ns
Fall Time	External 1 kΩ pull−up to 3.3 V, CTOT = 45 pF, ΔVo = 90% to 10%			20		ns
Output Voltage at Power−Up	Pulled up to 5 V via 2 kΩ		–	–	1.0	V
VR_READY Delay (Rising)	DAC = Target to VR_READY			50		μs
VR_READY Delay (Falling)	From OCP or OVP			5		μs
VRRDY Pin Low Voltage	Voltage at VRRDY pin with 4 mA sink current	VPG_L	–	–	0.3	V
VRRDY Pin Leakage Current	VRRDY = 5 V	PG_LK	−1.0	–	1.0	μA
OVER VOLTAGE PROTECTION						
Absolute Over Voltage Threshold During Soft−Start			2.8	2.9	3.0	V
Over Voltage Threshold Above DAC	VSP rising		350	400	425	mV
Over Voltage Delay	VSP rising to GH low			50		ns
UNDER VOLTAGE PROTECTION						
Under Voltage Threshold Below DAC	VSP falling		250	300	350	mV
Under−voltage Delay				5		μs
OVER CURRENT PROTECTION						
ILIM Threshold Current (OCP shutdown after 50 μs delay)		I_{LIMTH_SLOW}	8.5	10.0	12.0	μA
ILIM Threshold Current (immediate OCP shutdown)		I_{LIMTH_FAST}	12.0	15.0	18.0	μA
IOUT OUTPUT						
Current Gain	(IOUTCURRENT) / (ILIMCURRENT); RILIM = 20 kΩ; RIOUT = 5.0 kΩ; DAC = 0.8 V, 1.25 V, 1.52 V		9.5	10	10.5	A/A
Input Referred Offset Voltage	ILIM − CSREF		−5.5	–	5.5	mV
Output Source Current	ILIM sink current = 80 μA			800		μA
HIGH−SIDE MOSFET						
Drain−to−Source ON Resistance	V_{GS} = 4.5 V, I_D = 10 A	R_{ON_H}	–	8.0	–	mΩ
LOW−SIDE MOSFET						
Drain−to−Source ON Resistance	V_{GS} = 4.5 V, I_D = 10 A	R_{ON_L}	–	4.0	–	mΩ

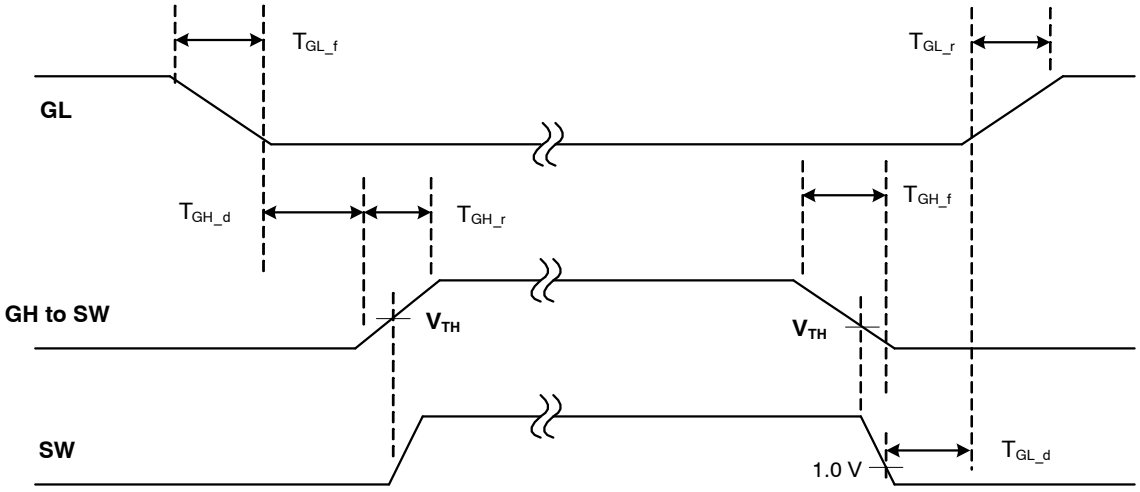
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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
HIGH−SIDE GATE DRIVE						
Pull−High Drive ON Resistance	$V_{BST} - V_{SW}$ = 5 V	R_{DRV_HH}	−	1.2	2.9	Ω
Pull−Low Drive ON Resistance	$V_{BST} - V_{SW}$ = 5 V	R_{DRV_HL}	−	0.8	2.2	Ω
GH Propagation Delay Time	From GL falling to GH rising	T_{GH_d}		15		ns
LOW−SIDE GATE DRIVE						
Pull−High Drive ON Resistance	$V_{CCP} - V_{PGND}$ = 5 V	R_{DRV_LH}	−	0.9	3.0	Ω
Pull−Low Drive ON Resistance	$V_{CCP} - V_{PGND}$ = 5 V	R_{DRV_LL}	−	0.4	1.25	Ω
GL Propagation Delay Time	From GH falling to GL rising	T_{GL_d}		10		ns
SW to PGND RESISTANCE						
SW to PGND Pull−Down Resistance	(Note 5)	R_{SW}	−	1.88	−	kΩ
BOOTSTRAP RECTIFIER SWITCH						
On Resistance	EN = L or EN = H and DRVL = H	R_{on_BST}	5	13	22	Ω

5. Guaranteed by design, not tested in production.
6. T_J = 25°C.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



NOTE: Timing is referenced to the 90% and 10% points, unless otherwise noted.

Figure 4. Timing Diagram of Gate Drivers

Table 4. STATE TRUTH TABLE

STATE	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	Method of Reset
POR 0 < VCC < UVLO	N/A	N/A	N/A	
Disabled EN < threshold UVLO > threshold	Low	Low	Disabled	
Start up Delay & Calibration EN > threshold UVLO > threshold	Low	Low	Disabled	
Soft Start EN > threshold UVLO > threshold	Low	Operational	Active / No latch	
Normal Operation EN > threshold UVLO > threshold	High	Operational	Active / Latching	N/A
Over Voltage	Low	N/A	DAC + 400 mV	
Over Current	Low	Operational	Last DAC Code	
Vout = 0 V	Low: if Reg34h:bit0 = 0; High:if Reg34h:bit0 = 1	Clamped at 0.9 V	Disabled	

DETAILED DESCRIPTION

General

The NCP81250, a single−phase synchronous buck regulator, integrates power MOSFETs to provide a high−efficiency and compact−footprint power management solution for new generation computing CPUs. The device is able to deliver up to 14 A TDC output current on an adjustable output with SVID interface. Operating in high switching frequency up to 1.2 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. Current−mode RPM control with feedforward from both input power supply and output voltage ensures stable operation over wide operation condition.

Current−Mode RPM Operation

The NCP81250 operates with the current−mode Ramp−Pulse−Modulation (RPM) scheme in PS0/1/2/3 operation modes. In forced CCM mode, the inductor current is always continuous and the device operates in quasi−fixed switching frequency, which has a typical value programmed by users through a resistor at pin FREQ. In auto CCM/DCM mode, the inductor current is continuous and the device operates in quasi−fixed switching frequency in medium and heavy load range, while the inductor current becomes discontinuous and the device automatically operates in PFM mode with an adaptive fixed on time and variable switching frequency in light load range.

Serial VID interface (SVID)

The NCP81250 supports Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). For NCP81250, VID code change rate is controlled by the SVID interface with three options. Information regarding SVID interface can be obtained from Intel.

Boot Voltage and SVID Address

Table 5 shows two boot voltage options of 0.9 V and 1.35 V programmed by an external 1% resistor Rvboot from Vboot pin to GND, which programs SVID address as well. Both values are set on power up and cannot be changed after the initial power up sequence is complete.

Table 5. BOOT VOLTAGE AND SVID ADDRESS CONFIGURATION

Rvboot (Ω)	Vboot Pin Voltage (mV)			Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	0.9
14.0k	102	140	180	0x1	0.9
22.1k	180	219	258	0x2	0.9
30.1k	258	301	344	0x3	0.9
39.2k	344	391	438	0x4	0.9
48.7k	438	484	531	0x5	0.9
57.6k	531	578	625	0x6	0.9
68.1k	625	676	727	0x7	0.9
78.7k	727	781	836	0x8	0.9
88.7k	836	894	953	0x0	1.35
100k	953	1007	1062	0x1	1.35
113k	1062	1125	1188	0x2	1.35
124k	1188	1250	1312	0x3	1.35
137k	1312	1378	1445	0x4	1.35
150k	1445	1511	1578	0x5	1.35
165k	1578	1648	1719	0x6	1.35
178k	1719	1789	1859	0x7	1.35
196k	1859	1950	–	0x8	1.35

Switching Frequency

Switching frequency is programmed by a resistor R_{FREQ} to ground at the FREQ pin. The typical frequency range is from 500 kHz to 1.2 MHz. The FREQ pin provides approximately 2 V out and the source current is mirrored into the internal ramp generator. The switching frequency can be found in Figure 5 with a given R_{FREQ}. The frequency shown in Figure 5 is under condition of 10 A output current at VID = 1 V. The frequency has a variation over VID voltage and loading current, which maintains similar output ripple voltage over different operation condition. Figure 6 shows frequency variations over the VID voltage range.

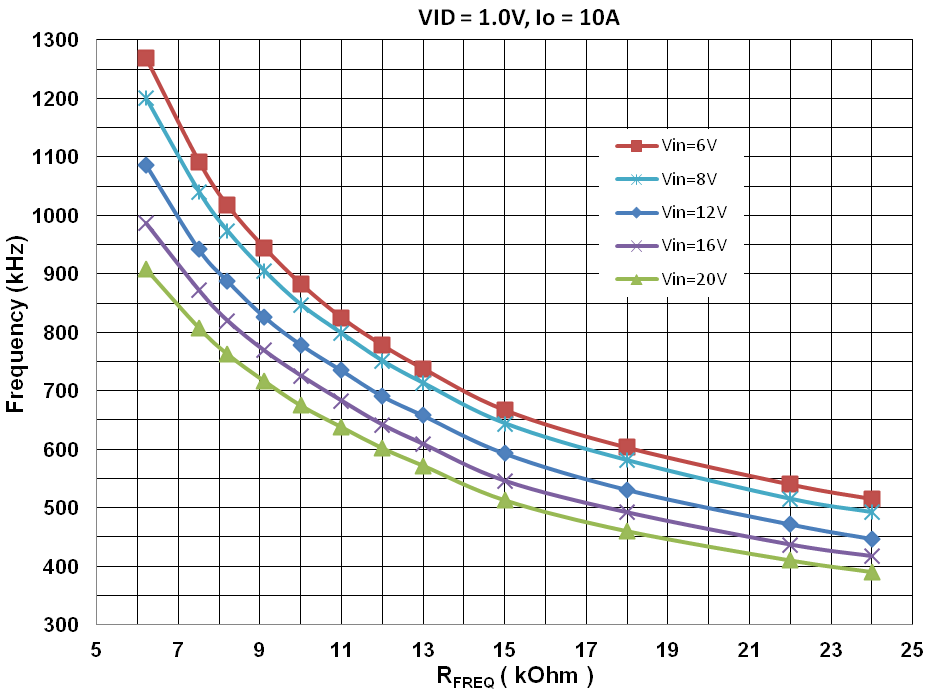


Figure 5. Switching Frequency vs. R_{FREQ}

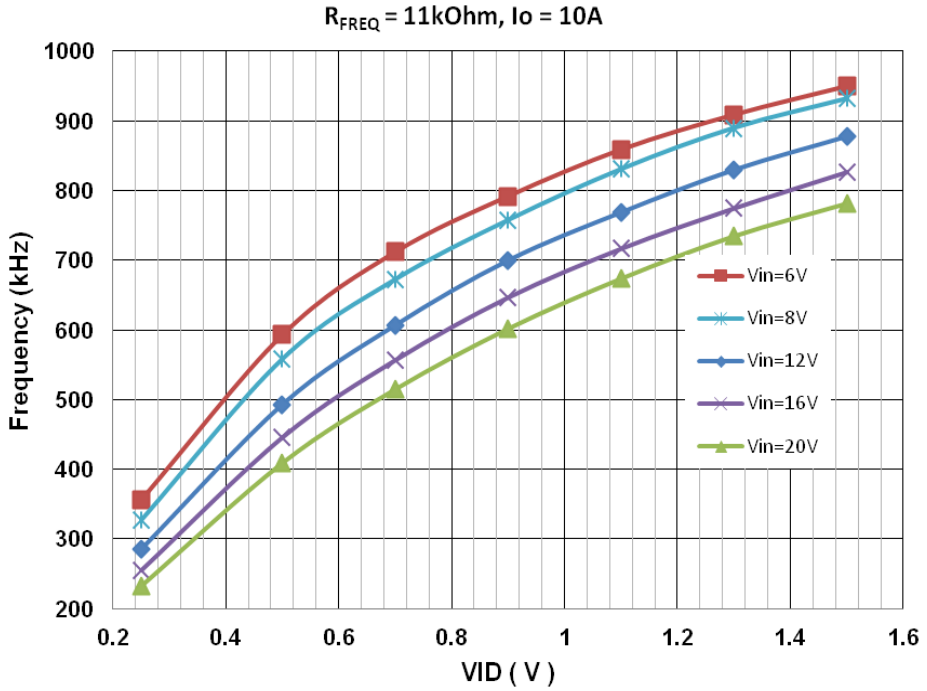


Figure 6. Switching Frequency vs. VID Voltage

Remote Voltage Sense

A high performance differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The output (DIFOUT) of the remote sense amplifier is a sum of the error voltage (between the output VSP−VSN and the DAC) and a 1.3 V DC bias.

$$V_{DIFOUT} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) \qquad \text{(eq. 1)}$$

The DIFOUT signal then goes through a compensation network and into the inverting input (FB pin) of an error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V used for the differential sense amplifier output bias.

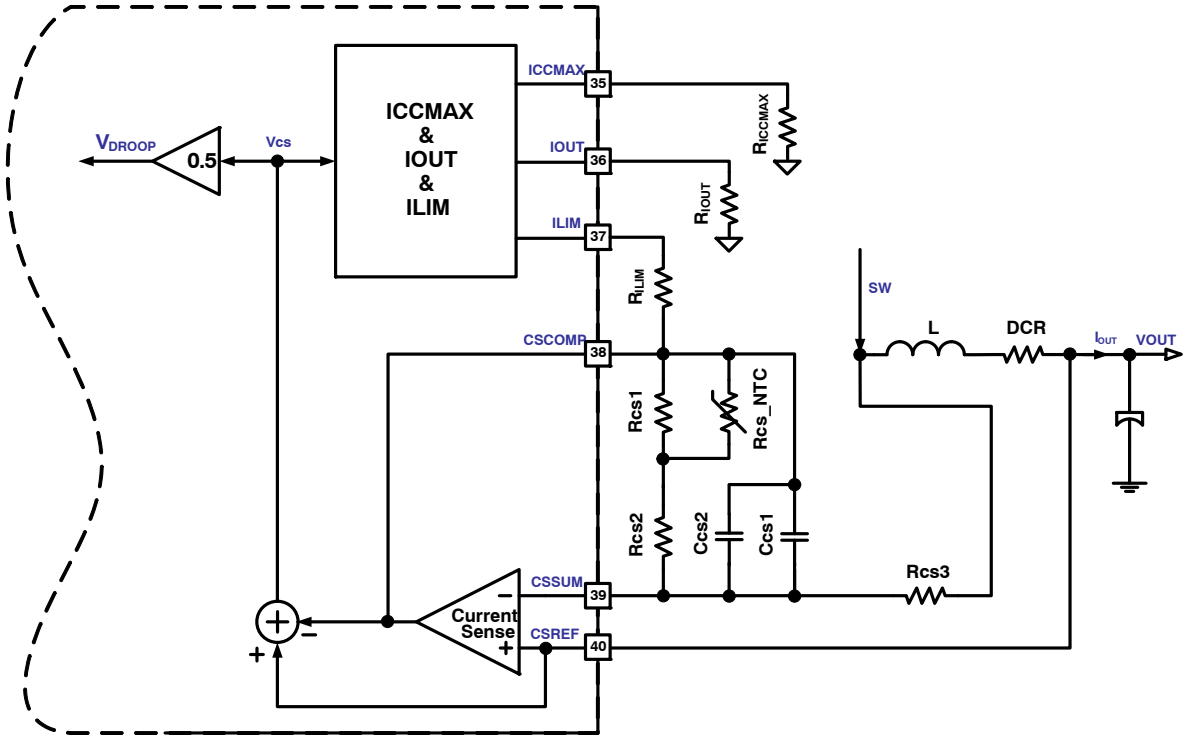


Figure 7. Differential Current−Sense Circuit Diagram

Differential Current Sense

The differential current−sense circuit diagram is shown in Figure 7. An internally−used voltage signal Vcs, representing the inductor current level, is the voltage difference between CSREF and CSCOMP. The output side of the inductor is used to create a low impedance virtual ground. The current−sense amplifier actively filters and gains up the voltage applied across the inductor to recover the voltage drop across the inductor's DC resistance (DCR). RCS_NTC is placed close to the inductor to sense the temperature. This allows the filter time constant and gain to be a function of the Rth_NTC resistor and compensate for the change in the DCR with temperature. The DC gain in the current sensing loop is

$$G_{CS} = \frac{V_{CS}}{V_{DCR}} = \frac{V_{CSREF} - V_{CSCOMP}}{I_{OUT} \cdot DCR} = \frac{R_{CS}}{R_{CS3}} \qquad \text{(eq. 2)}$$

Where

$$R_{CS} = R_{CS2} + \frac{R_{CS1} \cdot R_{CS_NTC}}{R_{CS1} + R_{CS_NTC}} \qquad \text{(eq. 3)}$$

The values of Rcs1 and Rcs2 are set based on a 220k NTC thermistor and the temperature effect of the inductor and thus usually they should not need to be changed. The gain Gcs can be adjusted by the value change of the Rcs3 resistor to provide about 100 mV in Vcs at full load.

In order to recover the inductor DCR voltage drop current signal, the pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor, that means

$$C_{CS1} + C_{CS2} = \frac{L}{DCR \cdot R_{CS}} \qquad \text{(eq. 4)}$$

Ccs1 and Ccs2 are in parallel to allow for a fine tuning of the time constant using commonly available values.

Over Current Protection

The NCP81250 provides two different types of current limit protection. Current limits are programmed with a resistor RILIM between the CSCOMP pin and the ILIM pin. The current from the ILIM pin to this resistor is then compared to two internal currents (10 μA and 15 μA) corresponding to two different current limit thresholds ILIM and ILIM_Fast (150% of ILIM level). If the ILIM pin current exceeds the 10 μA level, an internal latch−off timer starts. The controller shuts down if the fault is not removed after 50 μs. If the current into the pin exceeds 15 μA the

controller will shut down immediately. To recover from an OCP fault the EN pin must be cycled low.

The value of RILIM can be designed using the following equation with a required over current protection threshold ILIM and a known current−sense network.

$$R_{ILIM} = \frac{V_{CS}@I_{LIM}}{10\ \mu} = \frac{R_{CS}}{R_{CS3}} \cdot I_{LIM_PK} \cdot DCR \cdot 10^5 = \frac{R_{CS}}{R_{CS3}} \cdot \left(I_{LIM} + \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{2 \cdot L \cdot F_{SW} \cdot V_{IN}} \right) \cdot DCR \cdot 10^5 \quad \text{(eq. 5)}$$

ICC_MAX

A resistor connected from IMAX pin to ground sets ICC_MAX value at startup. A 10 μA current is sourced from this pin to generate a voltage on the program resistor. The resistor value can be determined by the following equation. The resistor value should be no less than 10 k.

$$ICC_MAX = \frac{R_{ICCMAX} \cdot 10\ \mu \cdot 64}{2} = R_{ICCMAX} \cdot 3.2 \cdot 10^{-4} \quad \text{(eq. 6)}$$

IOUT

The IOUT pin sources a current equal to the ILIM sink current gained by the IOUT Current Gain (10 typ.). The voltage of the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor to 5 V V_{CC} can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2}{10 \cdot V_{CS}@ICC_MAX} \cdot R_{ILIM} = \frac{1}{5 \cdot \frac{R_{CS}}{R_{CS3}} \cdot ICC_MAX \cdot DCR} \cdot R_{ILIM} \quad \text{(eq. 7)}$$

Input UVLO Protection

NCP81250 monitors supply voltages at the VCC pin and the VIN pins in order to provide under voltage protection. If either supply drops below its threshold, the controller will shut down the outputs. Upon recovery of the supplies, the controller reenters its startup sequence, and soft start begins.

Output Under−Voltage Protection

The output voltage is monitored by a dedicated differential amplifier. If the output falls below target by more than “Under Voltage Threshold below DAC−Droop”, the UVL comparator sends the VR_RDY signal low.

Output Over−Voltage Protection

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If the output voltage exceeds the DAC voltage by “Over Voltage Threshold above DAC”, GH will be forced low, and GL will go high. After the OVP trips, the DAC ramps slowly down to zero to avoid a negative output voltage spike during shutdown. If the DAC+OVP Threshold drops below the output, GL will again go high, and will toggle between low and high as the output voltage follows the DAC+OVP Threshold down. When the DAC gets to zero, the GH will be held low and the GL will remain high. To reset the part, the EN pin must be cycled low. During soft−start, the OVP threshold is set to 2.9 V. This allows the controller to start up without false triggering the OVP.

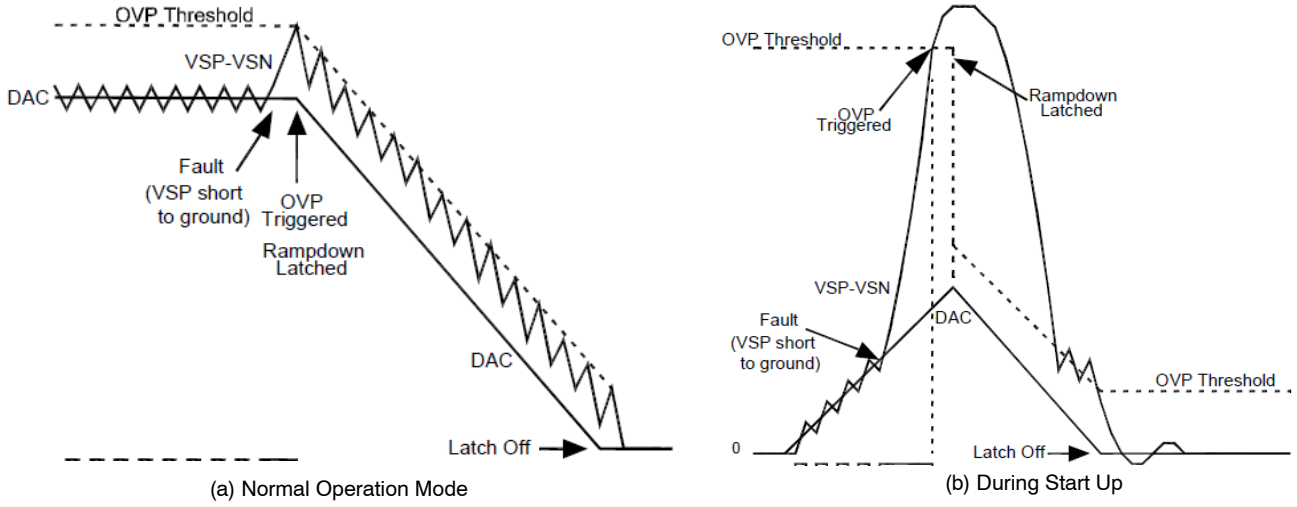


Figure 8. Function of Over Voltage Protection

Temperature Sense and Thermal Alert

The NCP81250 provides an external temperature sense and a thermal alert in normal operation mode. The temperature sense and thermal alert circuit diagram is shown in Figure 9. A precision current I_{TSENSE} is sourced out the output of the TSENSE pin to generate a voltage across the temperature sense network, which consists of a NTC thermistor R_NTC (100 kΩ typ.), two resistors R_COMP1 (0 Ω typ.) and R_COMP2 (8.2 kΩ typ.), and a filter capacitor C_Filter (0.1 μF typ.). The voltage on the temperature sense input is sampled by the internal A/D converter and then digitally converted to temperature and stored in SVID register 17h. Usually the thermistor is placed close to a hot spot like inductor or NCP81250 itself. A 100k NTC thermistor similar to the Murata NCP15WF104D03RC should be used. The NCP81250 also monitors the voltage at the TSENSE pin and compares the voltage to internal thresholds and assert ALERT# or VRHOT# once it trips the thresholds. The DC voltage at TSENSE pin can be calculated by

$$V_{TSENSE} = I_{TSENSE} \cdot \left(R_{COMP1} + \frac{R_{COMP2} \cdot R_{NTC_T}}{R_{COMP2} + R_{NTC_T}} \right) \quad \text{(eq. 8)}$$

R_{NTC_T} is the resistance of R_NTC at an absolute temperature T, which is obtained by

$$R_{NTC_T} = R_{NTC_T_0} \cdot \exp\left(B \cdot \left(\frac{1}{T} - \frac{1}{T_0} \right) \right) \quad \text{(eq. 9)}$$

where R_{NTC_T0} is a known resistance of R_NTC at an absolute temperature T_0, and B is the B−constant of R_NTC.

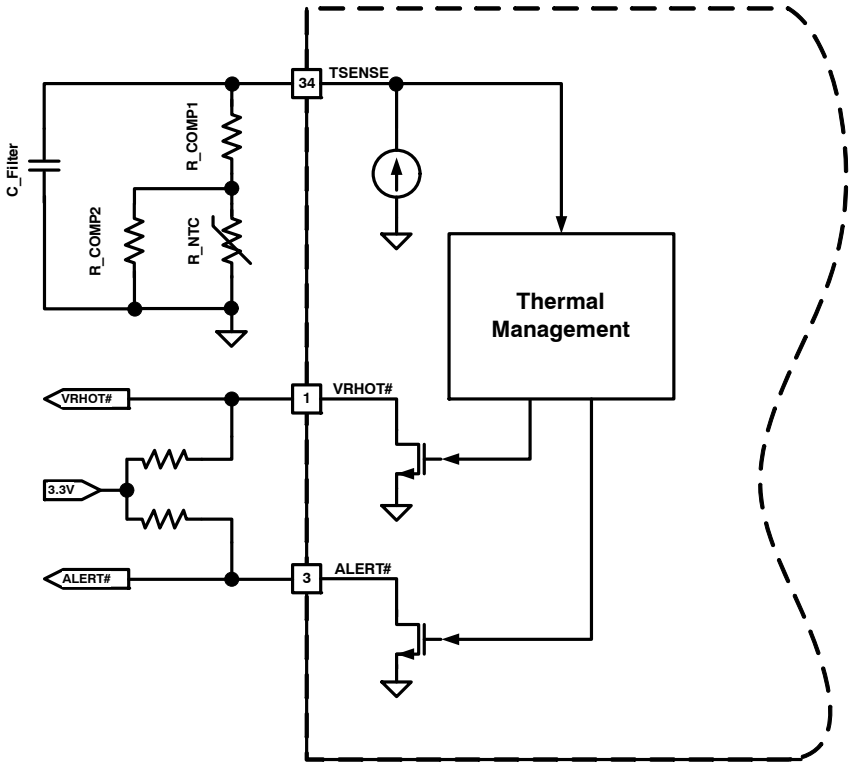


Figure 9. Temperature Sense and Thermal Alert Circuit Diagram

LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- **Power Paths:** Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling:** The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to VIN and PGND pins.
- **VCC Decoupling:** Place decoupling caps as close as possible to the controller VCC and VCCP pins. The filter resistor at VCC pin should be not higher than 2.2 Ω to prevent large voltage drop.
- **Switching Node:** SW node should be a copper pour, but compact because it is also a noise source.
- **Bootstrap:** The bootstrap cap and an option resistor need to be very close and directly connected between pin 8 (BST) and pin 10 (SW). No need to externally connect pin 10 to SW node because it has been internally connected to other SW pins.
- **Ground:** It would be good to have separated ground planes for PGND and GND and connect the two planes at one point. Directly connect GND pin to the exposed pad and then connect to GND ground plane through vias.
- **Voltage Sense:** Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense.
- **Current Sense:** Careful layout for current sensing is critical for jitter minimization, accurate current limiting, and IOUT reporting. The filter cap from CSCOMP to CSREF should be close to the controller. The temperature compensating thermistor should be placed as close as possible to the inductor. The wiring path should be kept as short as possible and well away from the switch node.
- **Compensation Network:** The small feedback cap from COMP to FB should be as close to the controller as possible. Keep the FB traces short to minimize their capacitance to ground.
- **SVID Bus:** The Serial VID bus is a high speed data bus and the bus routing should be done to limit noise coupling from the switching node. The signals should be routed with the Alert# line in between the SVID clock and SVID data lines. The SVID lines must be ground referenced and each line’s width and spacing should be such that they have nominal 50 Ω impedance with the board stackup.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

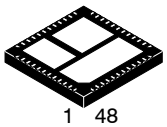
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PACKAGE DIMENSIONS

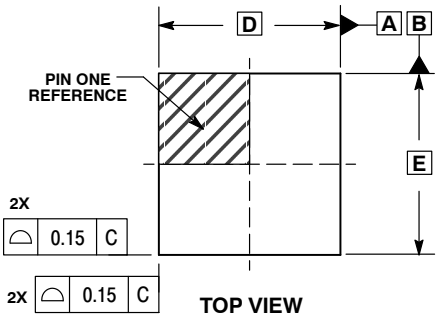
ON Semiconductor®

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CASE 485CJ
ISSUE A

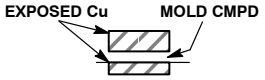
DATE 09 AUG 2012



SCALE 2:1

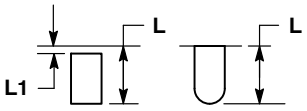


TOP VIEW



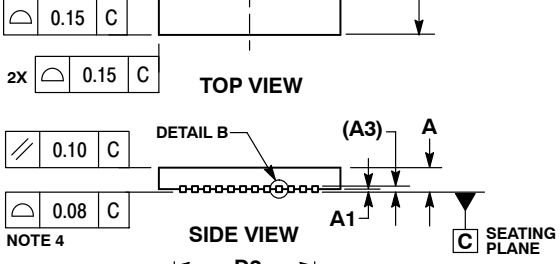
DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS IN BOTH X AND Y AXIS.

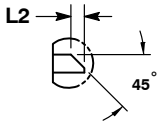


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

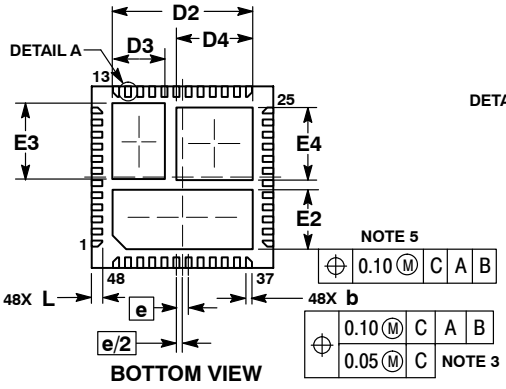
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.53	4.73
D3	1.64	1.84
D4	2.42	2.62
D5	4.58	4.78
E	6.00 BSC	
E2	1.86	2.06
E3	2.41	2.61
E4	2.30	2.50
e	0.40 BSC	
G3	1.45 BSC	
G4	1.06 BSC	
H2	1.40 BSC	
H3	1.19 BSC	
H4	1.10 BSC	
L	0.25	0.45
L1	---	0.15
L2	0.15 REF	



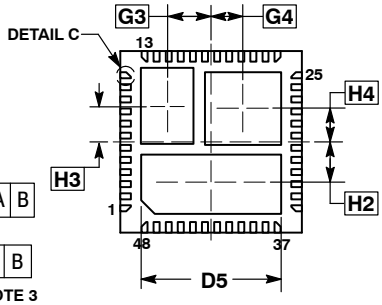
SIDE VIEW



DETAIL C

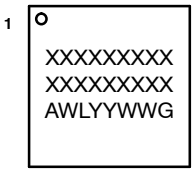


BOTTOM VIEW



SUPPLEMENTAL BOTTOM VIEW

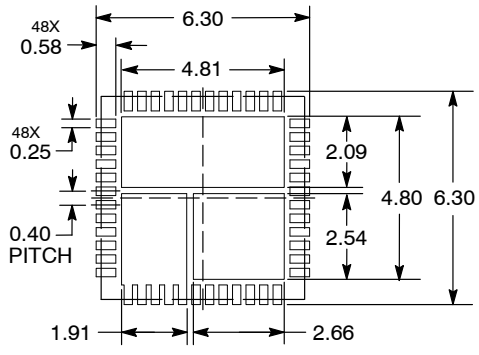
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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