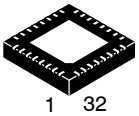
Power Management Unit - Automotive, Battery-Connected, Multi-Output

NCV97311A

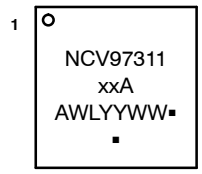
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QFNW32
MW SUFFIX
CASE 484AB

MARKING DIAGRAM



xx	= 33 or 50
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 23 of this data sheet.

Description

The NCV97311A is a 3−output regulator consisting of a low−Iq battery−connected 3 A, 2 MHz non−synchronous switcher and two low−voltage 1.5 A, 2 MHz synchronous switchers; all using integrated power transistors.

The high−voltage switcher is capable of converting a 4.1 V to 18 V battery input to a 5 V or 3.3 V output at a constant 2 MHz switching frequency, delivering up to 3 A. In overvoltage conditions up to 37 V, the switching frequency folds back to 1 MHz; in load dump conditions up to 45 V the regulator shuts down.

The output of the battery−connected buck regulator serves as the low voltage input for the 2 downstream synchronous switchers. Each downstream output is adjustable from 1.2 V to 3.3 V, with a 1.5 A average current limit and a constant 2 MHz switching frequency. Each switcher has an independent enable and reset pin, giving extra power management flexibility.

For low−Iq operating mode, the low−voltage switchers are disabled and the standby rail is supplied by a low−Iq LDO (up to 150 mA) with a typical Iq of 30 μA. The LDO regulator is in parallel to the high−voltage switcher, and is activated when the switcher is forced in standby mode.

All 3 SMPS outputs use peak current mode control with internal slope compensation, internally−set soft−start, battery undervoltage lockout, battery overvoltage protection, cycle−by−cycle current limiting, hiccup mode short−circuit protection and thermal shutdown. An error flag is available for diagnostics.

Features

- 5.0 V and 3.3 V Versions Available
- Low Quiescent Current in Standby Mode
- Programmable Spread Spectrum for EMI Reduction
- 2 Microcontroller Enabled Low Voltage Synchronous Buck Converters
- Large Conversion Ratio of 18 V to 3.3 V Battery Connected Switcher
- Wide Input of 4.1 to 45 V with Undervoltage Lockout (UVLO)
- Fixed Frequency Operation Adjustable from 2.0 to 2.6 MHz
- Internal 1.5 ms Soft−starts
- Cycle−by−cycle Current Limit Protections
- Hiccup Overcurrent Protections (OCP)
- Individual Reset Pins with Adjustable Delays
- QFN Package with Wettable Flanks (pin edge plating)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Infotainment, Body Electronics, Telematics, ECU

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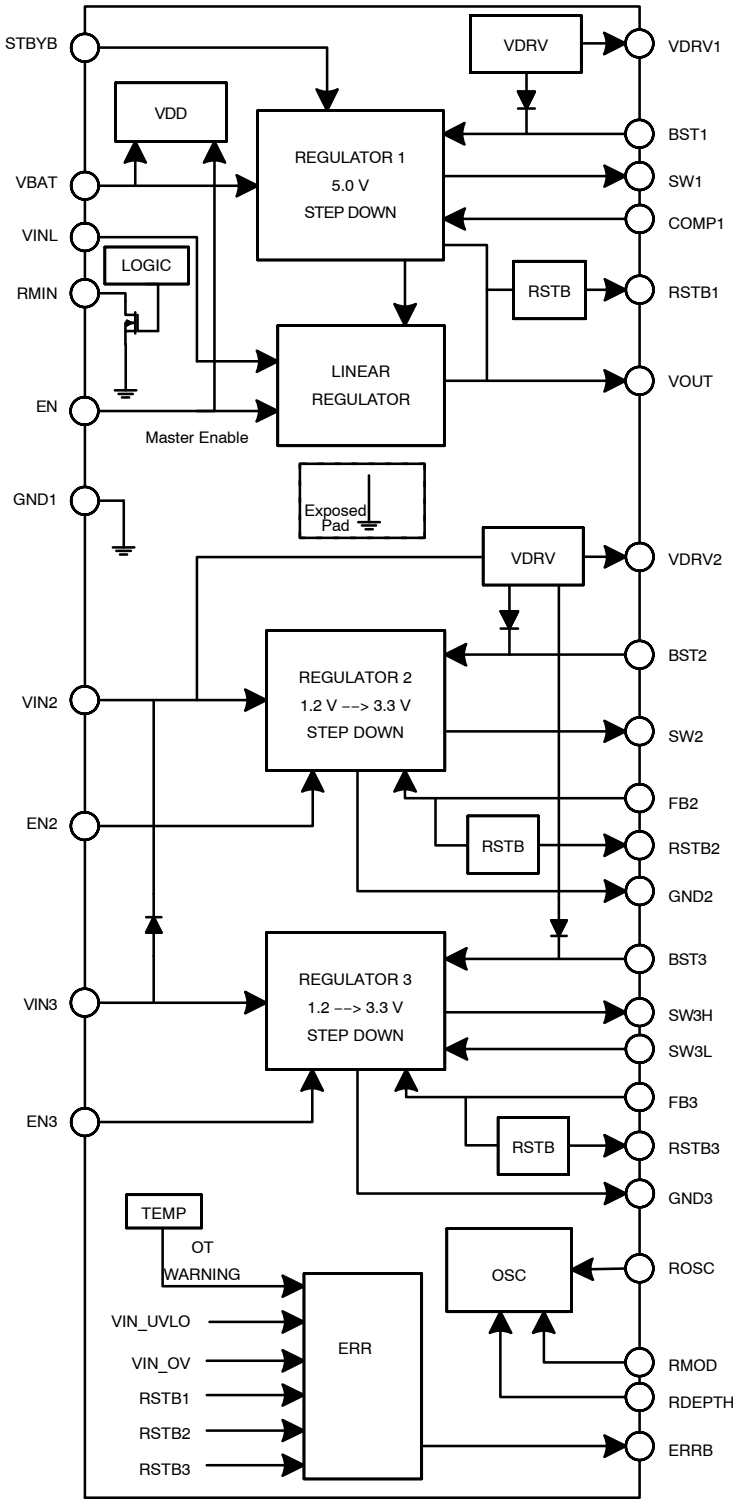


Figure 1. NCV97311A Block Diagram – 5.0 V Version

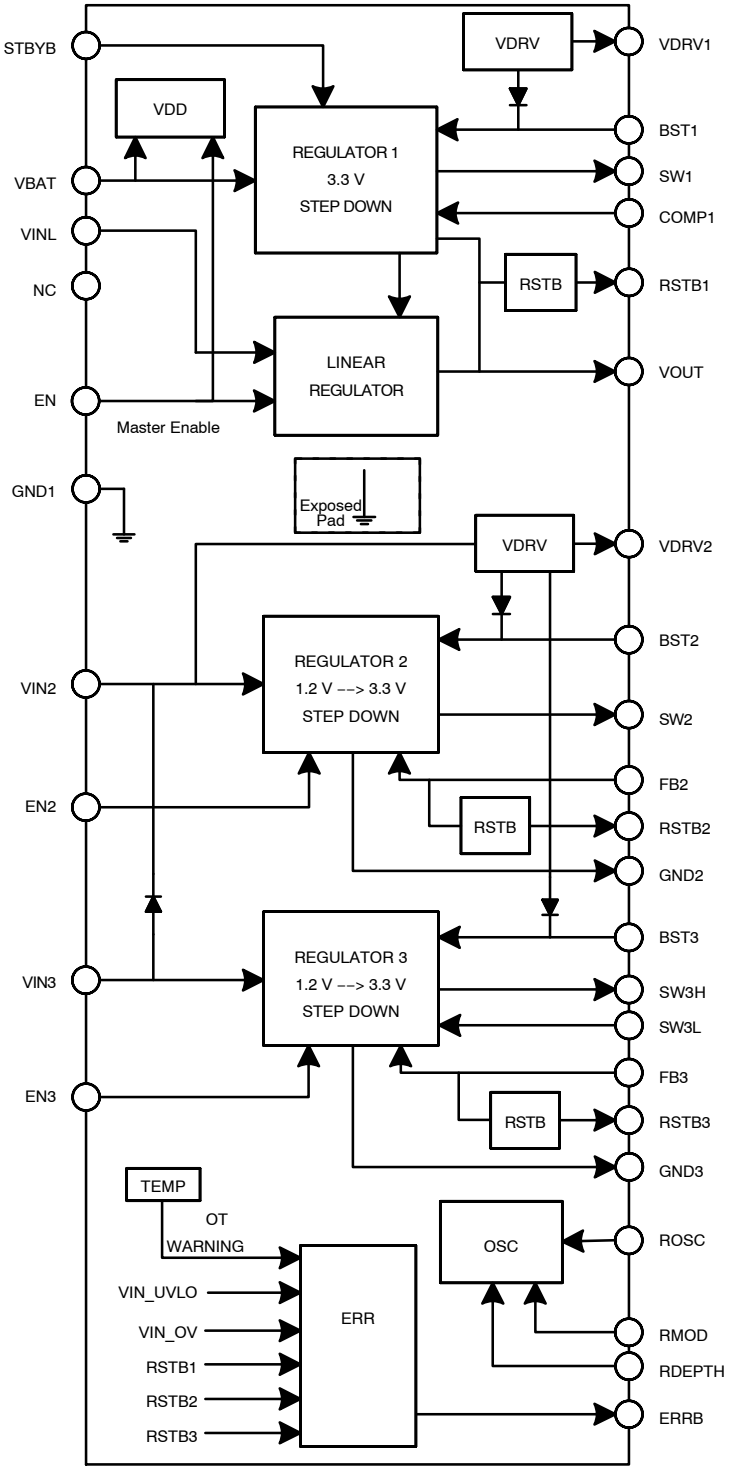


Figure 2. NCV97311A Block Diagram – 3.3 V Version

TYPICAL APPLICATION

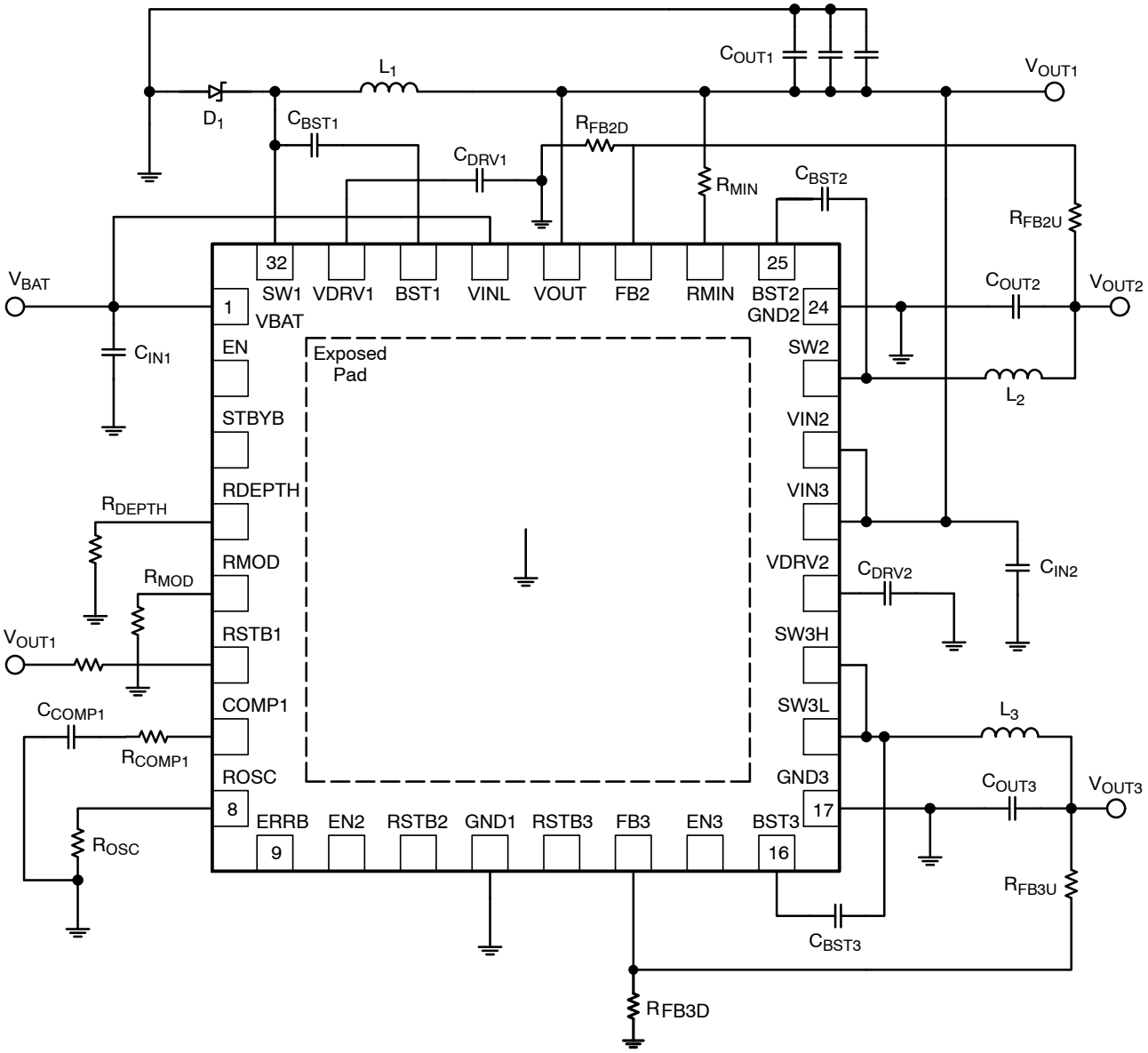


Figure 3. Typical Application – 5.0 V Version

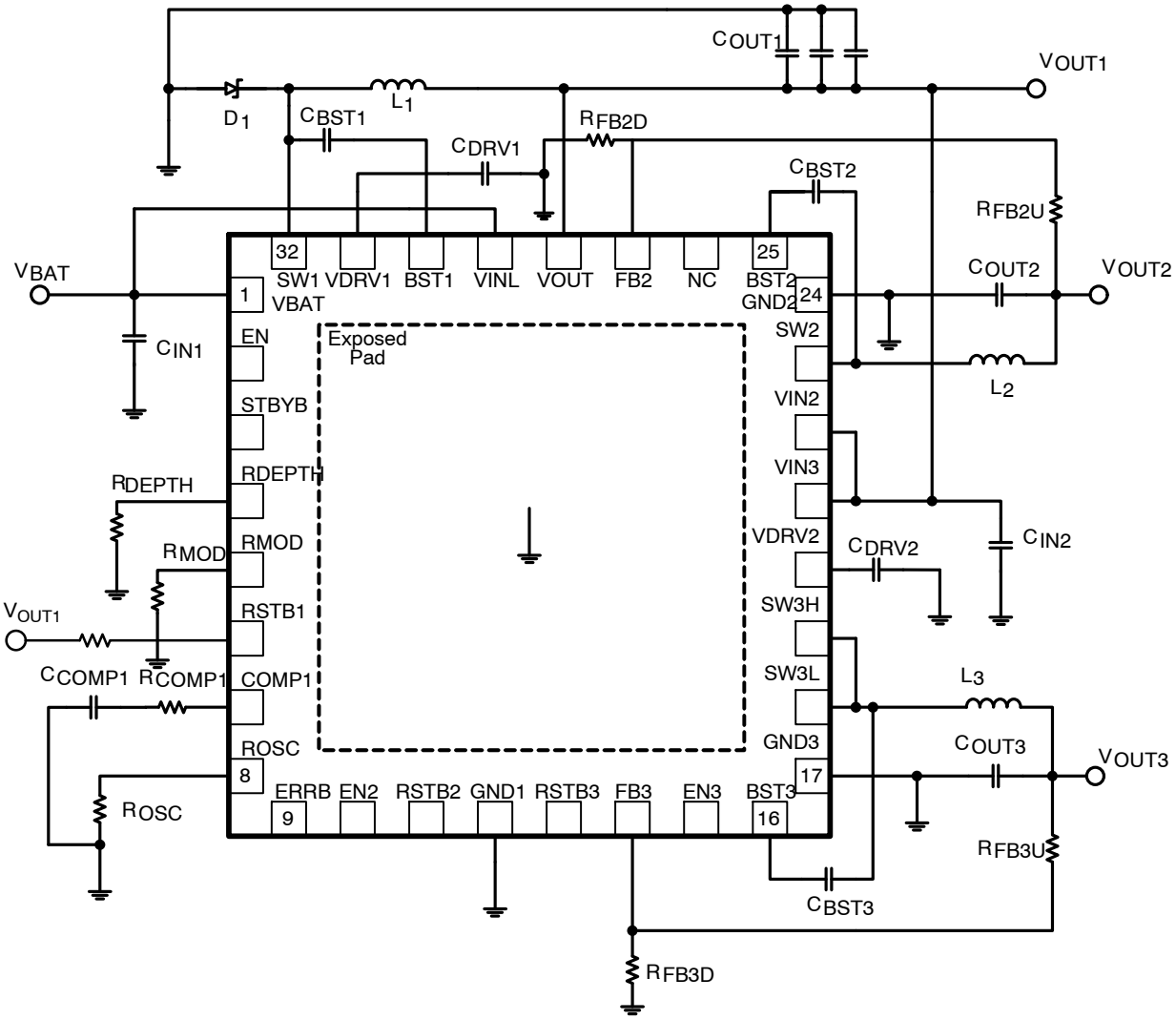


Figure 4. Typical Application – 3.3 V Version

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Min/Max Voltage VBAT, VINL		−0.3 to 45	V
Max Voltage VBAT to SW1		45	V
Min/Max Voltage SW1		−0.7 to 40	V
Min Voltage SW1, SW2, SW3 − 20 ns		−3.0	V
Min/Max Voltage BST1, STBYB, EN		−0.3 to 40	V
Min/Max Voltage VIN2, VIN3, BST2, BST3, SW2, SW3H, SW3L, VOUT, RMIN		−0.3 to 12	V
Min/Max Voltage on RSTB1, RSTB2, RSTB3, ERRB, EN2, EN3, FB2, FB3		−0.3 to 6	V
Max Voltage BST1 to SW1, BST2 to SW2, BST3 to SW3x		3.6	V
Min/Max Voltage VDRV1, VDRV2, COMP1, ROSC, RMOD, RDEPTH		−0.3 to 3.6	V
Thermal Resistance, 5 x 5 QFN Junction − to − Ambient (Note 1)	$R_{\theta JA}$	25	°C/W
Storage Temperature Range		−55 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +150	°C
ESD Withstand Voltage — Human Body Model Machine Model	V_{ESD}	2.0* 200	kV V
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Mounted on 1 sq. in. of a 4−layer PCB with 1 oz. copper thickness.
*BST2, BST3 HBM 1.5 kV

Table 2. RECOMMENDED OPERATING CONDITIONS

Rating	Value
VIN Range	4.5 V to 34 V
Ambient Temperature Range	−40°C to 125°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	VBAT	Input voltage from battery. Place an input filter capacitor in close proximity to this pin. Must be tied to Pin 29 – VINL.
2	EN	High−voltage (battery), TTL−compatible, master enable signal. Grounding this input stops all outputs and reduces Iq to a minimum (shutdown mode).
3	STBYB	High−voltage (battery), TTL−compatible, mode selection signal. Grounding this input activates the low−Iq mode of operation for switcher 1 (standby mode).
4	RDEPTH	Modulation depth adjustment (% of FSW) for spread spectrum. Set with a resistor to GND.
5	RMOD	Modulation frequency adjustment for spread spectrum. Set with a resistor to GND.
6	RSTB1	Reset with adjustable delay. Goes low when the output is out of regulation. When using Low−Iq LDO Mode, connect a pull−up resistor to a permanent external supply (e.g. V_{OUT1}).
7	COMP1	Output of the error amplifier for switcher 1
8	ROSC	Provides Frequency Adjustment
9	ERRB	Error flag combining temperature and input and output voltage sensing
10	EN2	TTL compatible low voltage input. Grounding this input stops switcher 2.
11	RSTB2	Reset with adjustable delay. Goes low when the output is out of regulation.
12	GND1	Ground reference for the IC.
13	RSTB3	Reset with adjustable delay. Goes low when the output is out of regulation.
14	FB3	Output voltage sensing, provides adjustability.
15	EN3	TTL compatible low voltage input. Grounding this input stops switcher 3.
16	BST3	Bootstrap input provides drive voltage higher than VIN3 to the high−side N−channel Switch for optimum switch $R_{DS(on)}$ and highest efficiency.
17	GND3	Ground connection for the source of the low−side switch of switcher 3.
18	SW3L	Drain of the low−side switch. Connect the output inductor to this pin. Must be tied to SW3H.
19	SW3H	Source of the high−side switch. Connect the output inductor to this pin. Must be tied to SW3L.
20	VDRV2	Internal supply voltage for driving the low−voltage internal switches. Connect a capacitor for noise filtering purposes.
21	VIN3	Low Input voltage for switcher 3. Place an input filter capacitor in close proximity to this pin. Must be connected to Pin 22 – VIN2 and Pin 28 – VOUT.
22	VIN2	Low Input voltage for switcher 2. Place an input filter capacitor in close proximity to this pin. Must be connected to Pin 21 – VIN3 and Pin 28 – VOUT.
23	SW2	Switching node of the switcher 2 regulator. Connect the output inductor to this pin.
24	GND2	Ground connection for the source of the low−side switch of switcher 2.
25	BST2	Bootstrap input provides drive voltage higher than VIN2 to the high−side N−channel Switch for optimum switch $R_{DS(on)}$ and highest efficiency.
26	RMIN	5.0 V Version: Minimum load pull−down for switcher mode. Connect a resistor to VOUT1, if needed (see applications section for details).
	NC	3.3 V Version: This pin is a no−connect. Leave the pin floating.
27	FB2	Output voltage sensing, provides adjustability.
28	VOUT	Output voltage sensing. Delivers the output current in low−Iq mode
29	VINL	Input voltage from battery. Place an input filter capacitor in close proximity to this pin. Must be tied to Pin1 – VBAT.
30	BST1	Bootstrap input provides drive voltage higher than VBAT to the N−channel Power Switch for optimum switch Rdson and highest efficiency.
31	VDRV1	Internal supply voltage for driving the low−voltage internal switch. Connect a capacitor for noise filtering purposes.
32	SW1	Switching node of the Regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
Exposed Pad		Must be connected to GND1 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

Table 4. ELECTRICAL CHARACTERISTICS (V_{BAT} = V_{INL} = 4.5 V to 28 V, V_{EN} = V_{STBYB} = V_{EN2} = V_{EN3} = 5 V, V_{BSTx} = V_{SWx} + 3.0 V, C_{DRV1} = 0.1 μF, C_{DRV2} = 0.47 μF. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Quiescent Current, shutdown	I_{qSD}	V_{BAT} = V_{INL}= 13.2 V, T_J=25°C, V_{EN} = 0 V		8	12	μA
Quiescent Current, standby	I_{qEN}	V_{BAT} = V_{INL} = 13.2 V, T_J=25°C V_{EN} = 3 V, V_{STBYB} = V_{EN2} = V_{EN3} = 0 V		25	35	μA
UNDERVOLTAGE LOCKOUT – VBAT (UVLO)						
VBAT UVLO Start Threshold	V_{UV1ST}	V_{BAT} rising	4.45		4.85	V
VBAT UVLO Stop Threshold	V_{UV1SP}	V_{BAT} falling	3.7		4.1	V
VBAT UVLO Hysteresis	V_{UV1HY}			0.75		V
ENABLE						
Logic Low (Voltage input needed to guarantee logic low)	V_{ENLO}, V_{EN2LO}, V_{EN3LO}, $V_{STBYBLO}$				0.8	V
Logic High (Voltage input needed to guarantee logic high)	V_{ENHI}, V_{EN2HI}, V_{EN3HI}, $V_{STBYBHI}$		2			V
Enable pin input Current	I_{EN}	V_{EN} = 5 V		0.125	1.0	μA
	I_{STBYB}	V_{STBYB} = 5 V		0.5	2.0	
	I_{EN2}, I_{EN3}	V_{EN2} = V_{EN3} = 5 V	30	50	70	
Switcher 1 start−up time	t_{STBYB}	STBYB 'High' to Switcher 1 ready		60	200	μs
OUTPUT VOLTAGE						
Switcher 1 output	V_{OUT}	5.0 V Version 3.3 V Version	4.9 3.23	5.0 3.3	5.1 3.37	V
V_{OUT} Line regulation in Low−Iq mode	V_{Line1}	I_{OUT} = 50 mA, V_{STBYB} = 0 V, 6 V < V_{INL} = V_{BAT} < 28 V		5	25	mV
V_{OUT} Load regulation in Low−Iq mode	V_{Load1}	V_{INL} = V_{BAT} = 13.2 V, V_{STBYB} = 0 V, 1 mA < I_{OUT} < 150 mA		10	35	mV
Voltage drop−out in Low−Iq mode	V_{DROP1}	I_{OUT} = 150 mA, V_{STBYB} = 0 V			500	mV
Switchers 2 and 3 FB Pin Voltage during regulation	V_{FB2R}, V_{FB3R}	OUTx connected to FBx through a 10 kΩ resistor	1.179	1.200	1.221	V
ERROR AMPLIFIER – SWITCHER 1						
Transconductance (Note 2)	g_m $g_{m(HV)}$	V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	0.6 0.35	1.0 0.55	1.4 0.75	mmho
Output Resistance	R_{OUT}			1.4		MΩ
COMP Source Current Limit	I_{SOURCE}	V_{OUT} = 4.0 V, V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	 50 25	 75 40	 100 55	μA
COMP Sink Current Limit	I_{SINK}	V_{OUT} = 6.0 V, V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	 50 25	 75 40	 100 55	μA
Minimum COMP voltage	V_{CMPMIN}	V_{OUT} = 6.0 V		0.15	0.3	V
Maximum COMP voltage	V_{CMPMAX}	V_{OUT} = 4.0 V	1.3	1.6		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Not tested in production. Limits are guaranteed by design.
3. Minimum load parameters are only valid for the 5.0 V version, OPN: NCV97311MW50AR2G

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Switching Frequency − switcher 1	f_{SW1} $f_{SW1(HV)}$	4.5 < V_{BAT} < 18 V, R_{OSC} = open 20 V < V_{BAT} < 28 V, R_{OSC} = open	1.8 0.9	2.0 1.0	2.2 1.1	MHz
Switching Frequency − switchers 2 & 3	f_{SW2}, f_{SW3}	R_{OSC} = open	1.8	2.0	2.2	MHz
Switching Frequency − R_{OSC}	f_{ROSC}	R_{OSC} = 12.5 kΩ	2.3	2.5	2.8	MHz
R_{OSC} reference voltage	V_{ROSC}	R_{OSC} = 25 kΩ	0.9	1.0	1.1	V
VBAT OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage Stop Threshold	V_{OV1SP}		37		40	V
Overvoltage Start Threshold	V_{OV1ST}		34			V
Overvoltage Hysteresis	V_{OV1HY}		0.6		2.7	V
VBAT FREQUENCY FOLDBACK MONITOR						
Frequency Foldback Threshold	V_{FL1U} V_{FL1D}	V_{BAT} rising V_{BAT} falling	18.4 18		20 19.8	V
Frequency Foldback Hysteresis	V_{FL1HY}		0.2	0.3	0.4	V
SOFT−START						
Soft−Start Completion Time	t_{SS1}, t_{SS2}, t_{SS3}		0.8	1.4	2.0	ms
SLOPE COMPENSATION						
Ramp Slope (Note 2) − switcher 1 (With respect to switch current)	S_{ramp1} $S_{ramp1(HV)}$	4.5 < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	1.8 0.8		3.4 1.6	A/μs
Ramp Slope (Note 2) − switchers 2 & 3	S_{ramp2}		1.9		3.7	A/μs
POWER SWITCH − SWITCHER 1						
ON Resistance	R_{DS1ON}	V_{BST1} = V_{SW1} + 3.0 V, I_{SW1} = 500 mA		185	360	mΩ
Leakage current VBAT to SW1	I_{LKSW1}	V_{EN} = 0 V, V_{SW1} = 0, V_{BAT} = 18 V			10	μA
Minimum ON Time	t_{ON1MIN}	Measured at SW1 pin	45		70	ns
Minimum OFF Time	$t_{OFF1MIN}$	Measured at SW1 pin	30	50	70	ns
POWER SWITCHES − SWITCHER 2						
High−Side ON Resistance	R_{HS2ON}	V_{BST2} = V_{SW2} + 3.0 V, I_{SW2} = 500 mA		165	300	mΩ
Low−Side ON Resistance	R_{LS2ON}	I_{SW2} = 500 mA		130	230	mΩ
Leakage current high−side switch	I_{LKSW2}	V_{EN2} = 0 V, V_{SW2} = 0, V_{IN2} = 5.5 V			5	μA
Minimum ON Time	t_{ON2MIN}	Measured at SW2 pin	60	80	95	ns
Minimum OFF Time	$t_{OFF2MIN}$	Measured at SW2 pin	35	55	75	ns
Non−overlap time	t_{NOVLP}			10		ns
POWER SWITCHES − SWITCHER 3						
High−Side ON Resistance	R_{HS3ON}	V_{BST3} = V_{SW3H} + 3.0 V, I_{SW3H} = 500 mA		140	250	mΩ
Low−Side ON Resistance	R_{LS3ON}	I_{SW3L} = 500 mA		130	230	mΩ
Leakage current high−side switch	I_{LKSW3}	V_{EN3} = 0 V, V_{SW3H} = 0, V_{IN3} = 5.5 V			5	μA
Minimum ON Time	t_{ON3MIN}	Measured at SW3x pin	60	80	95	ns
Minimum OFF Time	$t_{OFF3MIN}$	Measured at SW3x pin	35	55	75	ns

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SWITCHES – SWITCHER 3						
Non−overlap time	t_{NOVLP}			10		ns
PEAK CURRENT LIMITS						
Current Limit Threshold – switcher 1 Normal mode Low−Iq mode	 I_{LIM1} $I_{LIM1,stby}$	 V_{STBYB} = 5 V V_{STBYB} = 0 V	 3.9 0.15	 4.4 0.2	 4.9 0.25	A
Current Limit Threshold – switcher 2	I_{LIM2}		2.6	2.9	3.2	A
Current Limit Threshold – switcher 3	I_{LIM3}		2.6	2.9	3.2	A
SHORT CIRCUIT FREQUENCY FOLDBACK – SWITCHER1						
Lowest Foldback Frequency Lowest Foldback Frequency – high V_{IN}	f_{SW1AF} $f_{SW1AFHV}$	V_{OUT} = 0 V, 4.5 V < V_{BAT} < 18 V V_{OUT} = 0 V, 20 V < V_{BAT} < 28 V	450 225	550 275	650 325	kHz
HICCUP MODE						
Hiccup Mode	f_{SW1HIC}, f_{SW2HIC}, f_{SW3HIC}	V_{SWx} = 0 V	24	32	40	kHz
RESET						
Reset Threshold – Switcher 1 (as a ratio of V_{OUT1})	K_{RES_LO1} K_{RES_HI1}	V_{OUT1} decreasing V_{OUT1} increasing	90 90.5	92.5	95 97	%
Reset Threshold – Switchers 2 & 3 (at FBx)	K_{RES_LO2} K_{RES_HI2}	FBx decreasing FBx increasing	1.1		 1.164	V
Reset Hysteresis (ratio of VOUTx)	K_{RES_HYS}		0.5			%
Noise−filtering delay	t_{RES_FILT}		5		25	μs
Reset delay time	t_{RESET}	I_{RSTBx} = 2 mA I_{RSTBx} = 1 mA I_{RSTBx} = 100 μA	 3.5 15	1.0 4.5 30	 5.5 50	μs ms ms
Reset Output Low level	V_{RESL}	I_{RSTBx} = 2 mA			0.4	V
BOOTSTRAP VOLTAGE SUPPLY						
Output Voltage	V_{DRV1}, V_{DRV2}		3.1	3.3	3.5	V
V_{DRVx} POR Start Threshold	V_{DRV1ST} V_{DRV2ST}		2.7 2.35	2.85 2.5	3.05 2.65	V
V_{DRVx} POR Stop Threshold	V_{DRV1SP} V_{DRV2SP}		2.55 2.2	2.75 2.35	2.95 2.5	V
MINIMUM LOAD – 5.0 V VERSION (Note 3)						
RMIN Saturation Voltage	V_{RMIN}	I_{RMIN} = 100 mA into the pin	0.9		2.9	V
VBAT Threshold to Activate RMIN	V_{RMIN_TH}		7.2	7.5	7.9	V
SPREAD SPECTRUM						
RMOD Pin Voltage	V_{RMOD}	R_{MOD} = 10 kΩ	0.54	0.60	0.66	V
RDEPTH Pin Voltage	V_{RDEPTH}	R_{DEPTH} = 10 kΩ	0.54	0.60	0.66	V
Modulation Frequency	f_{MOD}	RMOD = RDEPTH = 10 kΩ	22	25	28	kHz
Modulation Depth (Top Frequency)	$f_{DEPTH,max}$	RMOD = RDEPTH = 10 kΩ	2.05	2.3	2.55	MHz
Spread Spectrum Disable	R_{SSDIS}	RMOD or RDEPTH	 1.7		150	kΩ

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ERROR FLAG						
ERRB Output Low level	V_{ERRBL}	I_{ERRB} = 1 mA			0.4	V
THERMAL SHUTDOWN						
Thermal Warning Activation Temperature (Note 2)	T_{WARN}			150		°C
Thermal Shutdown Activation Temperature (Note 2)	T_{SD}		150		190	°C
Hysteresis (Note 2)	T_{HYS}		5		20	°C

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TYPICAL CHARACTERISTICS

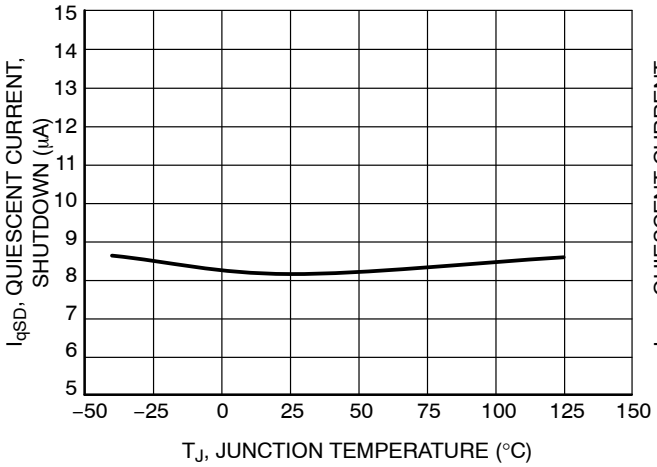


Figure 5. Quiescent Current (Shutdown) vs. Junction Temperature

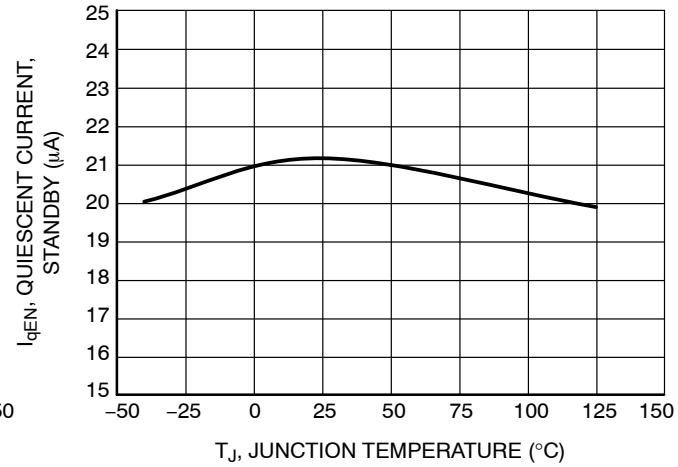


Figure 6. Quiescent Current (Standby) vs. Junction Temperature

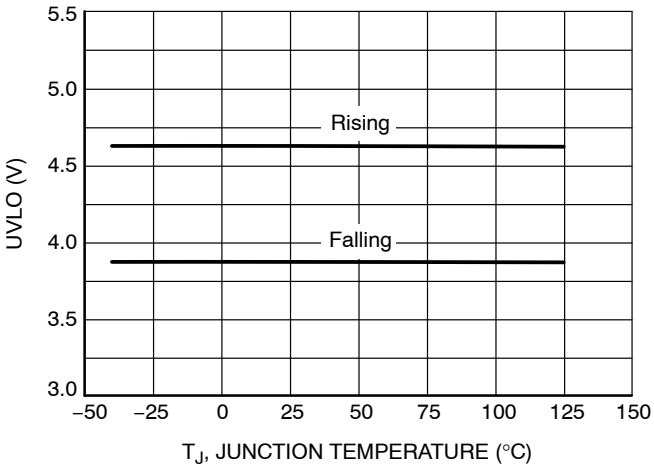


Figure 7. UVLO vs. Junction Temperature

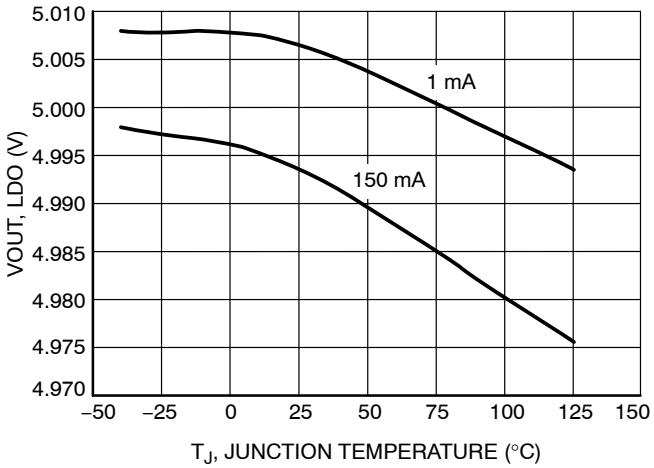


Figure 8. VOUT vs. Junction Temperature

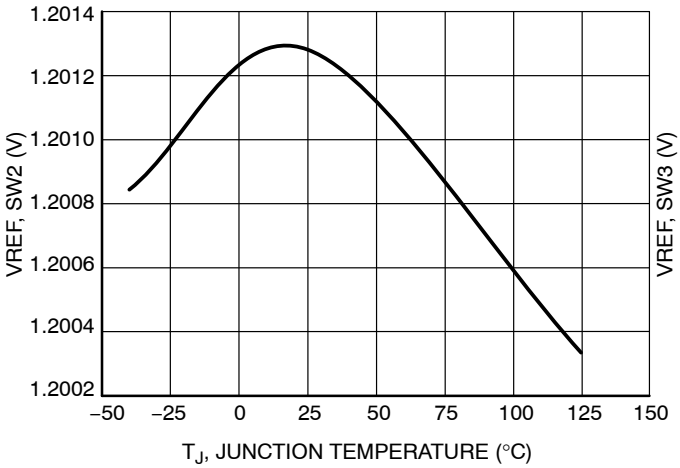


Figure 9. SW2 VREF vs. Junction Temperature

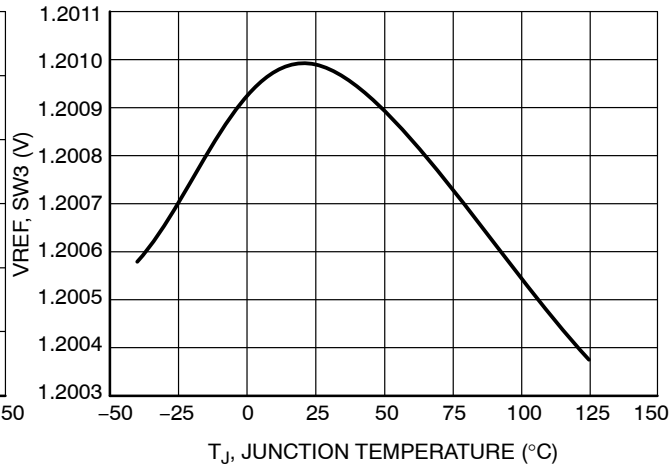


Figure 10. SW3 VREF vs. Junction Temperature

TYPICAL CHARACTERISTICS

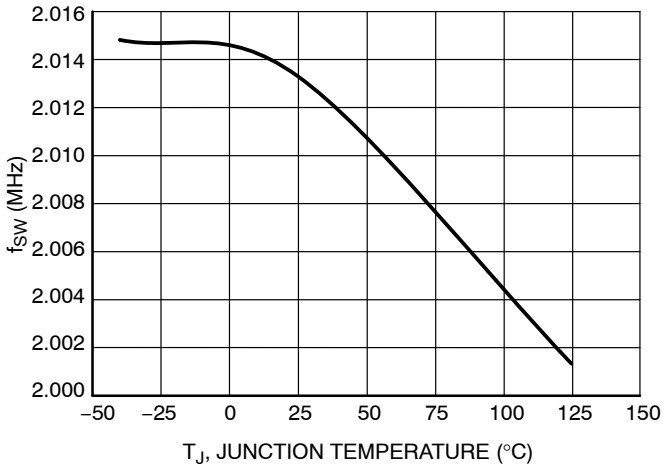


Figure 11. F_{SW} vs. Junction Temperature

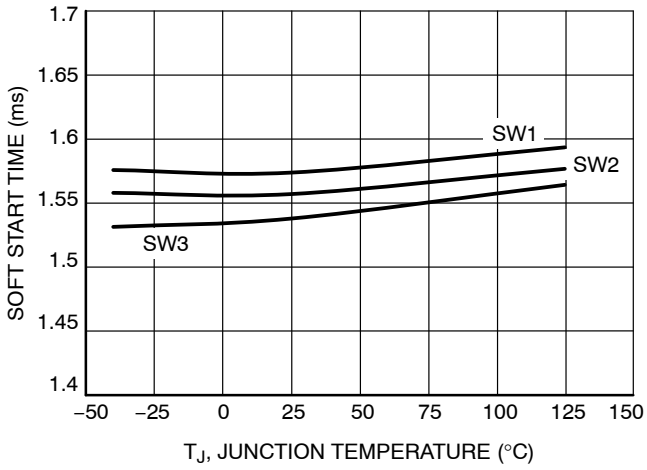


Figure 12. Soft Start Time vs. Junction Temperature

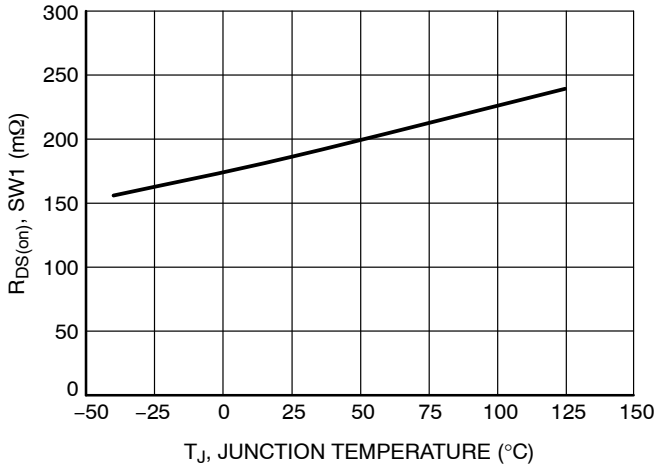


Figure 13. SW1 $R_{DS(on)}$ vs. Junction Temperature

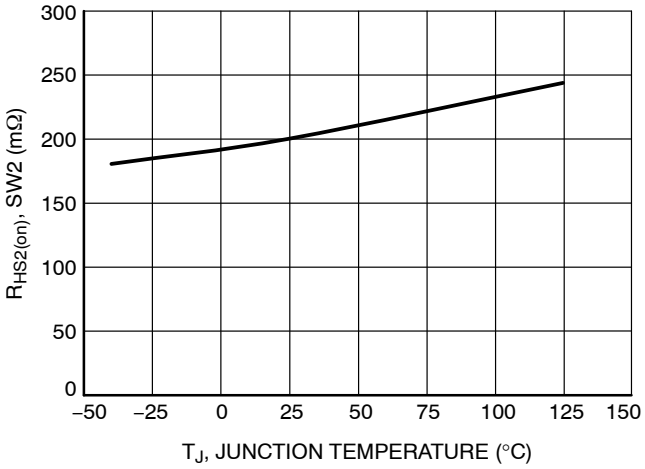


Figure 14. SW2 High Side $R_{DS(on)}$ vs. Junction Temperature

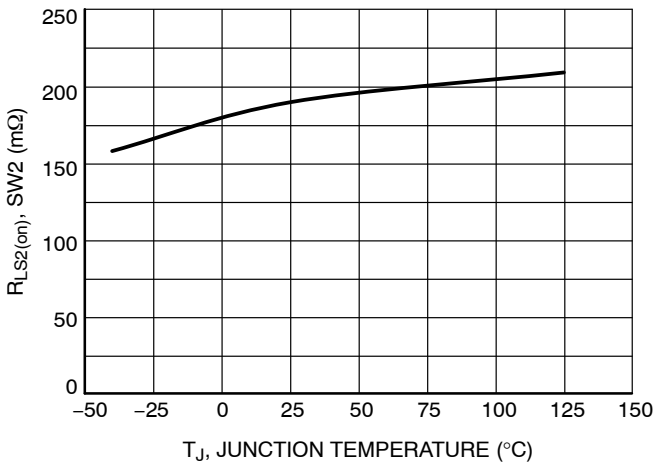


Figure 15. SW2 Low Side $R_{DS(on)}$ vs. Junction Temperature

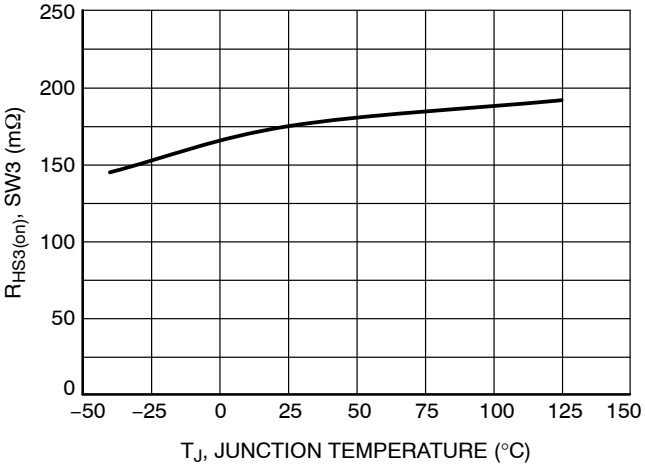


Figure 16. SW3 High Side $R_{DS(on)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

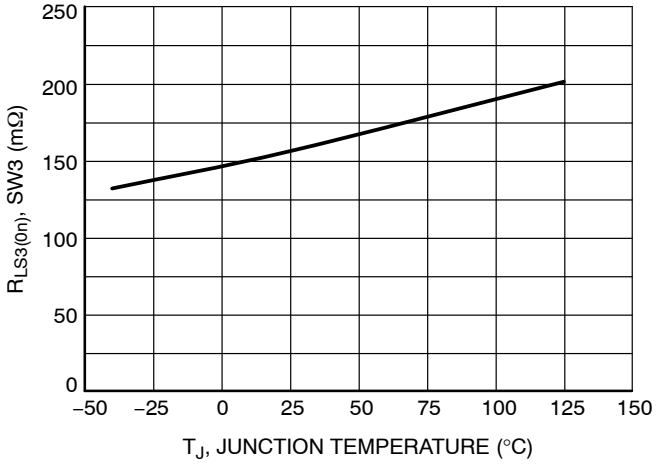


Figure 17. SW3 Low Side $R_{DS(on)}$ vs. Junction Temperature

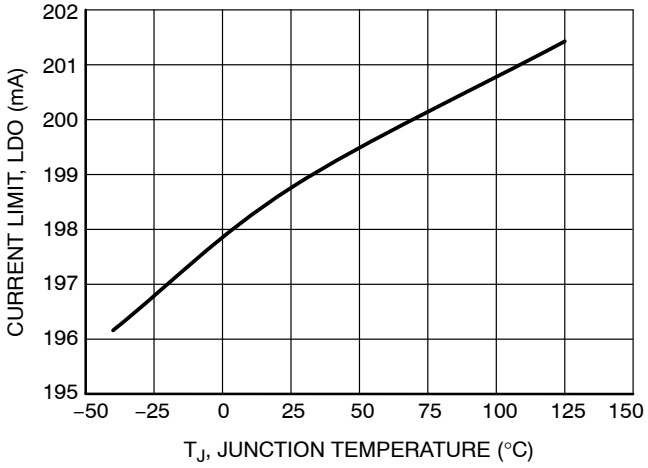


Figure 18. LDO Current Limit vs. Junction Temperature

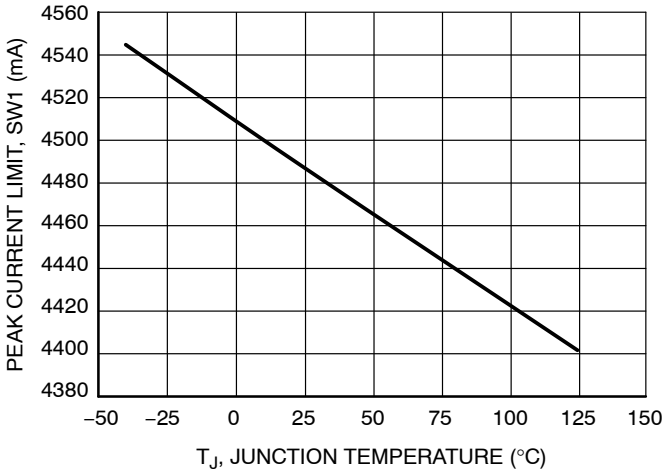


Figure 19. SW1 Peak Current Limit vs. Junction Temperature

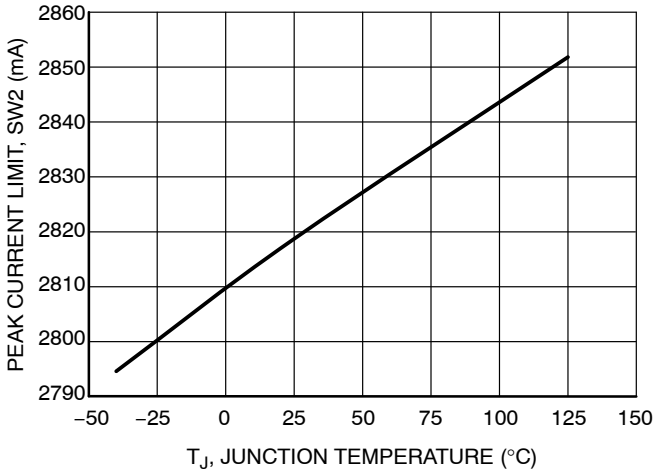


Figure 20. SW2 Peak Current Limit vs. Junction Temperature

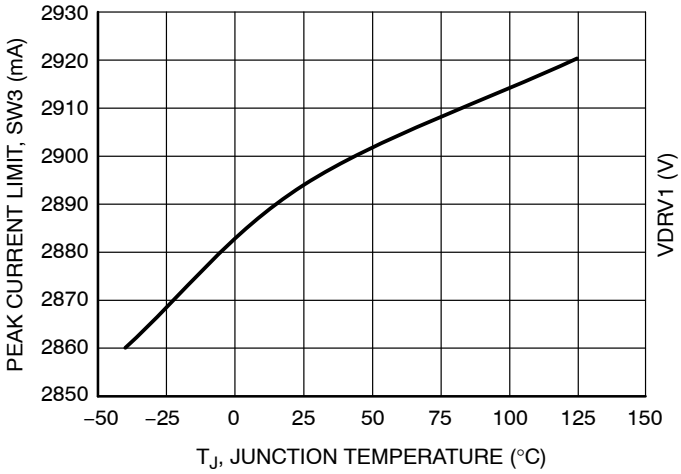


Figure 21. SW3 Peak Current Limit vs. Junction Temperature

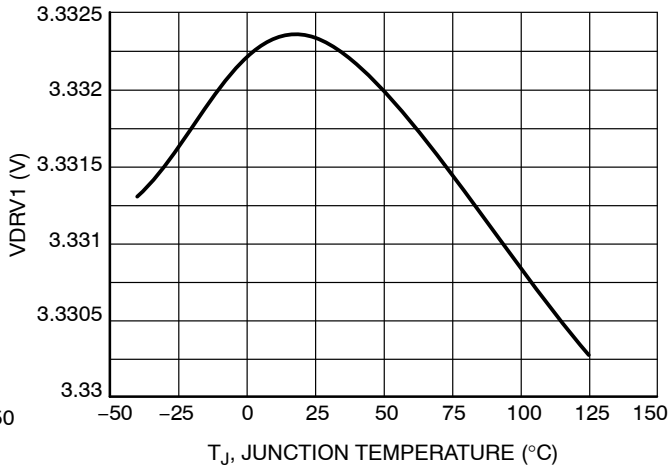


Figure 22. VDRV1 Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

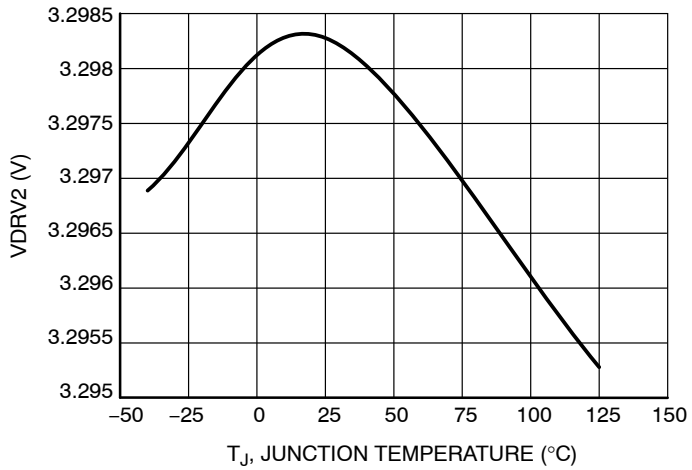


Figure 23. VDRV2 Voltage vs. Junction Temperature

APPLICATION INFORMATION

General Description

The NCV97311A consists of one 2 MHz battery−connected 2.5 A switcher (switcher 1) with a parallel low−Iq 150 mA LDO, and two low−voltage 2 MHz 1.5 A switchers (switchers 2 and 3).

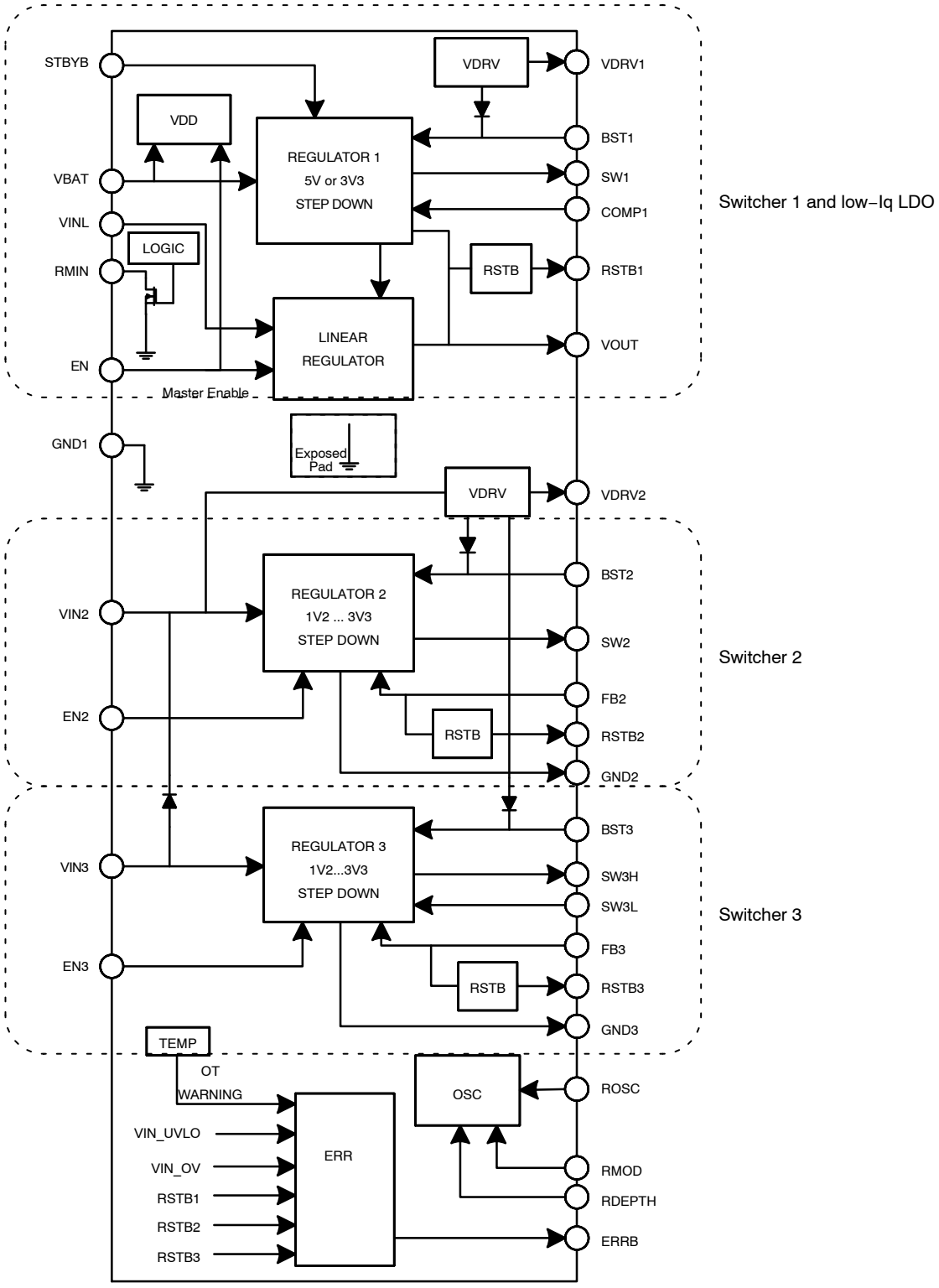


Figure 24. NCV97311A Block Schematic

COMMON BLOCKS

Input Voltage

The main supply for the part is taken from the VBAT pin, which much always be tied to a voltage source between 4.1 V and 37 V.

- Below 4.1 V an Undervoltage Lockout (UVLO) circuit inhibits all switching, resets the Soft−start circuits, and turns off the LDO.
- Above 40 V, an Overvoltage Shutdown circuit inhibits all switching and allows the NCV97311A to survive a 45 V load dump. Normal operation resumes when VBAT goes back down below 37 V.

Although the LDO has its own input pin VINL (that can also survive a 45 V load dump), it must always be connected to VBAT for proper operation.

Switcher 2 and switcher 3 each have a dedicated input pin, VIN2 and VIN3. VIN2 and VIN3 should be shorted together right at the pin because they share a common drive pin, VDRV2. Please note that VIN2 and VIN3 are strictly low voltage (up to 12 V when disabled and 9.5 V when switching) and there is no voltage sensing present.

It is recommended to connect VIN2 (and VIN3) to VOUT1, although a different rail could be used to supply switchers 2 and 3, as long as VBAT is powered and switcher 1 enabled (see Oscillator section for details).

Oscillator

All three switchers share the same oscillator, which defaults to 2.0 MHz and can be adjusted from 2.0 to 2.6 MHz using an external resistor (R_{OSC}) to ground. The range of ROSC value for this range of frequency adjustment is between 12.5 kΩ and 50 kΩ (see Figure 25). For resistor values below 10 kΩ, the frequency is safely clamped to 2.8 MHz.

Instead of a resistor, one can force a current out of the ROSC pin, between 20 μA (corresponding to 2 MHz) and 80 μA (corresponding to 2.5 MHz), typical.

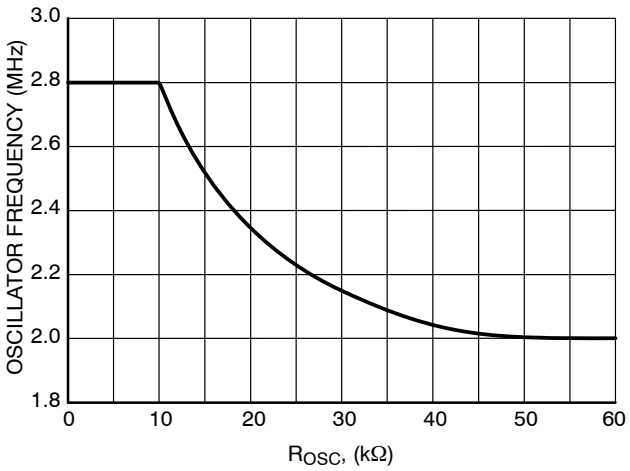


Figure 25. Oscillator Frequency vs. ROSC Value

Manually adjusting the oscillator frequency using the ROSC pin changes the switching frequency of all 3 switchers, since they share a common oscillator. When switcher 1 enters maximum duty cycle frequency foldback, though, switchers 2 and 3 remain at their nominal switching frequency. The foldback for switcher 1 takes place in logic outside of the oscillator. The same applies for both switcher 2 and switcher 3. When switcher 2, for example, enters maximum duty cycle frequency foldback, the other two switchers remain at their nominal switching frequency.

Spread Spectrum

In SMPS devices, switching translates to higher efficiency. Unfortunately, the switching leads to a much noisier EMI profile. We can greatly decrease some of the radiated emissions with some spread spectrum techniques. Spread spectrum is used to reduce the peak electromagnetic emissions of a switching regulator.

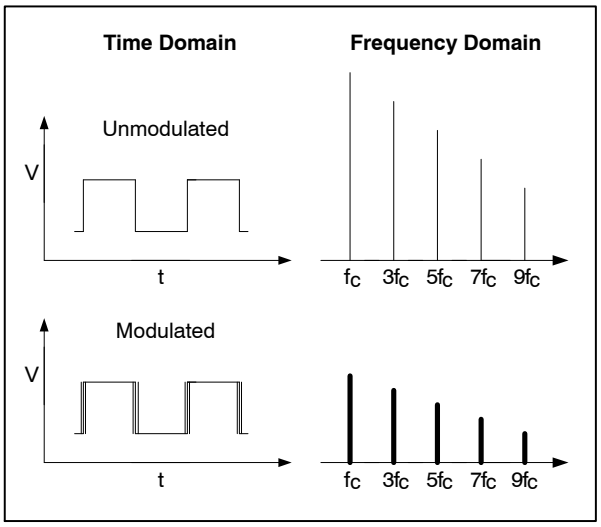


Figure 26.

The spread spectrum used in the NCV97311A is an “up−spread” technique, meaning the switching frequency is spread upward from the 2.0 MHz base frequency. For example, a 5% spread means that the switching frequency is swept (spread) from 2.0 MHz up to 2.1 MHz in a linear fashion – this is called the modulation depth. The rate at which this spread takes place is called the modulation frequency. For example, a 10 kHz modulation frequency means that the frequency is swept from 2.0 MHz to 2.1 MHz in 50 μs and then back down from 2.1 MHz to 2.0 MHz in 50 μs.

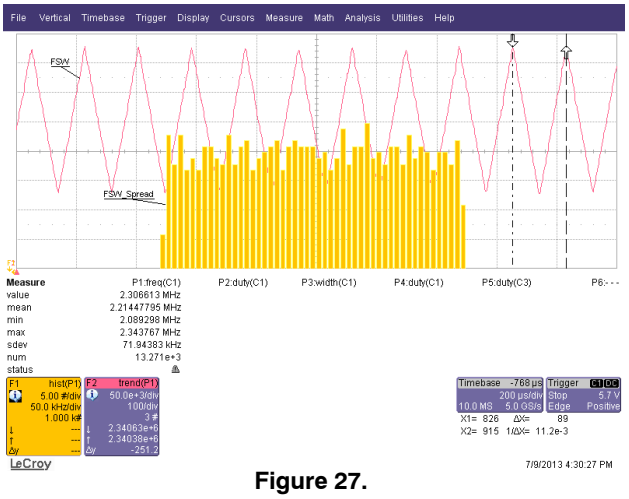


Figure 27.

The modulation depth and modulation frequency are each set by an external resistor to GND. The modulation frequency can be set from 5 kHz up to 50 kHz using a resistor from the RMOD pin to GND. The modulation depth can be set from 3% up to 30% of the nominal switching frequency using a resistor from the RDEPTH pin to GND. Please see the curves below for typical values:

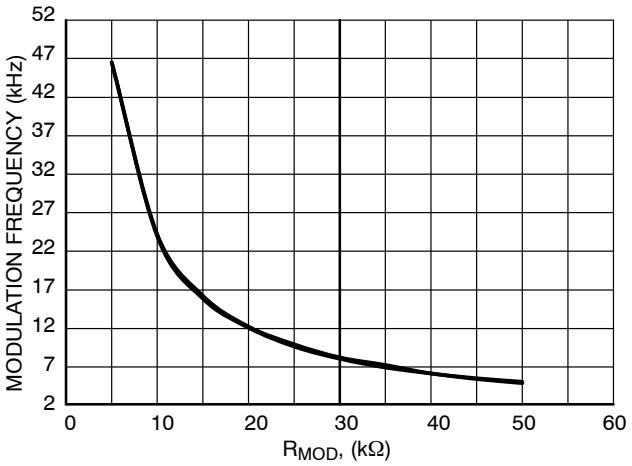


Figure 28. Modulation Frequency vs. RMOD Value

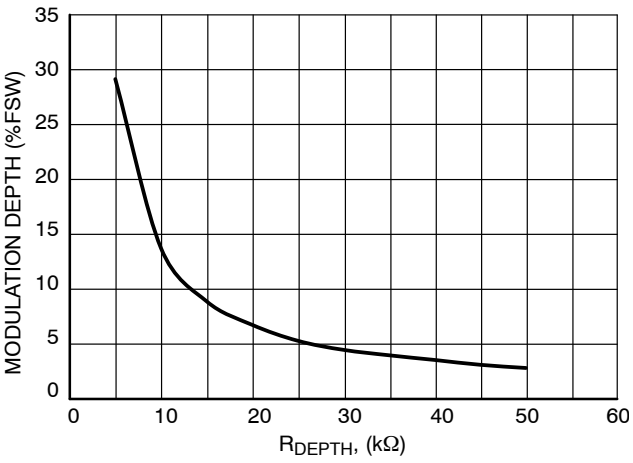


Figure 29. Modulation Depth vs. RDEPTH Value

Spread spectrum is automatically turned off when there is a short to GND or an open circuit on either the RMOD pin or the RDEPTH pin. Please be sure that the ROSC pin is an open circuit when using spread spectrum.

Master Enable

The NCV97311A can be completely disabled (shutdown mode) by connecting the EN pin to ground. As a result, all outputs are stopped and the internal current consumption drops below 10 µA.

The EN pin is designed to accept either a logic level signal or the battery voltage.

Reset

When the voltage on the OUTx pin drops below the reset threshold (92.5% typically for RSTB1, 93.5% typically for RSTB2 & RSTB3), the open−drain output RSTBx is pulled low. The RSTB1 pin is fully operational in Low−Iq mode. A pull−up resistor must be connected to RSTB1, typically from RSTB1 to V_{OUT1} (permanent supply voltage in low−Iq mode). The RSTB2 & RSTB3 pins are asserted (pulled low) when the associated switcher is disabled and when in Low−Iq mode (STBYB low).

Delay

Each of the RSTB signals can either be used as a reset with delay or a power good (no delay). The delay is determined by the current into the RSTBx pin, set by a resistor, shown in Figure 30.

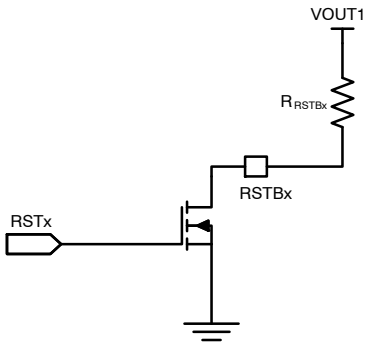


Figure 30. Reset Delay Time

Use the following equation to determine the ideal reset delay time using currents less than 1 mA:

$$t_{delay} = \frac{3000}{I_{RSTBx}} + 1.2 \qquad \text{(eq. 1)}$$

where:

t_{delay}: ideal reset delay time [ms]

I_{RSTBx}: current into the RSTBx pin [µA]

Using I_{RSTBx} = 2 mA removes the delay and allows the reset to act as a “power good” pin.

The RSTBx resistor is commonly tied to VOUT1. For a 5.0 V pull−up voltage, typical delay times can be achieved with the following resistor values:

R_{RSTBx} (kΩ)	t_{DLY} (ms)
2.5	0
5	4.4
10	7.3
20	13.0
30	18.8
50	31.5

For a 3.3 V pull−up voltage, typical delay times can be achieved with the following resistor values:

R_{RSTBx} (kΩ)	t_{DLY} (ms)
1.6	0
3.3	4.5
5	5.9
10	10.3
20	19.3
30	28.9

Minimum Dropout Voltage

When operating at low input voltages, two parameters play a major role in imposing a minimum voltage drop across the regulator: the minimum off time (that sets the maximum duty cycle) and the on−state resistance.

When operating in continuous conduction mode (CCM), the output voltage is equal to the input voltage multiplied by the duty ratio. Because each switcher needs a sufficient bootstrap voltage to operate, its duty cycle cannot be 100%: it needs a minimum off time ($t_{off,min}$) to periodically re−fuel the bootstrap capacitor, C_{BST}. This imposes a maximum duty ratio $D_{MAX}= 1 - t_{off,min} \cdot F_{SW(min)}$ with the switching frequency being folded back to $F_{SW(min)}$ = 500 kHz to keep regulating at the lowest input voltage possible. The drop due to the on−state resistance is simply the voltage drop across the switch at the given output current: $V_{SW,drop} = I_{OUT} \cdot R_{DS(on)}$. Which leads to the maximum output voltage in low Vin condition: $V_{OUT} = D_{MAX} \cdot V_{IN(min)} - V_{SW,drop}$

Error Flag

An open drain ERRB pin (active low) flags the status of several internal error detectors: VBAT undervoltage, VBAT overvoltage, thermal warning, switcher 1 reset, as well as the reset flags RSTB2 and RSTB3 if their respective switchers are enabled. Note that overvoltage is not flagged in Low−Iq standby mode.

When the master enable pin EN is forced low, the error flag is not active anymore.

Thermal Shutdown

A thermal shutdown circuit inhibits switching, resets the Soft−start circuits, and removes DRVx voltages if the internal temperature exceeds a safe level. Switching is automatically restored when the temperature returns to a safer level.

Inductor Selection

By default, a 4.7 μH inductor is recommended for the primary switching output. If you'd like to choose a different value, please follow the equation, below.

$$L = \frac{V_{out}\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{\delta I_r \cdot f_{sw} \cdot I_{out}}$$

where:

V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
δI_r: inductor current ripple [%]
f_{SW}: switching frequency [Hz]
I_{OUT}: dc output current [A]

Discontinuous Mode

In order to ensure continuous conduction mode, the ripple (half of the peak−to−peak ripple) needs to be less than the average current through the inductor. The limit can be found using the following equation for borderline conduction mode:

$$I_{BCM} = \frac{1}{2} \cdot \frac{\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{f_{sw}} \cdot \frac{V_{OUT}}{L}$$

where:

I_{BCM}: borderline conduction mode output current [A]
V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
f_{SW}: switching frequency [Hz]
L: inductor value [H]

Average output currents above I_{BCM} will operate in continuous mode while average output currents below I_{BCM} will operate in discontinuous mode.

SWITCHER 1

Output Voltage

The NCV97311A comes in a 5.0 V version and a 3.3 V version. The output of switcher 1, as well as the output of the low−Iq LDO, are fixed at 5.0 V and 3.3 V, respectively.

High Voltage Frequency Foldback

To limit the power lost in generating the drive voltage for the Power Switch, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{BAT} Frequency Foldback threshold V_{FL1U} (see Figure 31). Frequency reduction is automatically terminated when the input voltage drops back below the V_{BAT} Frequency Foldback threshold V_{FL1D}.

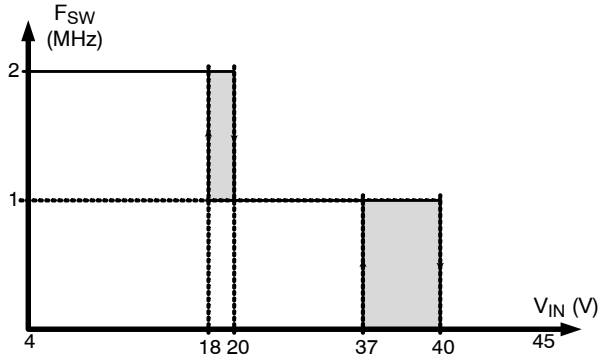


Figure 31. Switcher 1 Switching Frequency Reduction at High Input Voltage

Low−IQ Mode

The NCV97311A can be put in a low−Iq regulating mode by connecting the STBYB pin to ground. As a result, Switcher 1 turns off and the low−Iq LDO turns on, maintaining regulation on VOUT (up to 150 mA). In this mode the VOUT reset monitor is still active (RSTB1 pin), as well as the under−voltage sensing on VBAT and the thermal sensing, and they're all flagged on the ERRB pin. Switchers 2 and 3 are automatically disabled, with their respective reset pins pulled low.

Upon enabling standard switching mode again (bringing STBYB high), voltage is established at the DRV1 pin, followed by a pre−charge of the bootstrap capacitor before switcher 1 starts switching. There is no soft−start unless VOUT is below the reset threshold.

It is recommended to wait at least 200 μs after toggling STBYB before applying a load higher than 150 mA.

The STBYB pin is designed to accept either a logic level signal or the battery voltage.

Soft−Start

Upon being enabled or released from a fault condition, and after the DRV1 voltage is established, a soft−start circuit ramps the switching regulator error amplifier reference voltage to the final value. During soft−start, the average switching frequency is lower than its normal mode value (typically 2 MHz) until the output voltage approaches regulation. There is no soft−start if the output is already above the reset threshold.

Error Amplifier

The error amplifier is a transconductance type amplifier. The output voltage of the error amplifier controls the peak inductor current at which the power switch shuts off. The Current Mode control method employed allows the use of a simple, type II compensation to optimize the dynamic response according to system requirements.

The compensation components must be connected between the output of the error amplifier and the electrical ground (between pins COMP1 and GND1). For most applications, the following compensation circuitry is recommended:

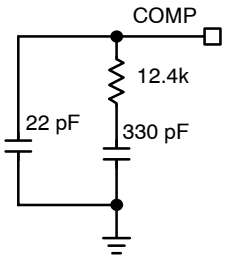


Figure 32. Recommended Compensation for Primary Switcher

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50% (sub−harmonics oscillations). The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub−harmonic oscillations. For both 3.3 V and 5.0 V versions, the recommended inductor value is either 2.2 μH or 4.7 μH.

To determine the minimum inductor required to avoid sub−harmonic oscillations, please refer to the following equation:

$$L_{min} = \frac{V_{OUT}}{(2 * S_{ramp})}$$

where:

L_{min}: minimum inductor required to avoid sub-harmonic oscillations [μH]

V_{out}: output voltage [V]

S_{ramp}: internal slope compensation [A/μs]

Short Circuit Frequency Foldback

During severe output overloads or short circuits, switcher 1 automatically reduces its switching frequency. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed. If the current is still too high after the switching frequency folds back to 500 kHz (250 kHz for V_{IN} > 20 V), the regulator enters hiccup mode (32 kHz) that further reduces the dissipated power.

Bootstrap

At the DRV1 pin an internal regulator provides a ground−referenced voltage to an external capacitor (C_{DRV1}), to allow fast recharge of the external bootstrap capacitor (C_{BST1}) used to supply power to the power switch gate driver. If the voltage at the DRV1 pin goes below the DRV UVLO Threshold V_{DRVSTP}, switching is inhibited and the Soft−start circuit is reset, until the DRV1 pin voltage goes back up above V_{DRVSTT}.

In order for the bootstrap capacitor to stay charged, the Switch node needs to be pulled down to ground regularly. In very light load condition, when switcher 1 skips switching cycles to keep the output voltage in regulation, the bootstrap voltage could collapse and the regulator stop switching. To prevent this, an internal minimum load is connected on VOUT to operate correctly in all cases (it is disconnected in low Iq mode, when the STBYB pin is low).

A fast−charge circuit ensures the bootstrap capacitor is always charged prior to starting the switcher after it has been enabled.

Minimum Load

For a 3.3 V output, an external minimum load is not required. The internal minimum load ensures stability under low−battery conditions. For a 5.0 V output, an external minimum load is required when not using a pre−boost that maintains a minimum 6.8 V on the input. The following chart describes the ways in which the RMIN pin is recommended to be used:

VOUT1	Pre−boost?	VBAT Condition	RMIN Resistor	Configuration
5.0 V	No	VBAT < 6.8 V	Populated	Resistor connected from VOUT1 to RMIN pin
5.0 V	Yes	VBAT set to 6.8 V from pre− boost	Not Populated	RMIN not connected
3.3 V	No	VBAT < 6.8 V	Not Populated	RMIN not connected
3.3 V	Yes	VBAT set to 6.8 V from pre− boost	Not Populated	RMIN not connected

The RMIN resistance (from VOUT1 to RMIN) should be between 27 and 35 Ω. When using an external minimum load, 3 x 100 Ω, ¼ W resistors are recommended to be placed in parallel from VOUT1 to the RMIN pin of the IC.

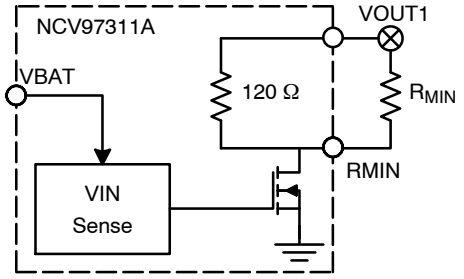


Figure 33. Internal Control for Minimum Load Circuit

Current Limiting

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 34 shows − for a 4.7 μH inductor − how the variation of inductor peak current with input voltage affects the maximum DC current switcher 1 can deliver to a load. Figure 35 shows the same for 2.2 μH inductor.

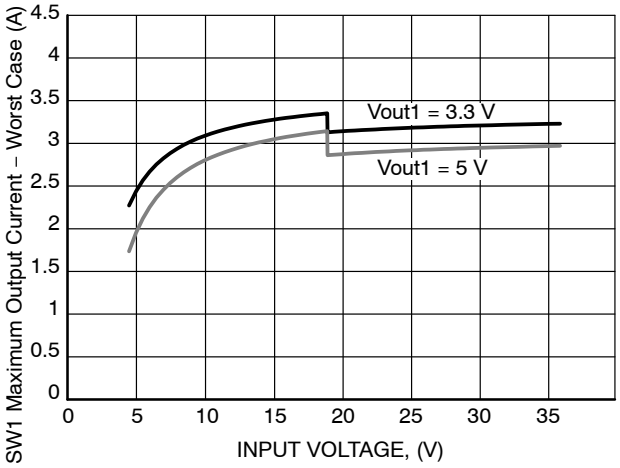


Figure 34. Switcher 1 Load Current Capability with a 4.7 μH Inductor

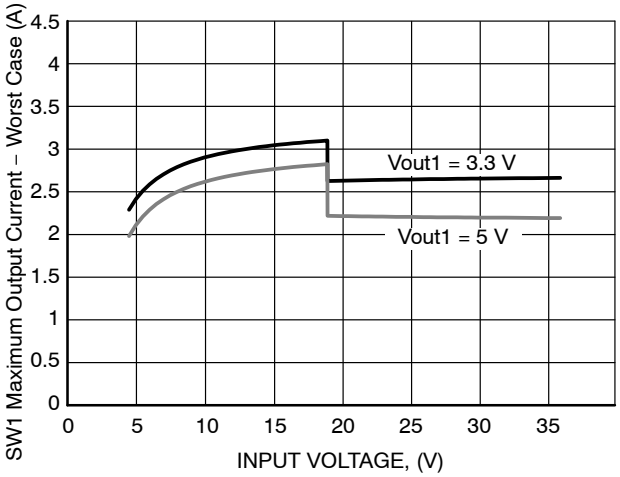


Figure 35. Switcher 1 Load Current Capability with a 2.2 μH Inductor

SWITCHERS 2 & 3

Enable

When a dc logic high (CMOS/TTL compatible) voltage is applied to the EN2 or EN3 pin and the STBYB pin is high Switcher 2 or Switcher 3, respectively, are allowed to operate. Switcher 1 soft start needs to complete before Switcher 2 or Switcher 3 is allowed to turn on. A dc logic low on EN2 or EN3 shuts off the respective regulators.

Soft−Start

Upon being enabled or released from a fault condition, voltage is first established on the VDRV2 pin (for the first of switcher 2 or 3 to be enabled). Then a soft−start circuit ramps the switching regulator error amplifier reference voltage to the final value, for a duration t_{SS} independent of the switching frequency (1.4 ms typically).

The low−side switch is always turned on first to ensure a proper charge of the bootstrap capacitor.

Error Amplifier

The error amplifier is a voltage type amplifier with fixed internal compensation, optimized for the range of input and output voltage combinations. The output voltage of the error amplifier controls the peak inductor current at which the power shuts off (current−mode operation).

Because the compensation is internally fixed, the value of the upper feedback resistor (in series between the output and the feedback pin) must be 10 kΩ to ensure stability, including in the case of a 1.2 V output, when no lower feedback resistor is used. In addition, it is recommended to use 1 or 2 10 μF capacitors on the output, depending on your ripple requirement; and an inductor value between 1 μH and 4.7 μH (see slope compensation section).

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50% (sub−harmonic oscillations). The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, dependent on the output voltage, in order to avoid sub−harmonic oscillations.

- For a 5 V output, the recommended inductor value is 4.7 μH.
- For 3.3 V or 2.5 V output, the recommended inductor value is 2.2 μH.
- For 1.2 V or 1.5 V output, the recommended inductor value is 1.0 μH.

Short Circuit Frequency Foldback

During severe output overloads or short circuits, switchers 2 and 3 (independently) automatically enter an auto−recovery burst mode in order to self−protect. When a short−circuit is detected, the switcher disables its output and remains off for the hiccup time and then goes through the power-on reset procedure. If the short has been removed then the output re−enables and operates normally; if, however, the short is still present the cycle begins again. The hiccup mode is continuous until the short is removed.

Current Limiting

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 36 shows how the variation of inductor peak current with input voltage affects the maximum DC current switcher 2 or 3 can deliver to a load.

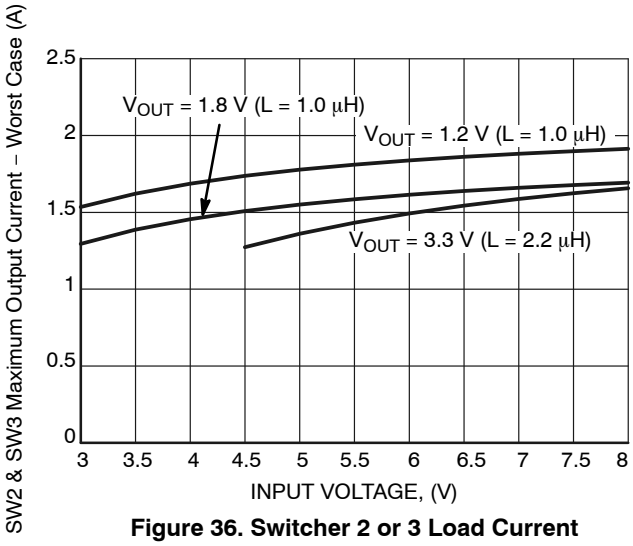


Figure 36. Switcher 2 or 3 Load Current Capability vs. Input Voltage

Output Voltage Selection

The voltage outputs for switcher 2 and switcher 3 are adjustable and can be set with a resistor divider. The FB reference for both switchers is 1.2 V.

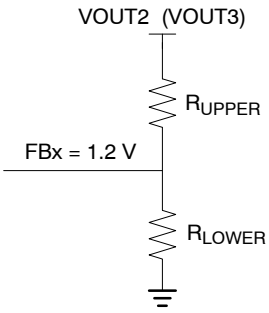


Figure 37. Output Voltage Selection with Feedback Divider

The upper resistor is set to 10 kΩ and is part of the feedback loop. To maintain stability over all conditions, it is recommended to change the only the lower feedback resistor to set the output voltage. Use the following equation:

$$R_{LOWER} = R_{UPPER}\frac{V_{FB}}{V_{OUT} - V_{FB}}$$

Some common setups are listed below:

Desired Output (V)	VREF (V)	R_{UPPER} (kΩ, 1%)	R_{LOWER} (kΩ, 1%)
1.2	1.2	10.0	NP
1.5	1.2	10.0	40.0
1.8	1.2	10.0	20.0
2.5	1.2	10.0	9.31
3.3	1.2	10.0	5.76

Noise Performance for Heavy Load

For heavy load conditions (> 1 A) on the downstream switching outputs, a snubber circuit is recommended for improved noise performance. The following circuit can be used for all output voltage combinations:

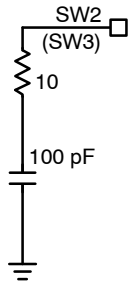


Figure 38. RC Snubber Circuit for Noise Performance at Heavy Loads

ORDERING INFORMATION

Device	Package	Shipping†
NCV97311MW50AR2G (5.0 V)	QFN32 (Pb−Free)	5000 / Tape & Reel
NCV97311MW33AR2G (3.3 V)		

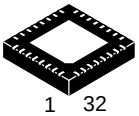
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

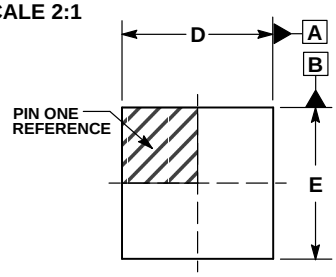
ON Semiconductor®

QFNW32 5x5, 0.5P
CASE 484AB
ISSUE D

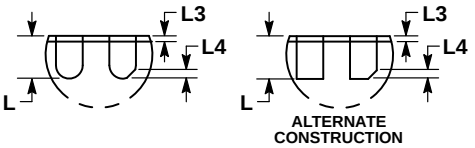
DATE 07 SEP 2018



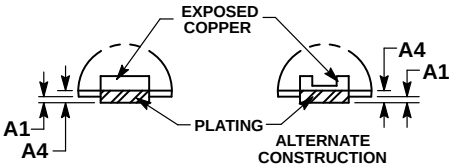
SCALE 2:1



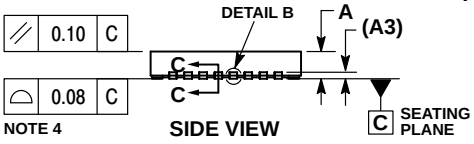
TOP VIEW



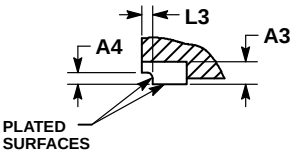
DETAIL A



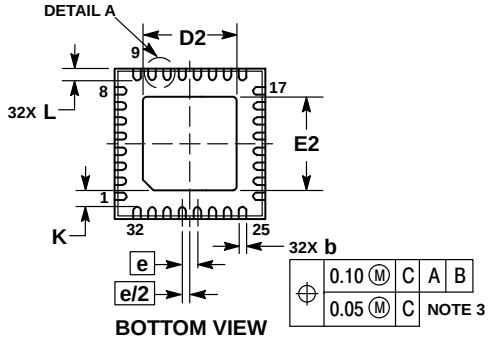
DETAIL B



SIDE VIEW



SECTION C−C

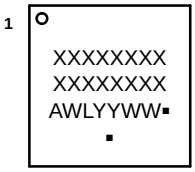


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	−−−	−−−	0.05
A3		0.20 REF	
A4	0.10	−−−	−−−
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.00	3.10	3.20
E	4.90	5.00	5.10
E2	3.00	3.10	3.20
e		0.50 BSC	
K	0.35	−−−	−−−
L	0.30	0.40	0.50
L3	−−−	−−−	0.10
L4		0.08 REF	

GENERIC MARKING DIAGRAM*

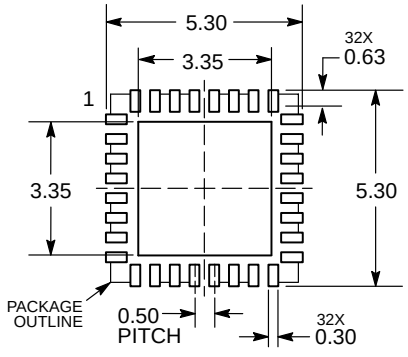


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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