NCV8851-1

Automotive Grade Synchronous Buck Controller

The NCV8851−1 is an adjustable output, synchronous buck controller, which drives dual N−channel MOSFETs, ideal for high power applications. Average current mode control is employed for very fast transient response and tight regulation over wide input voltage and output load ranges. The IC incorporates an internal fixed 6.0 V low−dropout linear regulator (LDO), which supplies charge to the switch mode power supply's (SMPS) bottom gate driver, limiting the power lost to excess gate drive. The IC is designed for operation over a wide input voltage range (4.5 V to 40 V) and is capable of 10 to 1 voltage conversion at 500 kHz.

Additional controller features include undervoltage lockout, internal soft−start, low quiescent current sleep mode, programmable frequency, SYNC function, average current limiting, cycle−by−cycle overcurrent protection and thermal shutdown.

Features

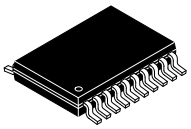
- Average Current Mode Control
- 0.8 V ±2% Reference Voltage
- Wide Input Voltage Range of 4.5 V to 40 V
- Operates through Load Dump Conditions
- 6.0 V Low−dropout Linear Regulator (LDO)
- Input UVLO (Undervoltage Lockout)
- Internal Soft−start
- 1.0 μA Maximum Quiescent Current in Sleep Mode
- Adaptive Non−overlap Circuitry
- 180 ns Minimum High−side Gate Off−time
- Programmable Fixed Frequency – 170 kHz to 500 kHz
- External Clock Synchronization up to 600 kHz
- Average Current Limiting (ACL)
- Cycle−by−Cycle Overcurrent Protection (OCP)
- Thermal Shutdown (TSD)
- This is a Pb−Free Device

Applications

- Automotive Systems Requiring High Current
- Pre−regulated Supply for Low−voltage SMPSs and LDOs

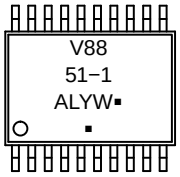
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TSSOP−20
SUFFIX DB
CASE 948E

MARKING DIAGRAM



V8851−1 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV8851−1DBR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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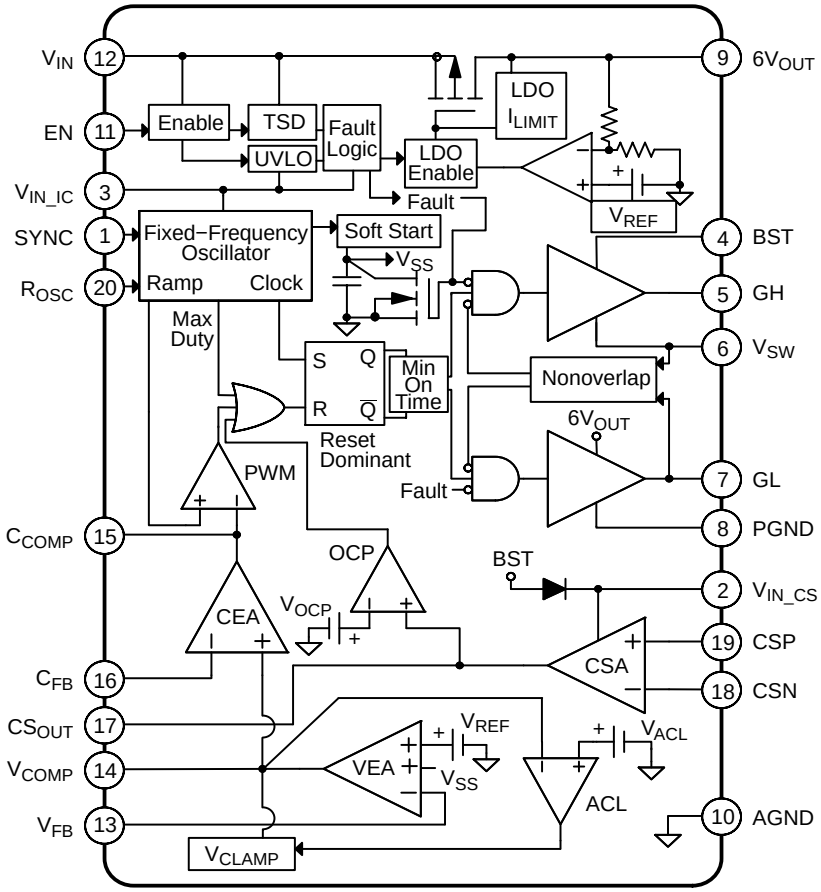


Figure 1. Functional Block Diagram

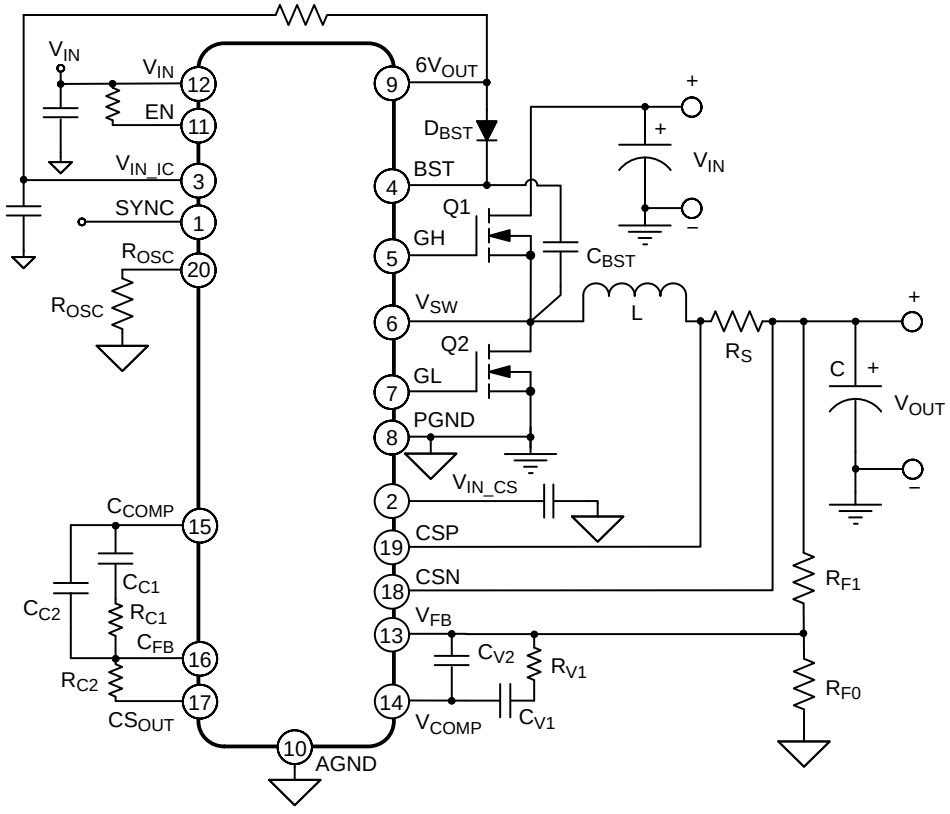


Figure 2. Application Schematic

Note: This part is recommended for synchronous use only.

PACKAGE PIN DESCRIPTIONS − 20 Lead TSSOP

Package Pin#	Pin Symbol	Function
1	SYNC	External clock synchronization input.
2	V_{IN_CS}	Supply input for the internal current sense amplifier.
3	V_{IN_IC}	Supply input for internal logic and analog circuitry.
4	BST	Supply input for the floating top gate driver. An external diode, D_{BST}, from $6V_{OUT}$ and a 0.1 μF to 1 μF capacitor, C_{BST}, to V_{SW} forms a boost circuit.
5	GH	Gate driver output for the external high−side NMOS FET.
6	V_{SW}	Switch−node. This pin connects to the source of the high−side MOSFET and drain of the low−side MOSFET. This pin serves as the switch output to the inductor.
7	GL	Gate driver output for the external low−side NMOS FET.
8	PGND	Power Ground. Ground reference for the high−current path including the NMOS FETs and output capacitor.
9	$6V_{OUT}$	Output of internal fixed 6.0 V LDO.
10	AGND	Analog Ground. Ground reference for the internal logic and analog circuitry as well as R_{OSC} and the compensators.
11	EN	Enable input. When disabled, the LDO, internal logic and analog circuitry and gate drivers enter sleep mode, drawing under 1 μA.
12	V_{IN}	Supply input for the SMPS.
13	V_{FB}	SMPS's voltage feedback. Inverting input to the voltage error amplifier. Connect to V_{OUT} through a resistive divider.
14	V_{COMP}	SMPS's voltage error amplifier output and non−inverting input to the current error amplifier.
15	C_{COMP}	SMPS's current error amplifier output and inverting input to the PWM comparator.
16	C_{FB}	SMPS's current feedback. Inverting input to the current error amplifier.
17	CS_{OUT}	Single−ended output of the differential current sense amplifier. Connect to C_{FB} through a resistor. Non−inverting input to the cycle−by−cycle overcurrent comparator.
18	CSN	Differential current sense amplifier inverting input.
19	CSP	Differential current sense amplifier non−inverting input.
20	R_{OSC}	Oscillator's frequency adjust pin. Resistor to ground sets the oscillator frequency.

MAXIMUM RATINGS (Voltages are with respect to AGND unless otherwise indicated.)

Rating	Value	Unit
Dc Supply Voltage (V_{IN}) Peak Transient Voltage (Load Dump)	−0.3 to 40 45	V
Dc Supply Voltage (V_{IN_CS})	46	V
Dc Supply Voltage (V_{IN_IC})	6.5	V
Pin Voltage (V_{SW}) $t \leq 50$ ns	−0.7 to 40.7 −2	V
Pin Voltage (BST, GH)	46 wrt PGND 7 wrt V_{SW}	V
Pin Voltage (GL)	−0.3 to 7 wrt PGND	V
Pin Voltage (EN)	−0.3 to 40	V
Pin Voltage (CSP, CSN)	−0.3 to 10	V
Pin Voltage (V_{FB}, V_{COMP}, CS_{OUT}, C_{FB}, C_{COMP}, SYNC, R_{OSC}, $6V_{OUT}$)	−0.3 to 7	V
Pin Voltage (PGND)	−0.3 to 0.3	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Lead−free 60 to 150 seconds at 217°C	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ATTRIBUTES

Characteristic	Value
ESD Capability	
Human Body Model (Boost, V_{IN_CS})	≥ 1.0 kV
Human Body Model (All Others)	≥ 1.5 kV
Machine Model	≥ 200 V
Charge Device Model	≥ 1.0 kV
Package Thermal Resistance	
Junction–to–Ambient, $R_{\theta JA}$ (Note 1)	156°C/W
Junction–to–Ambient, $R_{\theta JA}$ (Note 2)	108°C/W

1. 50 mm^2, 1.0 oz copper on FR4 board.
2. 500 mm^2, 1.0 oz copper on FR4 board.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 4.5 V < V_{IN} < 40 V, 4.5 V < BST < 46 V, R_{OSC} = 51.1 kΩ, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
GENERAL					
Quiescent Current (I_{VIN} + I_{VIN_CS} + I_{BST})	V_{IN} = 13.2 V, EN = 0 V, Sleep Mode −40°C < T_A < 125°C	−	−	1	μA
	V_{IN} = 13.2 V, V_{FB} = 1 V EN = 5 V, No Switching	−	2.0	3.0	mA
	V_{IN} = 13.2 V, V_{FB} = 0 V EN = 5 V, Switching	−	3.2	5.0	mA
LDO Current	V_{IN} = 13.2 V, V_{FB} = 0 V, EN = 5 V Switching, 3.3 nF on GH and GL	−	10	20	mA
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
Thermal Shutdown Hysteresis	Guaranteed by Design	−	10	20	°C
Undervoltage Lockout (V_{IN_IC})	V_{IN_IC} increasing	4.1	4.3	4.5	V
Undervoltage Lockout Hysteresis		50	125	200	mV
SWITCHING REGULATOR					
Reference Voltage		0.784	0.8	0.816	V
Minimum GH Off Time		110	180	250	ns
Minimum GH Pulse Width	Static Operating	−	140	200	ns
OSCILLATOR					
Switching Frequency	R_{OSC} = 51.1 kΩ R_{OSC} = 23.2 kΩ R_{OSC} = 16.2 kΩ	153 306 425	170 360 500	187 414 575	kHz kHz kHz
Ramp Voltage Amplitude		0.9	1.1	1.3	V
VOLTAGE ERROR AMPLIFIER					
DC Gain	Guaranteed by Design	70	73	−	dB
Gain−Bandwidth Product	Guaranteed by Design	8.0	10	−	MHz
Charge Currents	Source, V_{COMP} = 0 V	2	4	−	mA
	Sink, V_{COMP} = 1.75 V	1.3	3	−	mA
FB Bias Current	Guaranteed by Design	−	0.1	1.0	μA
CURRENT SENSE AMPLIFIER					
Common−Mode Range		0	−	10.0	V
Amplifier Gain	0 ≤ (CSP−CSN) ≤ 100 mV 0 V ≤ CSN ≤ 10.0 V	−	1	−	V/V

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 4.5 V < V_{IN} < 40 V, 4.5 V < BST < 46 V, R_{OSC} = 51.1 kΩ, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
CURRENT ERROR AMPLIFIER					
DC Gain	Guaranteed by Design	70	73	−	dB
Gain−Bandwidth Product	Guaranteed by Design	8.0	10	−	MHz
Charge Currents	Source, C_{COMP} = 1.75 V	2	4	−	mA
	Sink, C_{COMP} = 1.75 V	1.3	3	−	mA
FB Bias Current	Guaranteed by Design	−	0.1	1.0	μA
Clamping Voltage		2.7	3.5	−	V
CURRENT LIMIT					
Average Current Limit Threshold	1.2 V ≤ CSN ≤ 10.0 V	80	100	125	mV
Cycle−by−Cycle Current Limit Threshold Voltage		115	165	215	mV
Cycle−by−Cycle Current Limit Response Time	Guaranteed by Design	−	200	−	ns
Cycle−by−Cycle and Average Current Limit Threshold Difference		20	−	−	mV
SYNC					
SYNC Frequency Range		F_{SW}	−	600	kHz
SYNC Pin Bias Current	V_{SYNC} = 0 V V_{SYNC} = 5.0 V	− −	0.1 10	0.2 20	μA
SYNC Threshold Voltage	Logic Low Logic High	− 2.0	− −	0.8 −	V
6.0 V LDO					
Output Voltage	I_{OUT} = 20 mA	5.8	6.0	6.2	V
Dropout Voltage	I_{OUT} = 20 mA	−	−	200	mV
Current Limit		30	75	120	mA
GATE DRIVERS					
GH Sink Current	V_{GH} = 2 V, V_{IN_IC} = 6 V, Guaranteed by Design	−	1.5	−	A
GH Source Current	V_{GH} = 4 V, V_{IN_IC} = 6 V, Guaranteed by Design	−	1.5	−	A
GL Sink Current	V_{IN_IC} = 6 V V_{GL} = 1.0 V Guaranteed by Design	−	1.5	−	A
GL Source Current		−	1.5	−	A
GH to GL Delay	V_{IN} = 13.2 V	−	40	70	ns
GL to GH Delay	V_{IN} = 13.2 V	−	40	70	ns
SOFT START					
Time	F_{SW} = 170 kHz	−	14	−	ms
ENABLE (EN)					
Input Threshold	Logic Low Logic High	− 2.0	− −	0.8 −	V
Input Current	EN = 2.0 V	−	3.0	10	μA
Minimum Disable Time		−	−	20	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_A = +25°C, V_{IN} = 13.2 V, R_{OSC} = 51.1 kΩ, unless otherwise noted)

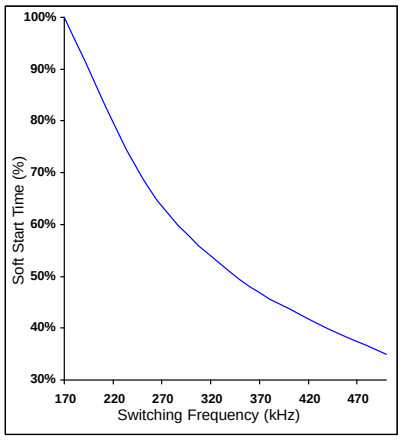


Figure 3. Soft−start Time vs. Frequency

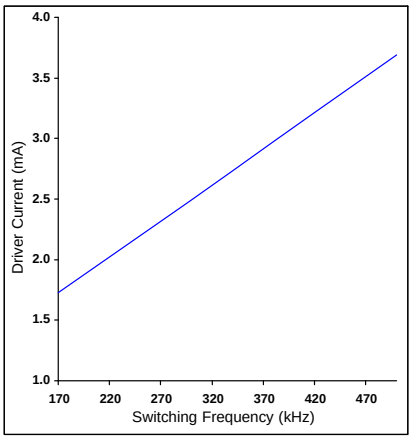


Figure 4. Driver Quiescent Current vs. Frequency

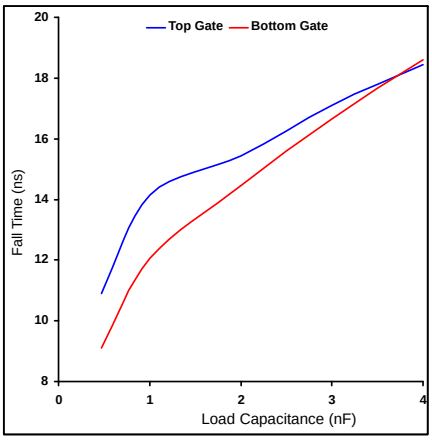


Figure 5. Driver Fall Time vs. Load Capacitance

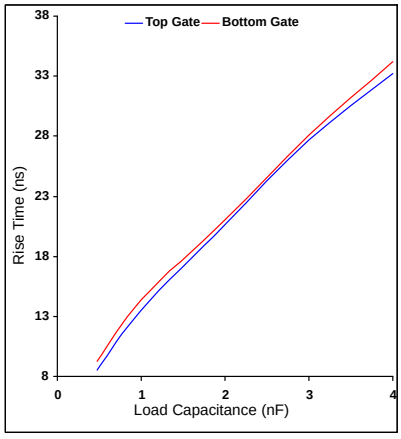


Figure 6. Driver Rise Time vs. Load Capacitance

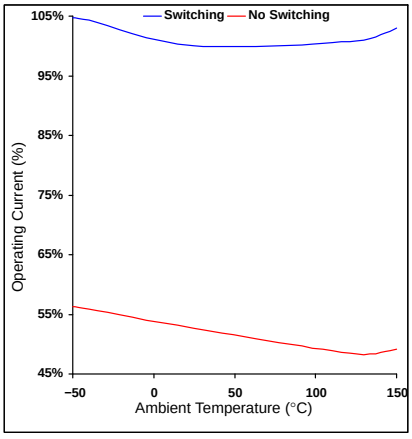


Figure 7. Operating Quiescent Current vs. Temperature

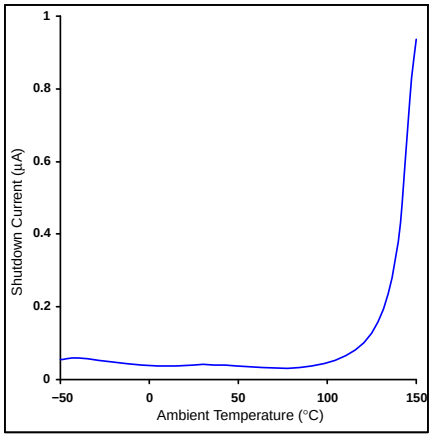


Figure 8. Sleep Mode Quiescent Current vs. Temperature

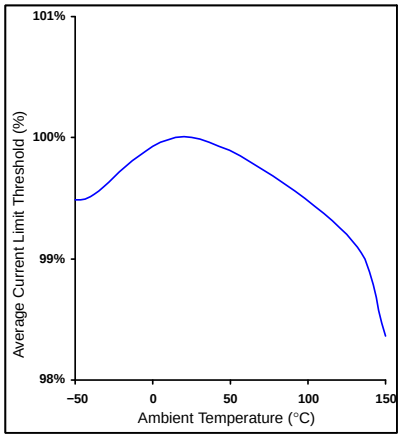


Figure 9. Average Current−Limit Threshold vs. Temperature

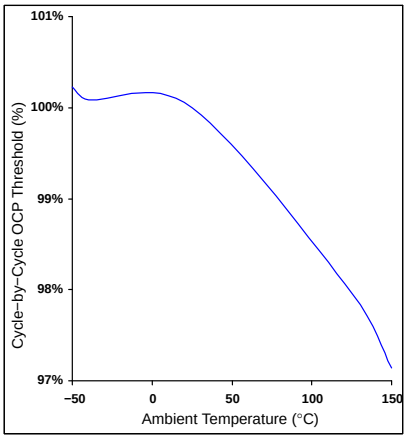


Figure 10. Cycle−by−Cycle Overcurrent Protection Threshold vs. Temperature

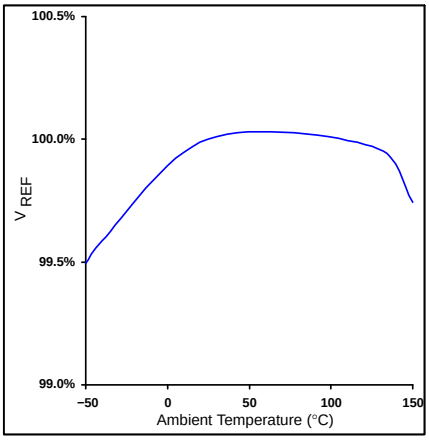


Figure 11. V_{REF} vs. Temperature

TYPICAL CHARACTERISTICS

(T_A = +25°C, V_{IN} = 13.2 V, R_{OSC} = 51.1 kΩ, unless otherwise noted)

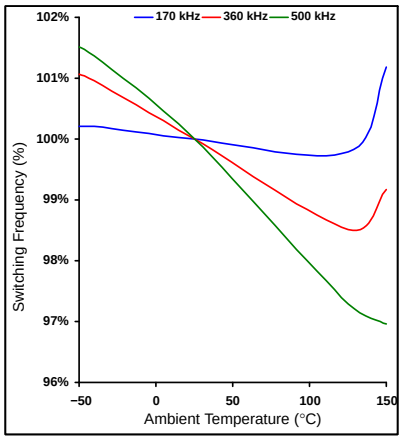


Figure 12. Oscillator Frequency vs. Temperature

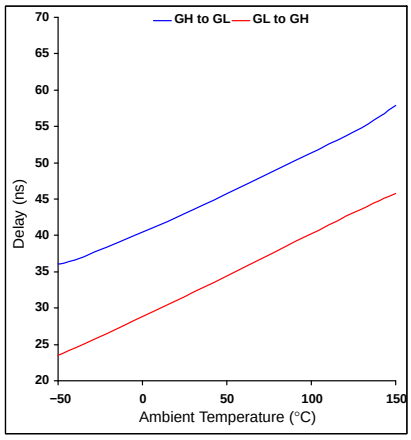


Figure 13. Non−Overlap Delay vs. Temperature

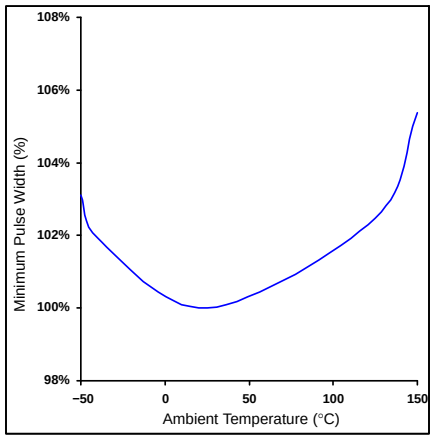


Figure 14. GH Minimum Pulse Width vs. Temperature

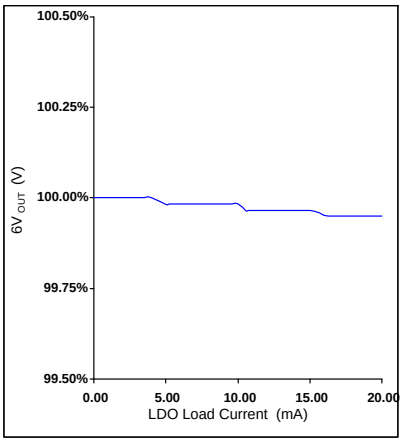


Figure 15. LDO Load Regulation

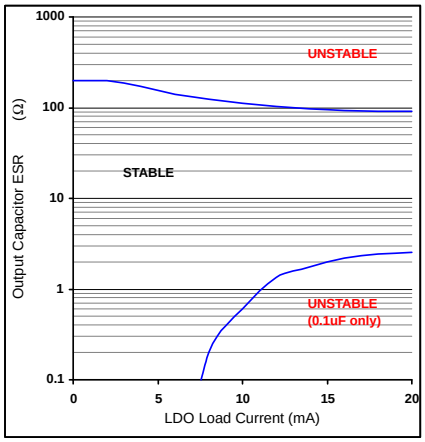


Figure 16. LDO Stability Region

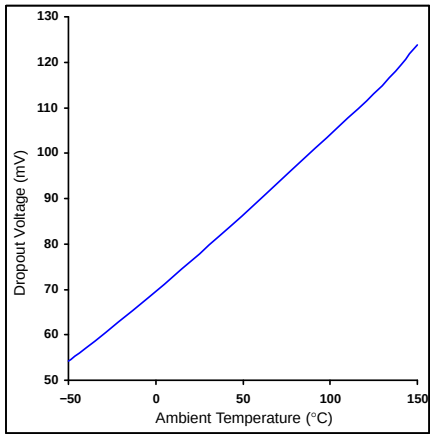


Figure 17. LDO Dropout Voltage vs. Temperature

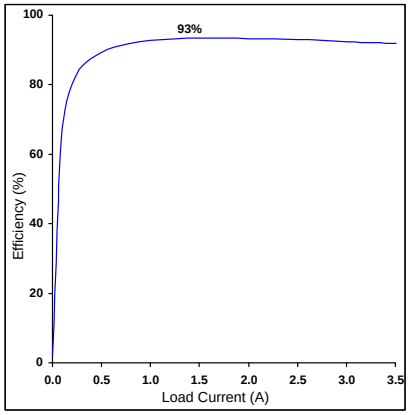


Figure 18. Efficiency vs. Load Current 5 V, 170 kHz Demo Board

DETAILED OPERATING DESCRIPTION

General

The NCV8851−1 is a synchronous buck controller with internal 1.5 A gate drivers designed to drive NMOS FETs. The internal gate drivers simplify design, improve performance and efficiency and minimize board area. The controller uses an 800 mV, 2.0% reference, allowing for a wide range of precise output voltage programmability.

The NCV8851−1 also provides a programmable fixed frequency range of 170 kHz to 500 kHz, allowing more design flexibility in compromising efficiency versus components' size and cost. This frequency is conveniently set with an external resistor to ground. An external clock signal can also be used to synchronize the NCV8851−1 to a higher operating frequency during operation.

To protect against possible damage of external power−stage components, excessive inrush of current during start−up is prevented by an internal soft−start, and inductor current is limited via average current limiting (ACL) and cycle−by−cycle overcurrent protection (OCP). Thermal shutdown (TSD) is also implemented to protect the device from overheating.

Average Current Mode Control

The NCV8851−1 employs an average current mode control (ACMC) architecture to regulate the output voltage. ACMC uses two loops, as seen in Figure 19. Through the current error amplifier (CEA), the inner current loop monitors the inductor current with the unity gain current sense amplifier (CSA). The current loop responds to input voltage changes, affecting the line transient response. Using the voltage error amplifier (VEA), the outer voltage loop monitors the output voltage, responding to output load changes, affecting the load transient response. Feedback resistors in the voltage loop select the output voltage.

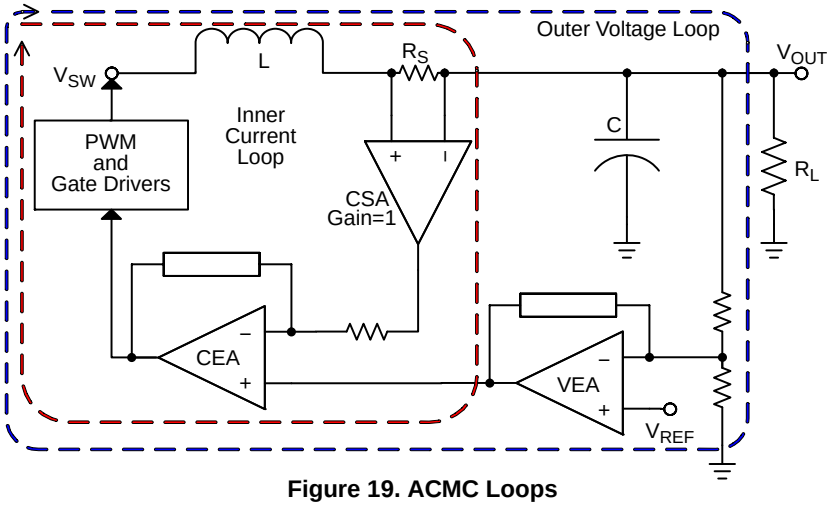


Figure 19. ACMC Loops

Unlike voltage mode control (VMC) of buck regulators, which almost always require the extra components of a Type−III compensation network for adequate transient response, ACMC buck regulators use Type−II compensation. This greatly simplifies the compensator design and optimization process, while offering much faster transient response than a Type−I compensation network. Additionally, the two−loop system separates the effects of output components between the two loops, further simplifying the compensation process.

Type−II compensation places a zero and two poles in each of the error loops to offset the effects of the inherent open−loop response. This compensation requires a resistor and two capacitors in the feedback loop for each of the error amplifiers, shown as complex impedances in Figure 19. An input resistor from the CSA to the CEA sets the gain of the CEA. The voltage loop also has a pair of feedback resistors from V_{OUT} to set the output voltage and gain of the VEA.

Enable

The enable input (EN) is a TTL−compatible input used to activate the internal LDO. The NCV8851−1 is disabled when the EN pin is pulled below the enable input logic low threshold voltage, causing a normal shutdown to occur, putting the part into a low quiescent current sleep mode. Once the device has been disabled it must remain disabled for the minimum disable time (20 ms) or abnormal startup behavior may be observed after enable is asserted. When the EN pin is pulled above the enable input logic high threshold voltage, the part is enabled, the LDO output is brought up and then the internal soft−start begins.

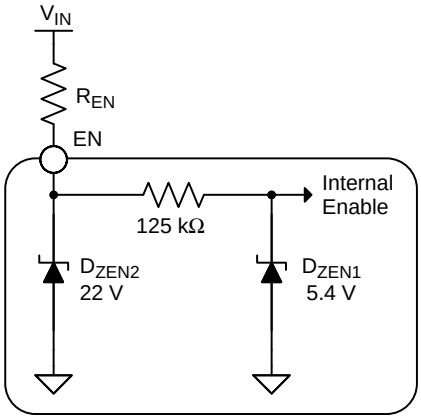


Figure 20. Enable Pin Equivalent Structure

The EN pin can be tied to V_{IN} in order to enable the part. If EN is above 22 V, D_{ZEN2} will be conducting, as well as D_{ZEN1}. The current to D_{ZEN1} is limited by an internal 125 kΩ resistor. If D_{ZEN2} is conducting, it is recommended at least 250 μA is pulled through this diode. The resistor R_{EN} must be used if V_{IN} can go above 20 V as follows.

$$R_{EN(max)} = \frac{V_Z}{250\ \mu A}$$

Where V_Z is the amount of volts where D_{ZEN2} is conducting, but not yet supplied with 250 μA. For example, setting V_Z to 1 V means R_{EN} must be less than 4 kΩ for D_{ZEN2} to have at least 250 μA when V_{IN} is at least 23 V; for the range of V_{IN} between 22 V and 23 V, D_{ZEN2} will be conducting, but not with the recommended 250 μA current.

UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{IN_IC} is too low to support the internal rails and power the controller. The IC will start up when enabled and V_{IN_IC} surpasses the UVLO threshold and will shutdown when V_{IN_IC} drops below the UVLO threshold minus the UVLO hysteresis. While V_{IN} is less than the set point for V_{OUT}, the output will run at max duty cycle, after soft−start, once V_{IN_IC} surpasses the UVLO threshold. If EN is high and not tied to V_{IN}, the output will begin to rise up while in UVLO, if a minimum output load of 1 kΩ is not met.

Thermal Shutdown

The NCV8851−1 provides Thermal Shutdown (TSD), which monitors the die temperature and turns off the top and bottom gate drivers if an over temperature condition is detected, for added protection. The internal soft−start capacitor is also discharged. A normal soft−start will occur when the die temperature falls below the TSD threshold minus the TSD hysteresis.

Duty Cycle and Maximum Pulse Width Limits

In steady state dc operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. There is a built in minimum off−time which ensures that the bootstrap supply is charged every cycle, determining the maximum duty cycle at a given frequency.

The NCV8851−1 can achieve at least a 95% duty cycle while operating at frequencies up to 200 kHz (89% at up to 500 kHz).

Internal Soft−Start

The NCV8851−1 features an internal soft−start function, which reduces inrush current and overshoot of the output voltage. Figures 21 and 22 show a typical soft−start sequence.

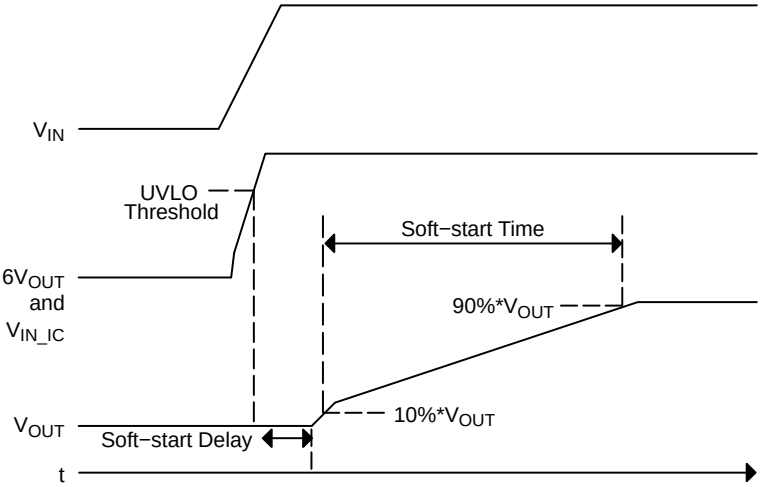


Figure 21. Normal Start−up

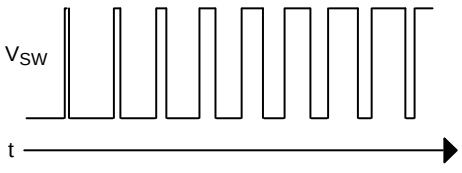


Figure 22. Switch−node in Soft−Start

Soft−start is achieved by ramping up the internal soft−start voltage (V_{SS}), which is applied to the non−inverting input of the voltage error amplifier, effectively limiting the slew rate of V_{OUT} rising. This ramp is generated by charging an internal soft−start capacitor based on the internal oscillator, causing the soft−start time to be inversely related to the frequency set by R_{OSC}. The internal soft−start capacitor is discharged when the part is disabled, enters TSD or enters UVLO, ensuring a proper start−up when the part is re−enabled, leaves TSD or leaves UVLO.

This sequence begins once V_{IN_IC} surpasses its UVLO threshold when the part is enabled and the LDO output has risen. After an initial delay to assure a clean start−up, switching begins, the output initially rises quickly and then rises monotonically. The duty cycle is gradually increased until V_{OUT} has reached its set point or until maximum duty cycle is reached.

Normal Shutdown Behavior and Sleep Mode

Normal shutdown occurs when the IC stops switching because the input supply drops below the UVLO threshold, the part enters TSD or the part is disabled. When disabled, the part enters sleep mode.

In sleep mode, the LDO turns off and its output capacitor discharges, causing switching to stop, the internal soft−start capacitor to discharge and GH and GL to go low. The switch node enters a high impedance state and the output inductor and capacitors discharge through the load. The supply current reduces to the sleep mode quiescent current.

Internal Linear Regulator (LDO)

The NCV8851−1 has an onboard low−dropout linear regulator (LDO) internally connected to drive the low−side gate. The $6V_{OUT}$ pin should be externally connected to the V_{IN_IC} pin to power the internal rails. Typically, a RC filter is used from $6V_{OUT}$ to V_{IN_IC} to further decrease noise on the internal rails.

The $6V_{OUT}$ pin should be externally connected through a low leakage (< 100 μA at T_{max}) diode to the BST pin, charging the BST capacitor during off−time to generate a voltage for the high−side driver. When the part is enabled and V_{IN} is below the LDO regulated value, the LDO is in dropout and it tracks V_{IN}. The LDO regulates its output once V_{IN} is above the output set point plus the dropout voltage.

An external bypass capacitor must be connected from $6V_{OUT}$ to ground. A short to ground or overcurrent condition on the $6V_{OUT}$ pin will be mitigated by the LDO current limit and internal thermal shutdown (TSD) circuitry which disables all outputs. A normal soft−start will occur when the die temperature falls below the TSD threshold.

Drivers

The NCV8851−1 includes 1.5 A gate drivers to switch external N−Channel MOSFETs. This allows the NCV8851−1 to address high−power, as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increases efficiency, which minimizes power dissipation, by minimizing the body diode conduction time, while protecting against cross−conduction (shoot−through) of the MOSFETs. A detailed block diagram of the non−overlap and gate drive circuitry used in the chip and related external components is shown in Figure 23.

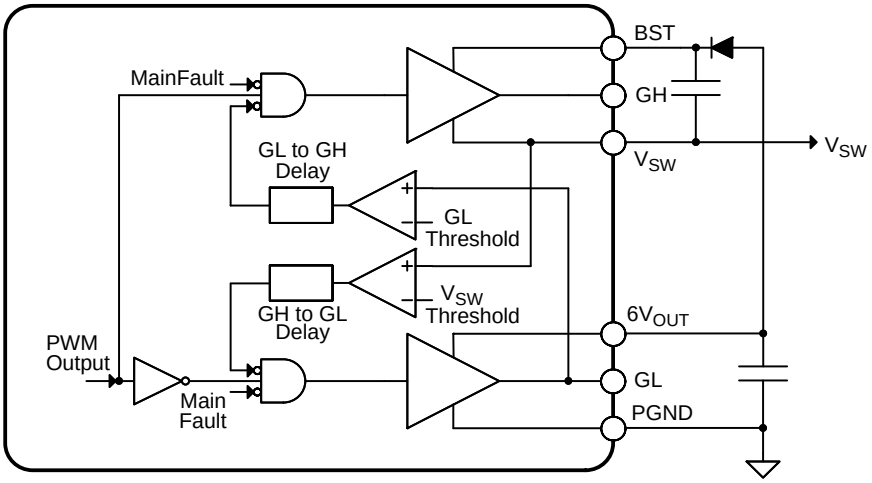


Figure 23. Gate Driver Block Diagram

A capacitor is placed from V_{SW} to BST and a diode is placed from $6V_{OUT}$ to BST to create a bootstrap supply on the BST pin for the high−side floating gate driver. This ensures that the voltage on BST is about $6V_{OUT}$ higher than V_{SW}, less a diode drop, yielding a gate drive voltage high enough to enhance the high−side MOSFET. The BST capacitor supplies the charge used by the gate driver to charge up the input capacitance of the high−side MOSFET, and is typically chosen to be at least a decade larger than this capacitance. A 0.1 μF BST capacitor is recommended.

Since the BST capacitor only recharges when the low−side MOSFET is on, pulling V_{SW} down to ground, the NCV8851−1 has a minimum off−time. This also means that the BST capacitor cannot be arbitrarily large, since $6V_{OUT}$ needs to be able to charge it up during this minimum off−time so the high−side gate driver doesn't run out of headroom. $6V_{OUT}$ needs to supply charge both to the BST capacitor and also the low−side driver, so the LDO capacitor must be sufficiently larger than the BST capacitor. A 1 μF LDO capacitor is recommended.

Careful selection and layout of external components is required to realize the full benefit of the onboard drivers.

The capacitors between V_{IN} and GND and between BST and V_{SW} must be placed as close as possible to the IC. The current paths for the GH and GL connections must be optimized, minimizing parasitic resistance and inductance.

Current Limiting and Overcurrent Protection

The NCV8851−1 contains average current limiting (ACL) and cycle−by−cycle overcurrent protection (OCP) to protect the power switches, inductor, current sense resistor and other external components. The current through the inductor is continuously sensed using the CSP and CSN pins. A sense resistor is placed between these pins to translate the output current to a proportional voltage. This voltage is compared to a fixed internal voltage threshold.

When the differential voltage exceeds the ACL threshold, the PWM pulse is terminated for this cycle, limiting the current through the inductor. In steady−state operation, decreasing the load resistance while in ACL will cause the duty cycle and V_{OUT} to decrease proportionally without skipping pulses or jitter.

There is also a fast OCP path which is tripped when the differential voltage exceeds the OCP threshold, which is above the ACL threshold. This causes the PWM pulse to be terminated very quickly and disables the part from switching back on until the current through the inductor has dropped below the OCP threshold. Once the inductor current is below the OCP threshold, the part will begin switching again and the current will be limited by ACL, until the inductor current drops below the ACL threshold.

An advantage of this current limiting scheme is that the NCV8851−1 will limit large transient currents yet resume normal operation on the following cycle. Additionally, the current will not run away, nor will the part latch off in case of a short, which is typical of other current limiting schemes employing high−side current sensing.

SYNC Feature

An external clock signal can synchronize the NCV8851−1 to a higher frequency. The rising edge of the SYNC pulse turns on the power switch to start a new switching cycle, as shown in Figure 24. There is a 0.5 μs delay between the rising edge of the SYNC pulse and rising edge of the V_{SW} pin voltage. The SYNC threshold is TTL logic compatible, and duty cycle of the SYNC pulses can vary from 10% to 90%. The SYNC frequency must be higher than the internal oscillator frequency set by R_{OSC}.

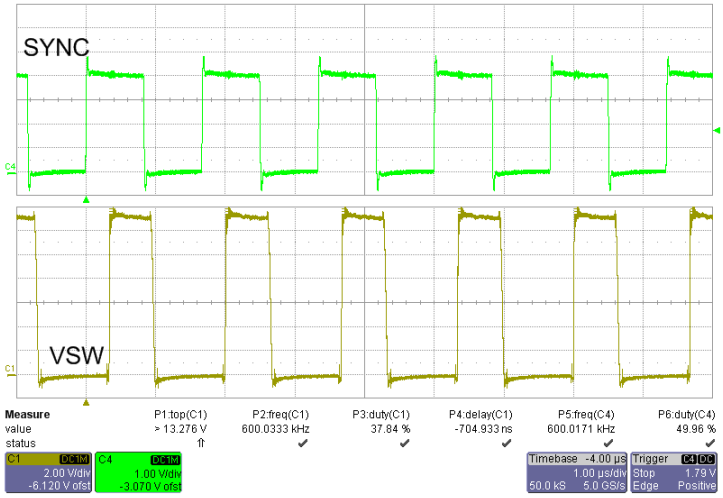


Figure 24. Synchronization from 170 kHz to an external 600 kHz signal

APPLICATIONS INFORMATION

Design Methodology

Choosing external components for the NCV8851−1 encompasses the following design process:

1. Define operational parameters
2. Select switching frequency
3. Select current sensor
4. Select output inductor
5. Select output capacitors
6. Select input capacitors
7. Select compensator components

(1) Operational Parameter Definition

Before proceeding with the rest of the design, certain operational parameters must be defined. These are application−dependent and include the following:

V_{IN}: input voltage, range from minimum to maximum with a typical value [V]

V_{OUT}: output voltage [V]

I_{OUT}: output current, range from minimum to maximum with initial start−up value [A]

I_{CL}: desired typical current−limit [A]

A number of basic calculations must be performed up−front to use in the design process, as follows:

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(max)}}$$

$$D = \frac{V_{OUT}}{V_{IN(typ)}}$$

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(min)}}$$

Where: D_{MIN}: minimum duty cycle (ideal) [%]

$V_{IN(max)}$: maximum input voltage [V]

D: typical duty cycle (ideal) [%]

$V_{IN(typ)}$: typical input voltage [V]

D_{MAX}: maximum duty cycle (ideal) [%]

$V_{IN(min)}$: minimum input voltage [V]

It should be noted that these are the ideal duty cycles; the actual duty cycles will be marginally higher than these calculated values. The actual duty cycles are dependent on load due to voltage drops in the MOSFETs, inductor and current sensor.

(2) Switching Frequency Selection

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values to achieve the same inductor current ripple and output voltage ripple. However, increasing the frequency increases the switching losses of the MOSFETs, leading to decreased efficiency, especially noticeable at light loads.

Typically, the switching frequency is selected to avoid interfering with signals of known frequencies. Often, in this case, the frequency can be programmed to a lower value with R_{OSC} and then a higher−frequency signal can be applied to the SYNC pin to increase the frequency dynamically to avoid given frequencies. A spread spectrum signal could also be used for the SYNC input, as long as the lowest frequency in the range is above the programmed frequency set by R_{OSC}. Additionally, the highest SYNC frequency must not exceed maximum switching frequency limits.

There are two limits on the maximum allowable switching frequency: minimum off−time and minimum on−time. These set two different maximum switching frequencies, as follows:

$$F_{SW(max)1} = \frac{1 - D_{MAX}}{T_{MinOff}}$$

$$F_{SW(max)2} = \frac{D_{MIN}}{T_{MinOn}}$$

Where: $F_{SW(max)1}$: maximum switching frequency due to minimum off−time [Hz]

T_{MinOff}: minimum off−time [s]

$F_{SW(max)2}$: maximum switching frequency due to minimum on−time [Hz]

T_{MinOn}: minimum on−time [s]

Alternatively, the minimum and maximum operational input voltage can be calculated as follows:

$$V_{IN(min)} = \frac{V_{OUT}}{1 - T_{MinOff} \cdot F_{SW}}$$

$$V_{IN(max)} = \frac{V_{OUT}}{T_{MinOn} \cdot F_{SW}}$$

Where: F_{SW}: switching frequency [Hz]

The switching frequency is programmed by selecting the resistor connected between the R_{OSC} pin and ground. The grounded side of this resistor should be directly connected to the AGND pin. Avoid running any noisy signals under the resistor, since injected noise could cause frequency jitter.

The graph in Figure 25 shows the required resistance to program the frequency. From 150 to 450 kHz, the following formula is accurate to within 3%:

$$R_{OSC} = \frac{8687000}{F_{SW}}$$

Where: R_{OSC}: frequency program resistor [Ω]

Some specific values for switching frequency with standard 1% resistors can be seen in Table 1.

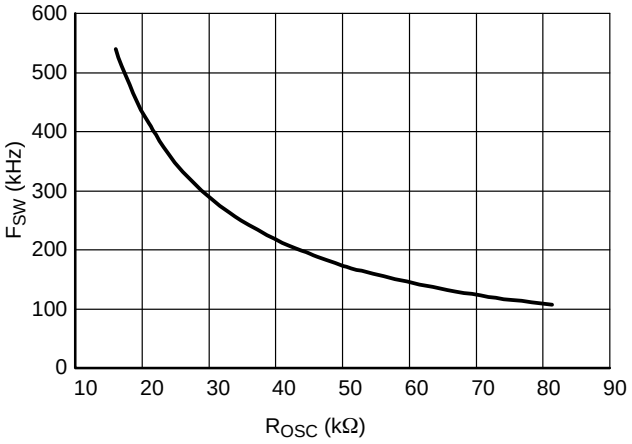


Figure 25. Frequency vs. R_{OSC}

Table 1. Frequency vs. R_{OSC}

F_{SW} (kHz)	R_{OSC} (kΩ)
170	51.1
250	34.8
300	28.7
360	23.2
500	16.2

The soft−start time can be estimated as follows:

$$T_{SS} \approx \frac{F_0}{F_{SW}} \cdot T_{SS0}$$

Where: T_{SS}: soft−start time [s]

F_0: specified frequency [Hz]

T_{SS0}: soft−start time at specified frequency [s]

(3) Current Sensor Selection

Current sensing for average current mode control relies on the inductor current signal. This is translated into a voltage via a current sensor, which is then measured differentially by the current sense amplifier, generating a single−ended output to use as a control signal. The easiest means of implementing this transresistance is through the use of a sense resistor in series with the output inductor and capacitors. A sense resistor should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}}$$

Where: R_S: sense resistor [Ω]

V_{CL}: current limit threshold voltage [V]

I_{CL}: desired current limit [A]

Alternative methods, such as lossless inductor current sensing, are feasible but beyond the scope of this document.

(4) Output Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the power supply, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, an inductor is chosen for a set amount of current ripple and to assure adequate transient response.

Larger inductor values limit the switcher's ability to slew current through the output inductor in response to output load transients, impacting the dynamic response. While the inductor is slewing current during this time, output capacitors must supply the load current. Therefore, decreasing the inductance allows for less output capacitance to hold the output voltage up during a load step. Load transient simulation is a powerful tool in anticipating this response.

For switchers with both cycle−by−cycle overcurrent protection (OCP) and average current limiting (ACL), the OCP and ACL references are compared to the sensed current via sense resistance, R_S. A minimum inductance is required to prevent the OCP from tripping during the onset of ACL during typical operation as follows:

$$L_{MIN} = \frac{V_{OUT}(1 - D)}{2 \cdot F_{SW}} \cdot \frac{R_S}{\Delta V_{CL}}$$

Where: L_{MIN}: minimum inductance to assure OCP and ACL do not both trip [H]

ΔV_{CL}: difference between OCP and ACL threshold voltages [V]

For switchers that use the current signal of the inductor for control purposes, the voltage ripple over the sense resistance must be sufficient in magnitude to counteract the contribution due to inherent comparator offsets and other errors, as follows:

$$L_{MAX} = \frac{V_{OUT} \cdot (1 - D_{MAX})}{F_{SW}} \cdot \frac{R_S}{\kappa_L \cdot V_{CL}}$$

Where: L_{MAX}: maximum inductance to assure adequate voltage ripple over the sense resistance [H]

κ_L: inductor peak−to−peak current ripple to current limit ratio [%]

V_{CL}: threshold voltage for the current limit [V]

As a rule of thumb, ensuring that κ_L is at least 5% to 10% has been empirically sufficient.

Smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current, which causes higher output voltage ripple. The peak−to−peak ripple current is given by the following equation:

$$i_L = \frac{V_{OUT} \cdot (1 - D)}{L \cdot F_{SW}}$$

Where: i_L: peak−to−peak output current ripple [App]

The ripple current is at a maximum when the duty cycle is at a minimum value and vice versa, as follows:

$$i_{L(max)} = \frac{V_{OUT} \cdot (1 - D_{MIN})}{L \cdot F_{SW}}$$

$$i_{L(min)} = \frac{V_{OUT} \cdot (1 - D_{MAX})}{L \cdot F_{SW}}$$

Where: $i_{L(max)}$: maximum inductor current ripple [App]

$i_{L(min)}$: minimum inductor current ripple [App]

From this equation it is clear that the ripple current increases as L decreases, emphasizing the trade−off between dynamic response and ripple current. The peak and valley values of the triangular current waveform are as follows:

$$I_{L(pk)} = I_{OUT} + \frac{i_L}{2}$$

$$I_{L(vly)} = I_{OUT} - \frac{i_L}{2}$$

Where: $I_{L(pk)}$: peak (maximum) value of ripple current [A]

$I_{L(vly)}$: valley (minimum) value of ripple current [A]

Saturation current is specified by inductor manufacturers as the current at which the inductance value has dropped a certain percentage from the nominal value, typically 10%. For stable operation, the output inductor must be chosen so that the inductance is close to the nominal value even at the peak output current, $I_{L(pk)}$. It is recommended to choose an inductor with saturation current sufficiently higher than the peak output current, such that the inductance is very close to the nominal value at the peak output current. This introduces a safety factor and allows for more optimized compensation.

Inductor efficiency is another consideration when selecting an output inductor. Inductor losses include dc and ac winding losses and core losses. Core losses include eddy current losses, which are very low due to high core resistance, and magnetic hysteresis losses, which increase with peak−to−peak ripple current. Core losses also increase as switching frequency increases.

Ac winding losses are based on the ac resistance of the winding and the RMS ripple current through the inductor, which is much lower than the dc current. The ac winding losses are due to skin and proximity effects and are typically much less than the dc losses, but increase with frequency. Dc winding losses account for a large percentage of output inductor losses and are the dominant factor at switching frequencies at or below 500 kHz. The dc winding losses in the inductor can be calculated with the following equation:

$$P_{L(dc)} = I_{OUT}^2 \cdot R_{dc}$$

Where: $P_{L(dc)}$: dc winding losses in the output inductor

R_{dc}: dc resistance of the output inductor (DCR)

As can be seen from the above equation, to minimize inductor losses, an inductor with very low DCR should be chosen.

(5) Output Capacitor Selection

The output capacitor is a basic component for the fast response of the power supply. During a load step, for the first few microseconds, it supplies the current to the load. The controller immediately recognizes the load step and increases the duty cycle, but the current slope is limited by the inductor's slew rate. During a load release, the output voltage will overshoot. The capacitance will dampen this undesirable response, decreasing the amount of voltage overshoot.

In the case of stepping into a short, the inductor current approaches zero with the worst case initial current at the current limit and the initial voltage at the output voltage set point, calculating the voltage overshoot as follows:

$$\Delta V_{OS} = \sqrt{\frac{L \cdot I_{CL}^2}{C} + V_{OUT}^2} - V_{OUT}$$

Accordingly, a minimum amount of capacitance can be chosen for a maximum allowed output voltage overshoot:

$$C_{MIN} = \frac{L \cdot I_{CL}^2}{(V_{OUT} + \Delta V_{OS(max)})^2 - V_{OUT}^2}$$

Where: C_{MIN}: minimum amount of capacitance to minimize voltage overshoot to $\Delta V_{OS(max)}$ [F]

$\Delta V_{OS(max)}$: maximum allowed voltage overshoot during a short [V]

A maximum amount of capacitance can be found based on the inrush current and current limit. To calculate the input startup current, the following equation can be used:

$$I_{INRUSH} = \frac{C_{OUT} \cdot V_{OUT}}{t_{SS}} + I_{OUT(i)}$$

Where: I_{INRUSH}: input current during startup

$I_{OUT(i)}$: initial output current

If the inrush current is higher than the steady−state input current with the maximum load, then the input fuse should be rated accordingly, if one is used. During soft−start, the inductor current must provide current to the load, as well as current to charge the output capacitor. The maximum current which the inductor is allowed to conduct is the current limit. Setting the inrush current to the current limit, this puts a limit on the maximum capacitor size, as follows:

$$C_{MAX} = \frac{(I_{CL} - I_{OUT(i)}) \cdot t_{SS}}{V_{OUT}}$$

Where: C_{MAX}: maximum output capacitance [F]

Capacitors should also be chosen to provide acceptable output voltage ripple with a dc load, in addition to limiting voltage overshoot during a dynamic response. Key specifications are equivalent series resistance (ESR) and equivalent series inductance (ESL). The output capacitors must have very low ESL for best transient response. The PCB traces will add to the ESL, but by putting the output capacitors close to the load, this effect can be minimized and ESL neglected in determining output voltage ripple.

The capacitance itself causes a voltage ripple due to the current ripple. This is as follows:

$$V_Q = i_L \cdot \frac{D}{C \cdot F_{SW}}$$

Where: v_Q: output voltage ripple due to output capacitance [Vpp]

Also, the ripple current through the inductor causes a voltage ripple over the output capacitor due to its ESR as follows:

$$V_{ESR} = i_L \cdot R_{ESR}$$

Where: v_{ESR}: output voltage ripple due to the effects of ESR [Vpp]

R_{ESR}: total ESR of output capacitors [Ω]

Typically, the ripple due to ESR dominates, having the largest effect on output voltage ripple. The total output voltage ripple in steady−state operation can be calculated as follows:

$$V_{OUT} = V_Q + V_{ESR} = \kappa_C \cdot V_{OUT}$$

Where: v_{OUT}: total output voltage ripple [Vpp]

κ_C: percent output voltage ripple [%]

Typically, the voltage ripple percentage is a performance parameter used to decide on the desired output capacitor. The maximum total effective ESR of the output capacitors is calculated as follows:

$$R_{ESR(max)} = \frac{V_{OUT} - V_Q}{i_{L(max)}}$$

Where: $R_{ESR(max)}$: maximum allowable total ESR of output capacitors

It should be noted that these values of ESR are at the switching frequency and ESR decreases as frequency increases. The steady−state power lost due to the ESR of the output capacitor can be calculated as follows:

$$P_{C(ESR)} = \frac{1}{3} i_L{}^2 \cdot R_{ESR}$$

(6) Input Capacitor Selection

The input capacitors have to sustain the ripple current produced during the on time of the high−side MOSFET and must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{IN(RMS)} = I_{OUT}\sqrt{D \cdot (1 - D)}$$

Where: $I_{IN(RMS)}$ = input RMS current

The large majority of the ripple spectrum will be at the switching frequency. The above equation reaches its maximum value with D = 0.5, $I_{IN(RMS)} = I_{OUT}/2$. The input capacitors must be rated to handle a ripple current of one−half the maximum output current at the switching frequency.

ESR is the majority cause of losses in the input capacitors. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = I_{IN(RMS)}{}^2 \cdot R_{ESR(CIN)}$$

Where: P_{CIN} = power loss in the input capacitors

$R_{ESR(CIN)}$ = effective series resistance of the input capacitance

Due to large current transients through the input capacitors, electrolytic, polymer or ceramics should be used. If a tantalum must be used, it must be surge protected, to prevent against capacitor failure. Due to the large ripple current, it is common to put small ceramic capacitors in parallel with the bulk input capacitors, which will handle a significant portion of the ripple current. A value of 0.01 μF to 0.1 μF placed near the MOSFETs is recommended.

(7) Compensator Design

The purpose of the compensators is to stabilize the dynamic response of the converter. By optimizing the compensators, stable regulation with fast input line and output load transient response is achieved.

Compensator design is related to the placement of zeros and poles in the closed loop, in order to assure stability with optimized transient response. The general approach is to use some rule of thumb values and then tune them through simulation to optimize load step response, while assuring stability over line and load variations.

Type−II compensators are used with the two error amplifiers in average current mode control. The CEA closes the inner current−loop and the VEA closes the outer voltage−loop. As a rule of thumb, a zero is placed in each loop with the intent to compensate the effects of the double pole from the output inductor and capacitor. Additionally, a pole is placed at origin, due to the negative feedback, and a pole is also placed in each loop with the intent to compensate the effects of the double right−half−plane zero from the current sampling function.

The crossover frequency is then set so that gain limitations of the error amplifier are not exceeded. The compensator must assure there is adequate phase margin in the total closed−loop response, which can be analyzed on a small−signal basis. Further reduction in loop gain, via decreasing the crossover frequency, may be required to avoid large−signal clamping limitations; this effect can be seen in simulation and taken care of in the compensator tuning process.

Equations for placement of pole, zero and crossover frequency follow:

Current−loop Compensator	Voltage−loop Compensator
$\omega_{iz} = \frac{1}{\sqrt{L \cdot C}}$	$\omega_{vz} = \frac{2}{\sqrt{L \cdot C}}$
$\omega_{ip} = \frac{F_{SW} \cdot \pi}{4}$	$\omega_{vp} = \frac{F_{SW} \cdot \pi}{4}$
$\omega_i = 2 \cdot \omega_{ip}$	$\omega_v = 2 \cdot \omega_{vp}$

The implementation of the above compensators is through a resistance on the negative input (R_{C2}, R_{F1}), resistor (R_{C1}, R_{V1}) and capacitor (C_{C1}, C_{V1}) in series in feedback and another capacitor (C_{C2}, C_{V2}) in feedback of an opamp. The feedback capacitors (C_{C1}, C_{V1}) in series with feedback resistor are chosen, on the order of less than 3 nF. The values are calculated as follows:

Current−loop Compensator	Voltage−loop Compensator
$R_{C1} = \frac{1}{\omega_{iz} \cdot C_{C1}}$	$R_{V1} = \frac{1}{\omega_{vz} \cdot C_{V1}}$
$C_{CE} = \frac{1}{\omega_{ip} \cdot R_{C1}}$	$C_{VE} = \frac{1}{\omega_{vp} \cdot R_{V1}}$
$C_{C2} = \frac{C_{C1}}{\frac{C_{C1}}{C_{CE}} - 1}$	$C_{V2} = \frac{C_{V1}}{\frac{C_{V1}}{C_{VE}} - 1}$
$R_{C2} = \frac{1}{\omega_i \cdot (C_{C1} + C_{C2})}$	$R_{F1} = \frac{1}{\omega_v \cdot (C_{V1} + C_{V2})}$

The resistor divider on the negative input of the VEA also sets the output voltage. This resistor divider is composed of a resistor from the output voltage to the negative input of the VEA (R_{F1}) and a resistor from the negative input of the VEA to ground (R_{F0}). The bottom resistor value is calculated as follows:

$$R_{F0} = \frac{R_{F1} \times V_{REF}}{V_{OUT} - V_{REF}}$$

Thermal Considerations

The power dissipation of the NCV8851−1 varies with the MOSFETs used, V_{IN} and the boost voltage (V_{BST}). The average MOSFET gate current typically dominates the control IC power dissipation. The IC power dissipation can be estimated as follows:

$$P_{IC} = V_{IN} \cdot I_Q + P_{HS} + P_L$$

Where: P_{IC}: control IC power dissipation

I_Q: IC measured supply current (quiescent current)

P_{TG}: high−side MOSFET gate driver losses

P_{BG}: low−side MOSFET gate driver losses

The high−side switching MOSFET gate driver losses are:

$$P_{TG} = Q_{TG} \cdot F_{SW} \cdot V_{BST}$$

Where: Q_{TG}: total high−side MOSFET gate charge at V_{BST}

V_{BST}: BST pin voltage

The low−side synchronous rectifier MOSFET gate driver losses are:

$$P_{BG} = Q_{BG} \cdot F_{SW} \cdot V_{CC}$$

Where: Q_{BG}: total low−side MOSFET gate charge at V_{IN}

The junction temperature of the controller can then be calculated as follows:

$$T_J = T_A + P_{IC} \cdot R_{\theta JA}$$

Where: T_J = junction temperature of the IC

T_A = ambient temperature

$R_{\theta JA}$ = junction−to−ambient thermal resistance of the IC package

The package thermal resistance ($R_{\theta JA}$) can be obtained from the specifications section of this data sheet and a calculation can be made to determine the IC junction temperature. It should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors and the amount of metal connected to the IC impact the temperature of the device. Use these calculations as a guide, but measurements should be taken in the actual application.

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