

NDD01N60, NDT01N60

N-Channel Power MOSFET 600 V, 8.5 Ω

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	V_{DS}	600		V
Continuous Drain Current $R_{\theta JC}$ Steady State, $T_C = 25^\circ\text{C}$ (Note 1)	I_D	1.5	0.4	A
Continuous Drain Current $R_{\theta JC}$ Steady State, $T_C = 100^\circ\text{C}$ (Note 1)	I_D	1.0	0.25	A
Pulsed Drain Current, $t_p = 10 \mu\text{s}$	I_{DM}	6.0	1.5	A
Power Dissipation – $R_{\theta JC}$ Steady State, $T_C = 25^\circ\text{C}$	P_D	46	2.5	W
Gate-to-Source Voltage	V_{GS}	± 30		V
Single Pulse Drain-to-Source Avalanche Energy ($I_{PK} = 1.0 \text{ A}$)	EAS	13		mJ
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Source Current (Body Diode)	I_S	1.5	0.4	A
Lead Temperature for Soldering Leads	T_L	260		$^\circ\text{C}$
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150		$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Limited by maximum junction temperature
2. $I_S = 1.5 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDD01N60	$R_{\theta JC}$	2.7	$^\circ\text{C}/\text{W}$
Junction-to-Ambient (Note 4) NDD01N60	$R_{\theta JA}$	38	$^\circ\text{C}/\text{W}$
(Note 3) NDD01N60-1		96	
(Note 4) NDT01N60		58	
(Note 5) NDT01N60		141	

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

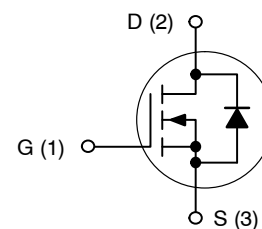


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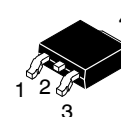
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$
600 V	8.5 Ω @ 10 V

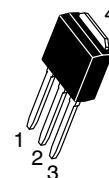
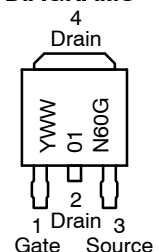
N-Channel MOSFET



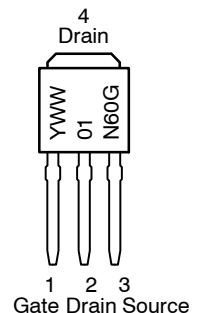
MARKING DIAGRAMS



**DPACK
CASE 369C
STYLE 2**



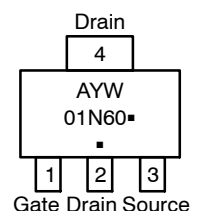
**IPACK
CASE 369D
STYLE 2**



Y = Year
WW = Work Week
G = Pb-Free Package



**SOT-223
CASE 318E
STYLE 3**



A = Assembly Location
Y = Year
W = Work Week
01N60 = Specific Device Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NDD01N60, NDT01N60

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	Reference to 25°C, I _D = 1 mA		660		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	T _J = 25°C		1	μA
			T _J = 125°C		50	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 50 μA	2.2	3.3	3.7	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			7.0		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 0.2 A		8.0	8.5	Ω
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 0.2 A		0.9		S

CHARGES, CAPACITANCES & GATE RESISTANCES

Input Capacitance (Note 7)	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		160		pF
Output Capacitance (Note 7)	C _{oss}			22		
Reverse Transfer Capacitance (Note 7)	C _{rss}			4.0		
Total Gate Charge (Note 7)	Q _g	V _{DS} = 300 V, I _D = 0.4 A, V _{GS} = 10 V		7.2		nC
Gate-to-Source Charge (Note 7)	Q _{gs}			1.2		
Gate-to-Drain Charge (Note 7)	Q _{gd}			3.1		
Plateau Voltage	V _{GP}			4.5		V
Gate Resistance	R _g			6.7		Ω

SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 0.4 A, V _{GS} = 10 V, R _G = 0 Ω		8.0		ns
Rise Time	t _r			5.1		
Turn-off Delay Time	t _{d(off)}			16.5		
Fall Time	t _f			21.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Diode Forward Voltage	V _{SD}	I _S = 0.4 A, V _{GS} = 0 V	T _J = 25°C		0.78	1.6	V
			T _J = 125°C		0.63		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, V _{DD} = 30 V I _S = 1.0 A, d _i /d _t = 100 A/μs		179			ns
Charge Time	t _a			37			
Discharge Time	t _b			141			
Reverse Recovery Charge	Q _{rr}			288			nC

6. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

7. Guaranteed by design.

8. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NDD01N60-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD01N60T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel
NDT01N60T1G	SOT-223 (Pb-Free, Halogen-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

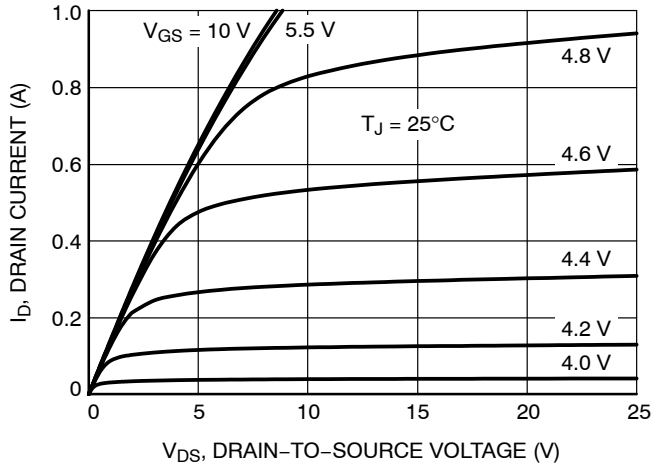


Figure 1. On-Region Characteristics

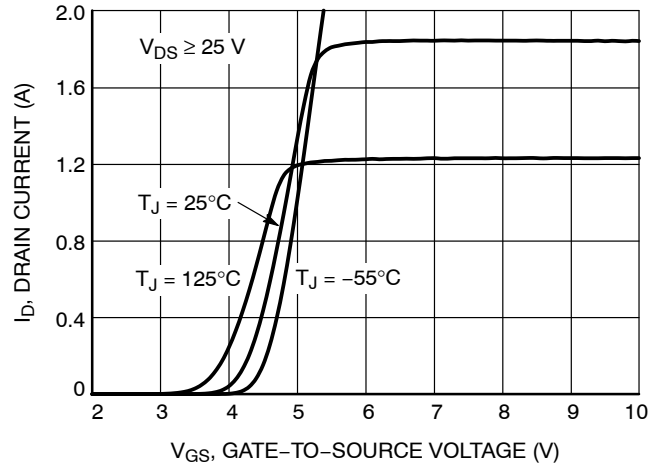


Figure 2. Transfer Characteristics

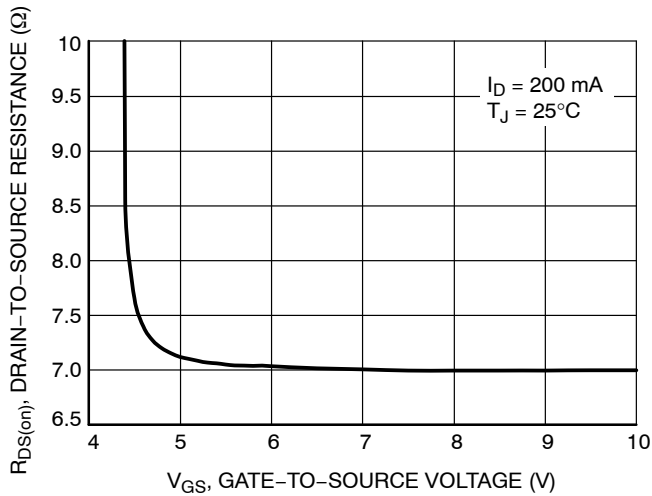


Figure 3. On-Resistance vs. Gate Voltage

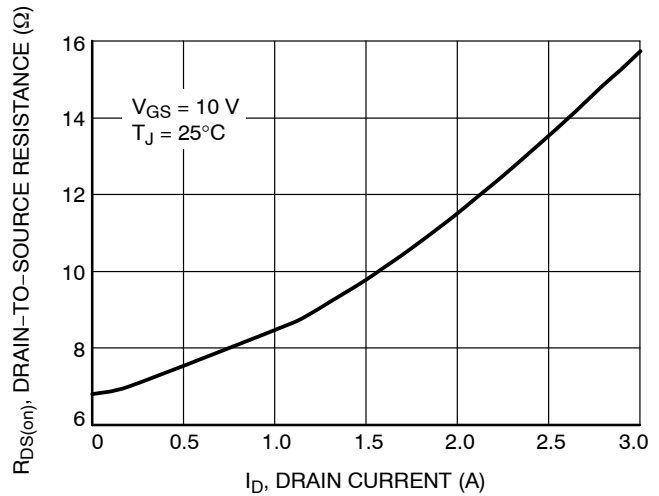


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

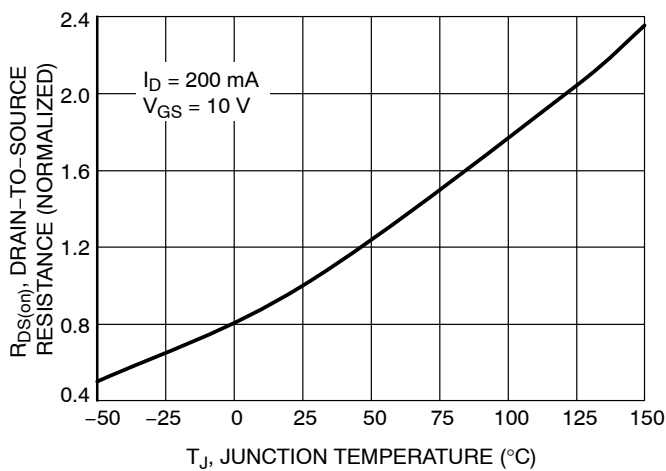


Figure 5. On-Resistance Variation with Temperature

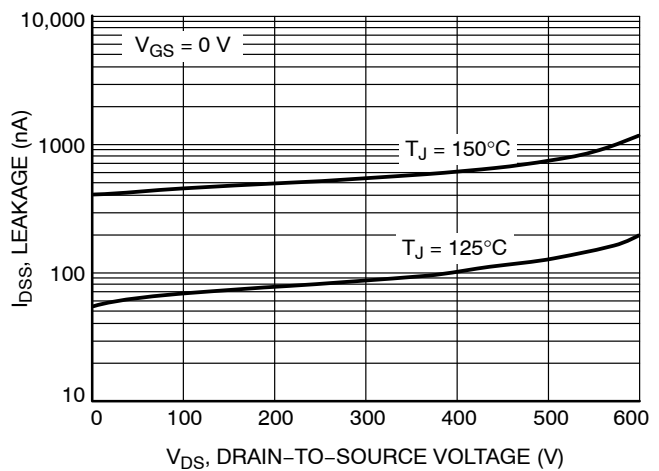


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NDD01N60, NDT01N60

TYPICAL CHARACTERISTICS

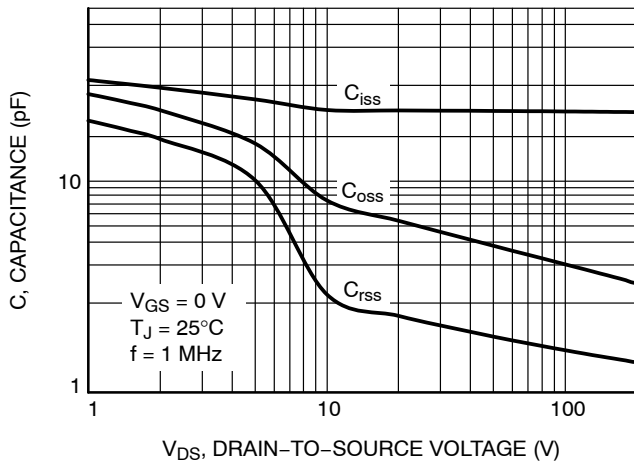


Figure 7. Capacitance Variation

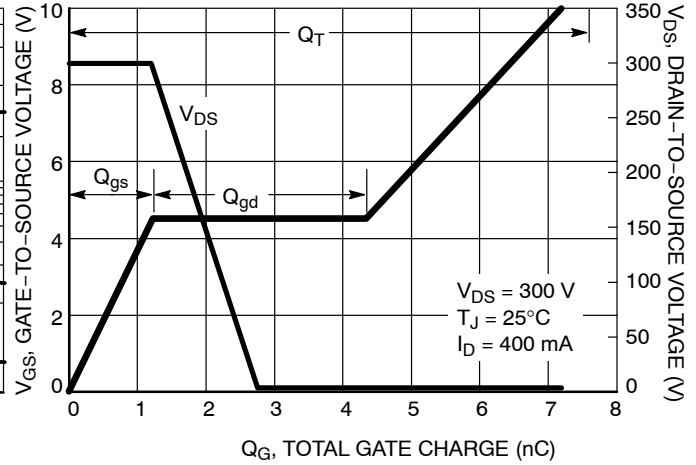


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

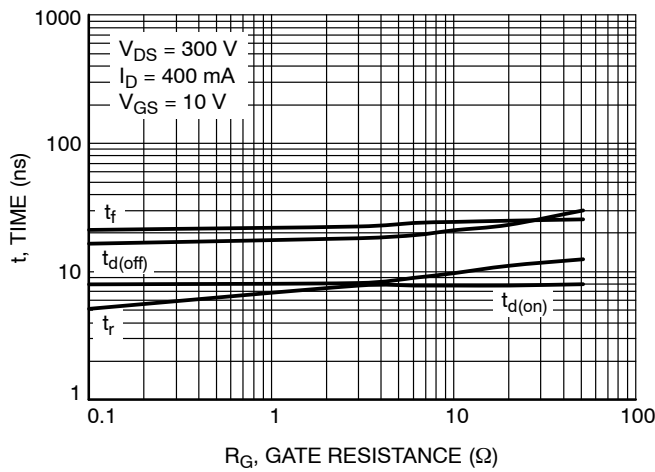


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

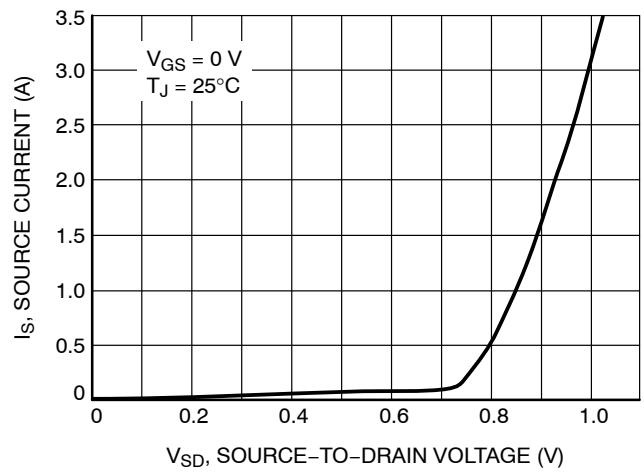


Figure 10. Diode Forward Voltage vs. Current

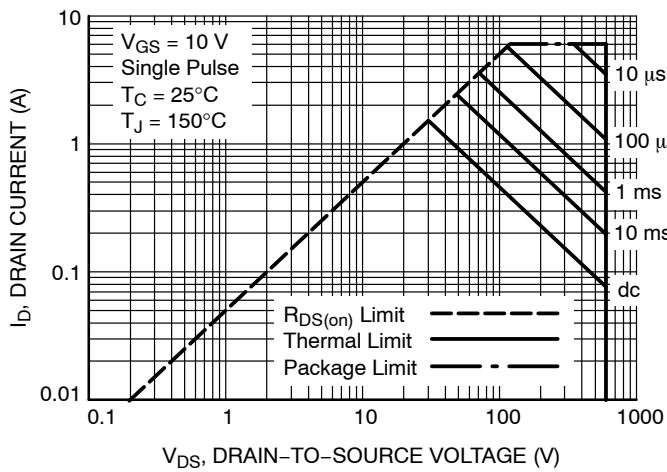


Figure 11. Maximum Rated Forward Biased Safe Operating Area NDD01N60

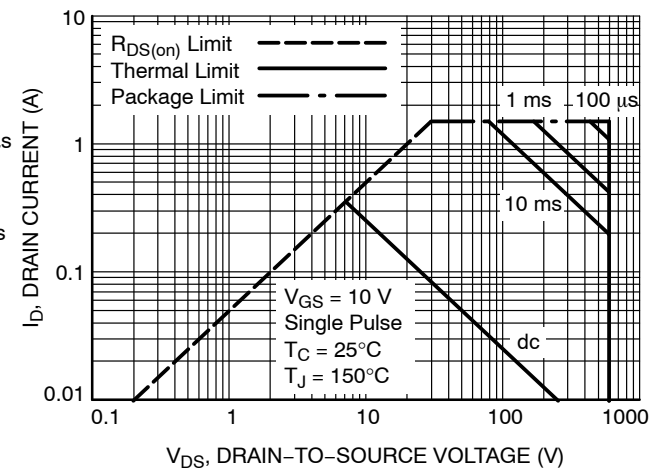


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDT01N60

NDD01N60, NDT01N60

TYPICAL CHARACTERISTICS

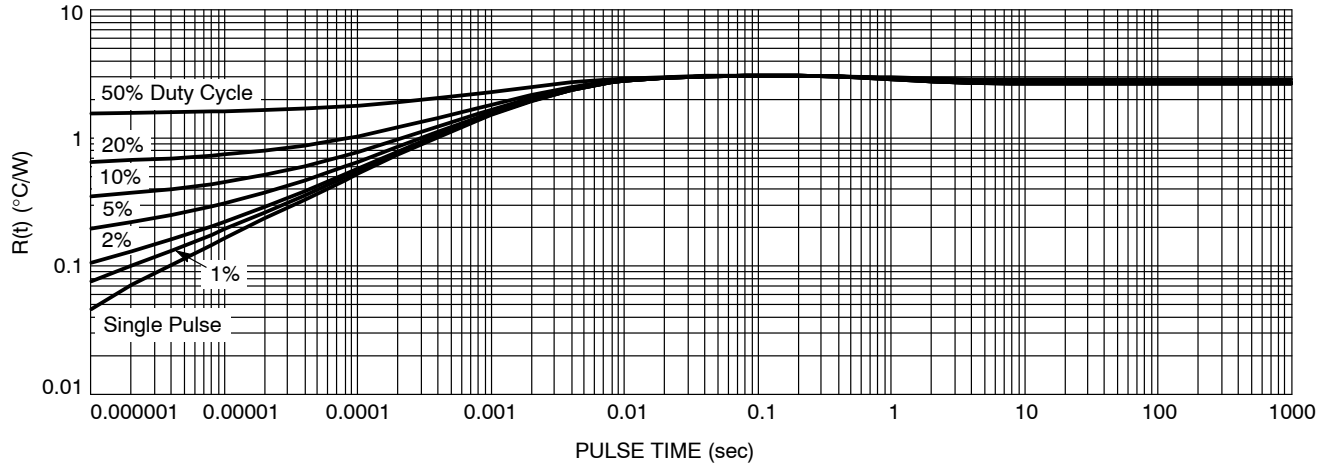


Figure 13. Thermal Impedance (Junction-to-Case) for NDD01N60

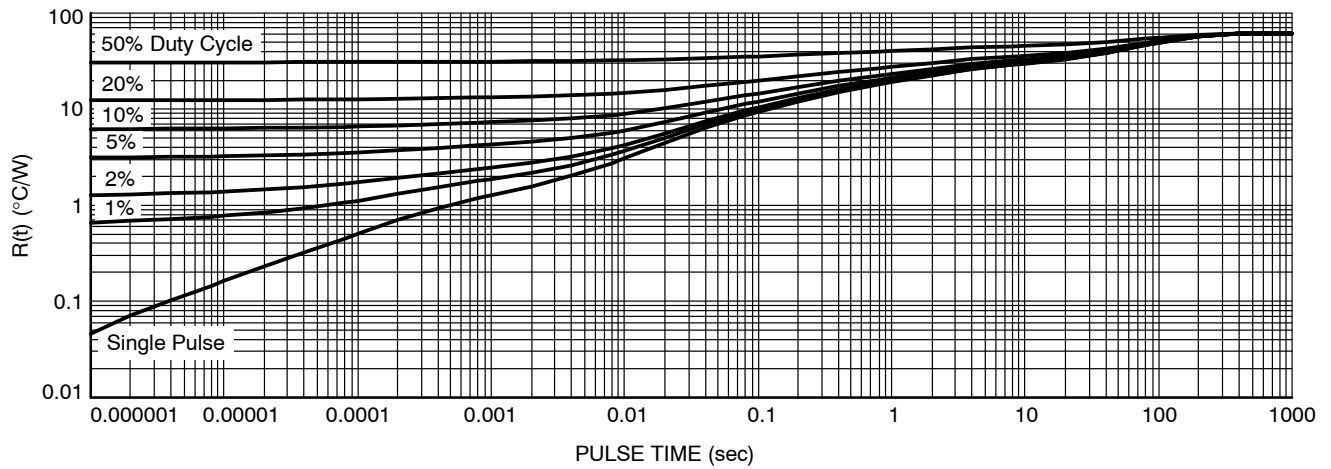


Figure 14. Thermal Impedance (Junction-to-Ambient) for NDT01N60

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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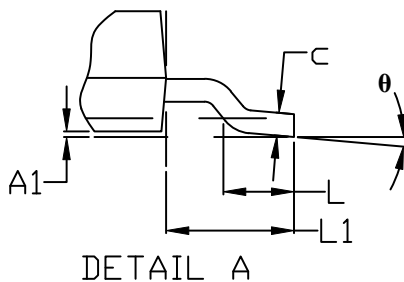
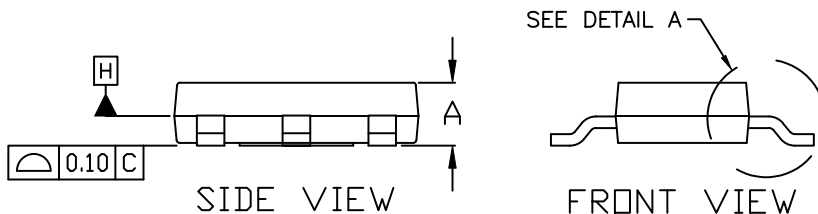
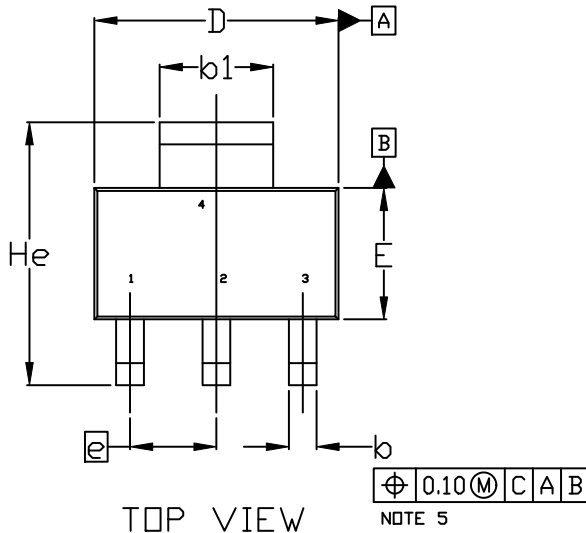
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SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

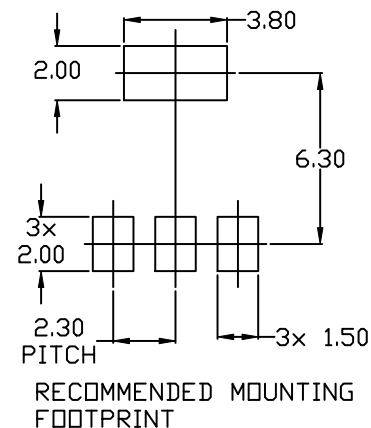
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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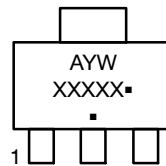
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

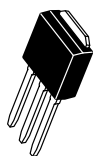
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DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

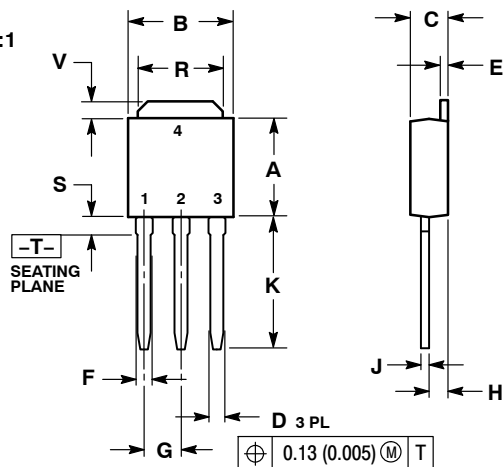
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IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



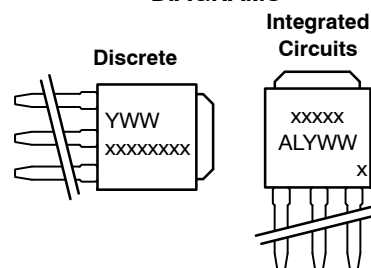
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

MARKING DIAGRAMS

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



xxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

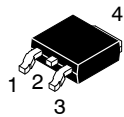
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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

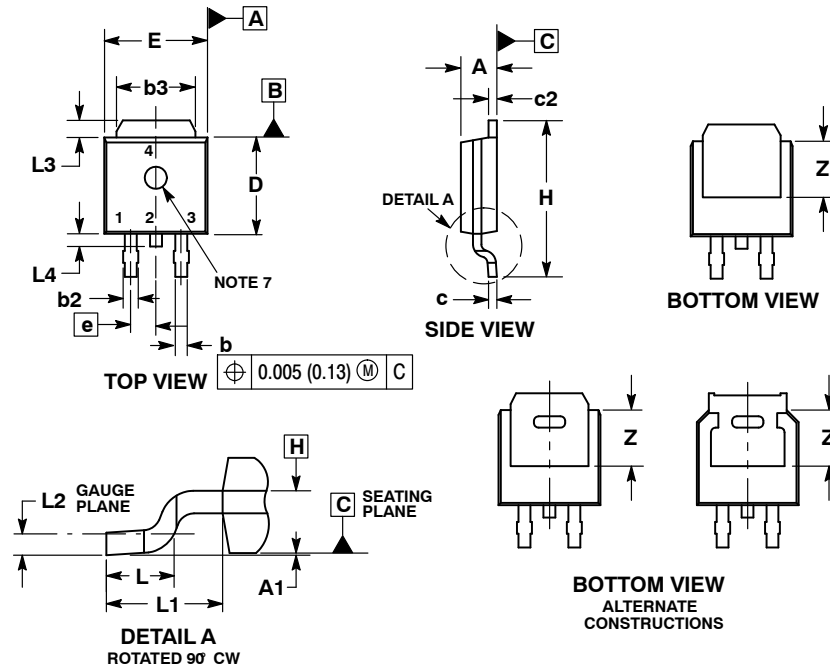
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SCALE 1:1

DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015

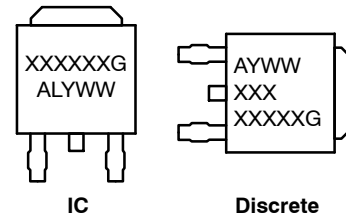


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*

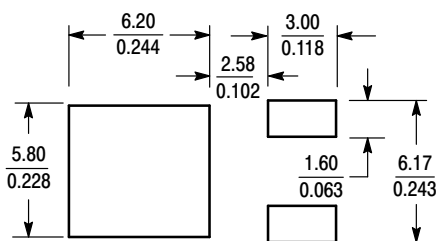


XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- STYLE 1:**
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:**
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:**
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:**
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:**
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:**
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:**
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 8:**
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 9:**
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE
- STYLE 10:**
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

SOLDERING FOOTPRINT*



SCALE 3:1 (mm inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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