NCV459

4 A Single Load Switch for Low Voltage Rail

The NCV459 is a power load switch with very low Ron NMOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a best in class current consumption optimization with NMOS structure, leakage currents are drastically decreased. Offering optimized leakages isolation on the ICs connected on the battery.

Output discharge path is proposed to eliminate residual voltages on the external components connected on output pin.

Proposed in wide input voltage range from 0.75 V to 5.5 V, and a very small DFNW8 3x3 mm, 0.65 pitch package.

Features

- 0.75 V − 5.5 V Operating Range
- 23 mΩ N−MOSFET
- Vbias Rail Input
- DC Current up to 4 A
- Output Auto−Discharge Option
- Active High EN Pin
- DFNW8, 3 x 3 mm, 0.65 pitch

Typical Applications

- ADAS System
- Camera Module
- Power Management

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MARKING DIAGRAM



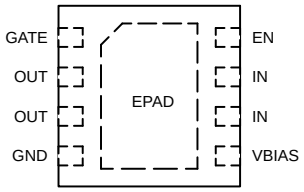
DFNW8
CASE 507AB



45A	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

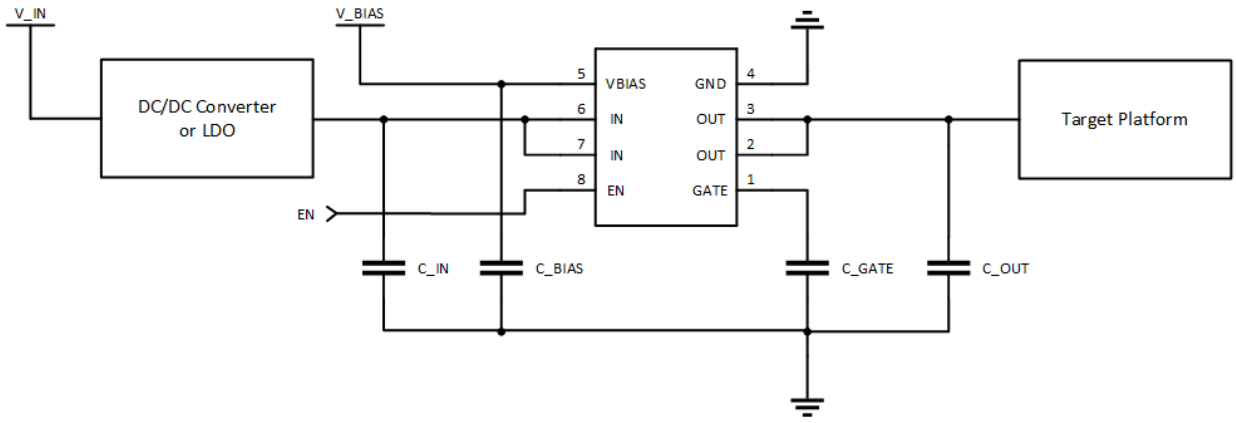


Figure 1. Typical Application Schematic

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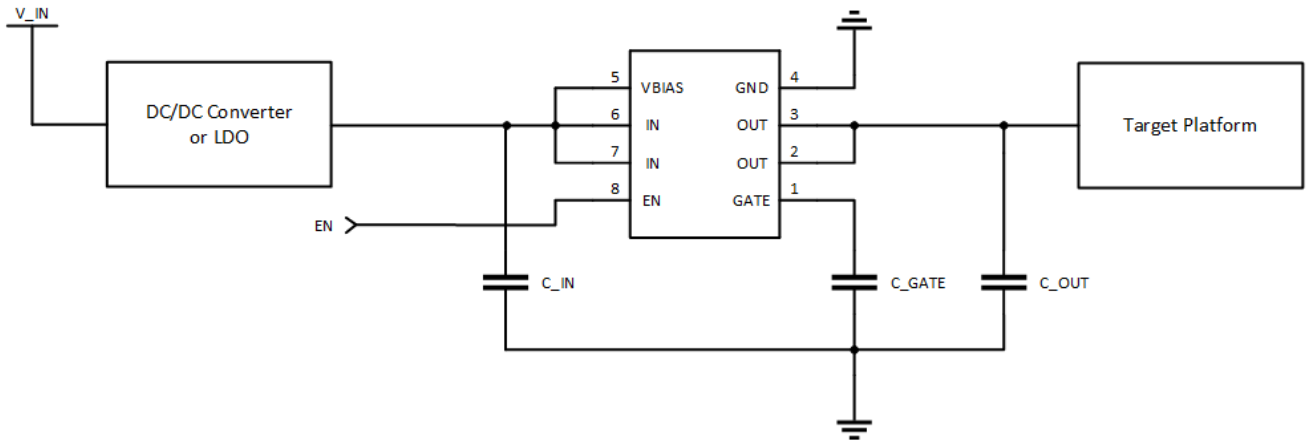


Figure 2. Application Schematic with Vbias Connected to IN

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
GATE	1	INPUT	OUT pin slew rate control (t_{rise}).
OUT	2, 3	POWER	Load−switch output pin.
GND	4	POWER	Ground connection.
VBIAS	5	POWER	External supply voltage input.
IN	6, 7	POWER	Load−switch input pin.
EN	8	INPUT	Enable input, logic high turns on power switch.
EPAD	9	POWER	Exposed pad, connect to ground potential.

BLOCK DIAGRAMS

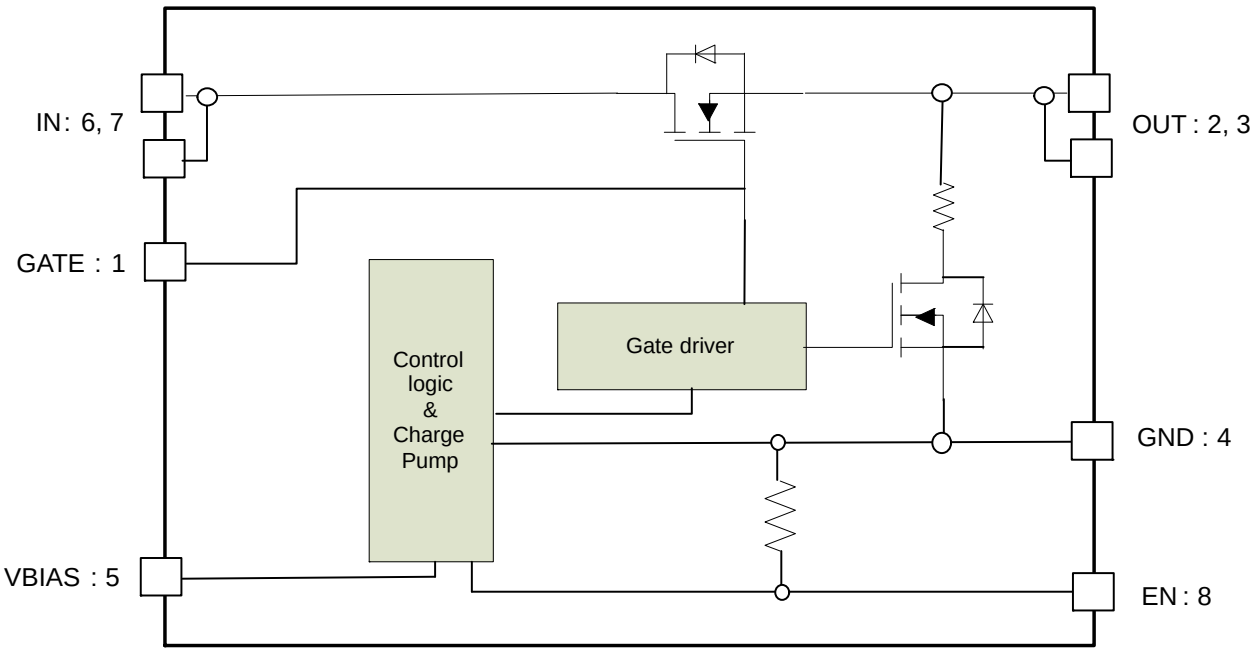


Figure 3. NCV459 Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, VBIAS, GATE Pins: (Note 1)	V_{EN}, V_{IN} , V_{OUT}, V_{BIAS}, V_{GATE}	−0.3 to +6.5	V
From IN to OUT Pins: Input/Output (Note 1)	V_{IN} , V_{OUT}	0 to + 6.5	V
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	2000	V
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard:
   JESD22−A114 for all pins.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply		0.75		5.5	V
V_{EN}	Enable Voltage		0		5.5	V
V_{BIAS}	Bias voltage ($V_{BIAS} \geq$ best of V_{IN}, V_{OUT})		1.2		5.5	V
T_A	Ambient Temperature Range		−40	25	+105	°C
C_{IN}	Decoupling input capacitor		100			nF
C_{OUT}	Decoupling output capacitor		100			nF
$R_{\theta JA}$	Thermal Resistance Junction to Air	DFNW8 (Note 4)		106		°C/W
I_{OUT}	DC current			4	4.5	A
	AC current 1 ms @ 217 Hz				5	A
	AC current 100 μs spike				15	A
P_D	Power Dissipation Rating (Note 5)			0.18		W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Value based on 1s0p board with copper 650 mm^2 (or 1 in^2) of 1 oz thickness and FR4 PCB substrate
5. The maximum power dissipation (PD) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J between −40°C to +125°C for V_{IN} between 0.75 V and 5.5 V, and V_{BIAS} between 1.2 V and 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C, V_{IN} = 3.3 V and V_{BIAS} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance for each rail	V_{IN} = V_{BIAS} = 5.5 V	I_{OUT} = 200 mA, T_A = 25°C		23	60	mΩ
			T_J = 125°C			80	
		V_{IN} = V_{BIAS} = 3.3 V	I_{OUT} = 200 mA, T_A = 25°C		23	60	
			T_J = 125°C			80	
		V_{IN} = V_{BIAS} = 1.8 V	I_{OUT} = 200 mA, T_A = 25°C		23	60	
			T_J = 125°C			80	
		V_{IN} = V_{BIAS} = 1.5 V	I_{OUT} = 200 mA, T_A = 25°C		23	60	
			T_J = 125°C			80	
		V_{IN} = V_{BIAS} = 1.2 V	I_{OUT} = 200 mA, T_A = 25°C		24	60	
			T_J = 125°C			80	
		V_{IN} = 1.0 V V_{BIAS} = 1.2 V	I_{OUT} = 200 mA, T_A = 25°C		24	60	
			T_J = 125°C			80	
		V_{IN} = 0.8 V V_{BIAS} = 1.2 V	I_{OUT} = 200 mA, T_A = 25°C		24	60	
			T_J = 125°C			80	
R_{DIS}	Output discharge path		EN = low		230	300	Ω
TIMINGS (Note 6)							
T_R	Output rise time From 10% to 90% of V_{OUT}	V_{IN} = 5 V C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω	No cap on GATE pin		0.26		ms
			Gate capacitor = 1 nF		1.5		
			Gate capacitor = 10 nF		15		
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}		Without Cgate		10		μs
			With 1 nF on Gate		60		μs
T_F	Fall Time. From 90% to 10% of V_{OUT}				50		μs
Tdis	Disable time		From EN to 90% Vout		75		μs
T_R	Output rise time From 10% to 90% of V_{OUT}	V_{IN} = 3.3 V C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω	No cap on GATE pin		0.25	0.5	ms
			Gate capacitor = 1 nF		1		
			Gate capacitor = 10 nF		10		
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}		Without Cgate		20	50	μs
			With 1 nF on Gate		114		μs
T_F	Output fall time From 90% to 10% of V_{OUT}				60	120	μs
T_R	Output rise time From 10% to 90% of V_{OUT}	V_{IN} = 1.8 V C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω	No cap on GATE pin		0.12		ms
			Gate capacitor = 1 nF		0.6		
			Gate capacitor = 10 nF		5.5		
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}		Without Cgate		15		μs
			With 1 nF on Gate		85		μs
T_F	Output fall time From 90% to 10% of V_{OUT}				35		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J between −40°C to +125°C for V_{IN} between 0.75 V and 5.5 V, and V_{BIAS} between 1.2 V and 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C, V_{IN} = 3.3 V and V_{BIAS} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TIMINGS (Note 6)							
T_R	Output rise time From 10% to 90% of V_{OUT}	V_{IN} = 1 V, C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω	No cap on GATE pin		0.01		ms
			Gate capacitor = 1 nF		1		
			Gate capacitor = 10 nF		13		
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}	V_{IN} = 1 V, C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω	Without Cgate		10		μs
			With 1 nF on Gate		0.4		ms
T_F	Output fall time				20		μs
Logic							
V_{IH}	High−level input voltage			0.9			V
V_{IL}	Low−level input voltage					0.4	V
R_{EN}	Pull down resistor			3		7	MΩ
QUIESCENT CURRENT							
I_{VBIAS}	V_{BIAS} Quiescent current	V_{BIAS} = 3.3 V, EN = high			1.3	5	μA
I_{INQ}	IN Quiescent current	EN = high			0.01	0.3	μA
I_{STBIN}	Standby current IN	EN = low, IN standby current, V_{IN} = 3.3 V, with discharge path, T_A = −40°C to 85°C			0.01	0.5	μA
$I_{STDVbias}$	Standby current V_{BIAS}	V_{BIAS} = 3.3 V EN = low, T_A = −40°C to 85°C			0.4	1.5	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

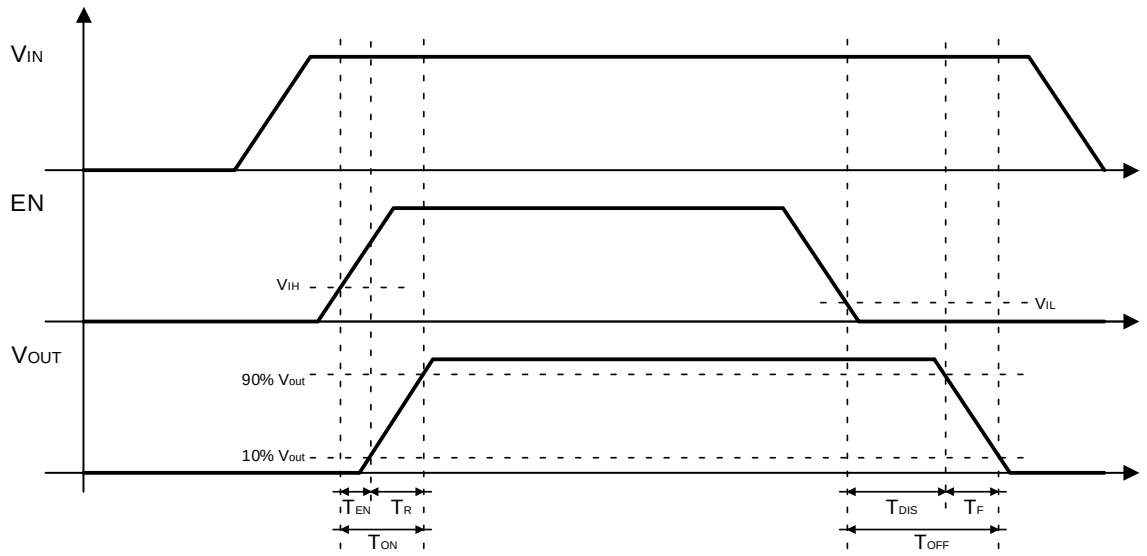


Figure 4. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

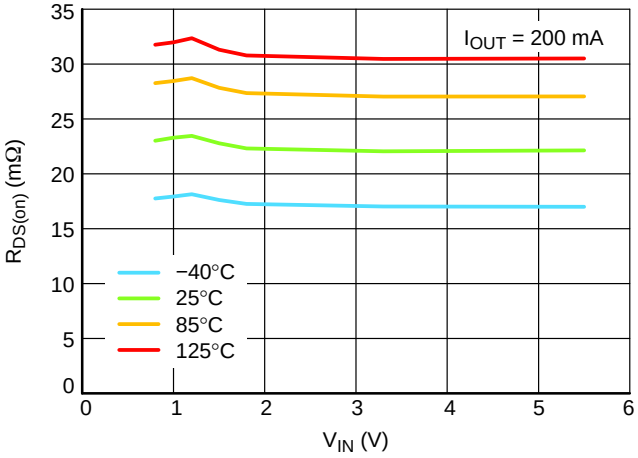


Figure 5. $R_{DS(on)}$ vs. V_{IN}, Multi Junction Temperature

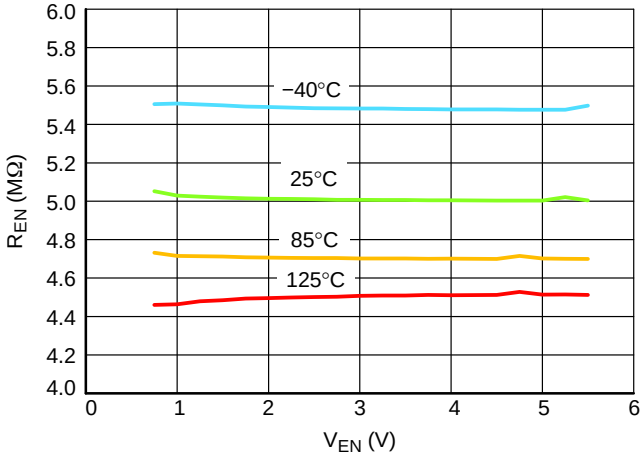


Figure 6. Pull Down Resistor vs. V_{EN}, Multi Junction Temperature

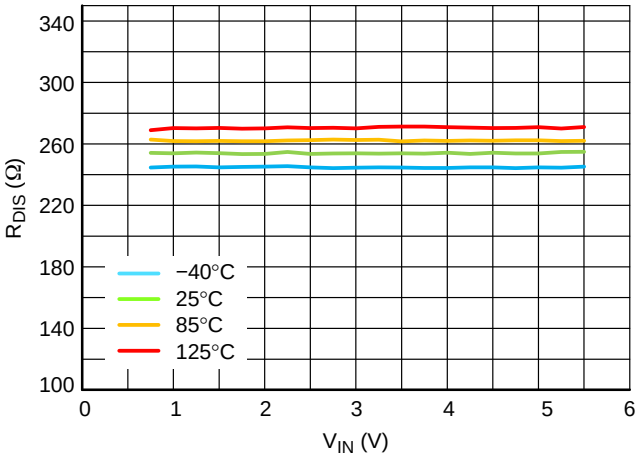


Figure 7. Output Discharge Resistor vs. V_{IN}, Multi Junction Temperature

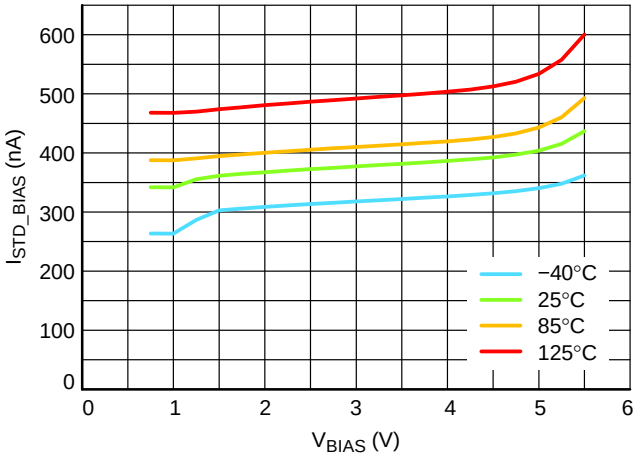


Figure 8. BIAS Standby Current vs. V_{BIAS}, Multi Junction Temperature

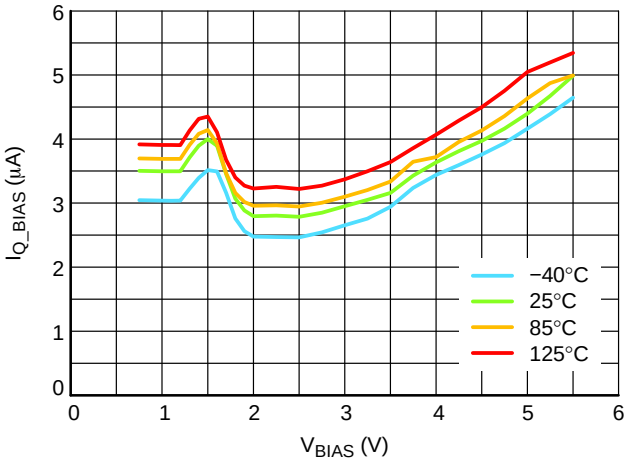


Figure 9. BIAS Quiescent Current vs. V_{BIAS}, Multi Junction Temperature

TYPICAL CHARACTERISTICS

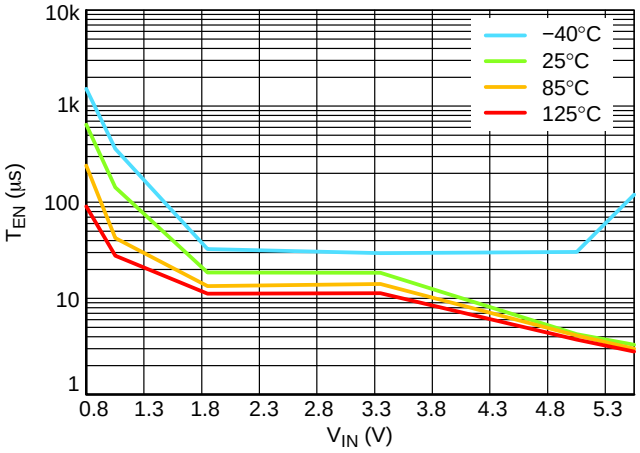


Figure 10. Enable Time vs. V_{IN}, Multi Junction Temperature (without Cgate)

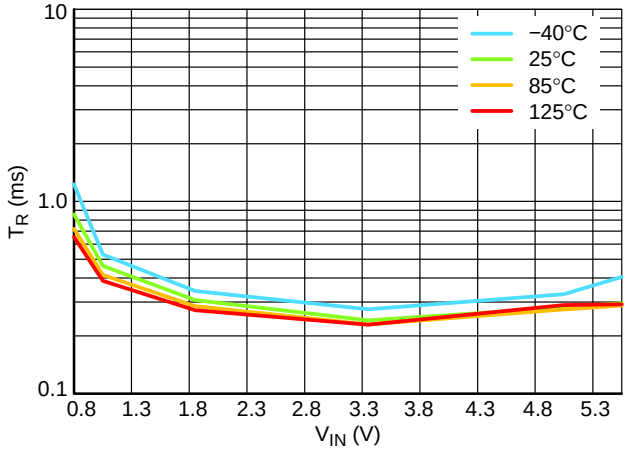


Figure 11. Rise Time vs. V_{IN}, Multi Junction Temperature (without Cgate)

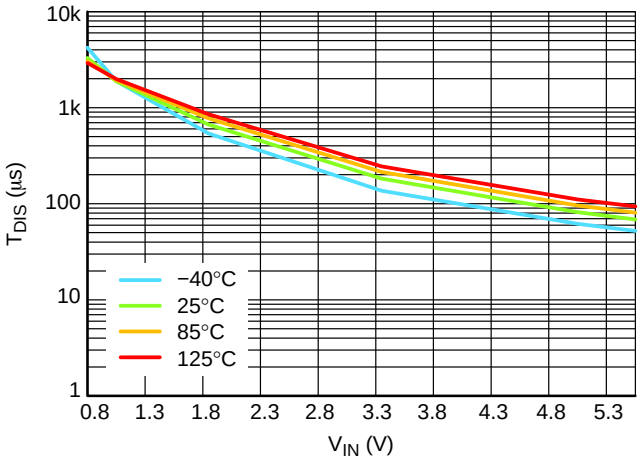


Figure 12. Disable Time vs. V_{IN}, Multi Junction Temperature, V_{BIAS} and V_{IN} Tied Together

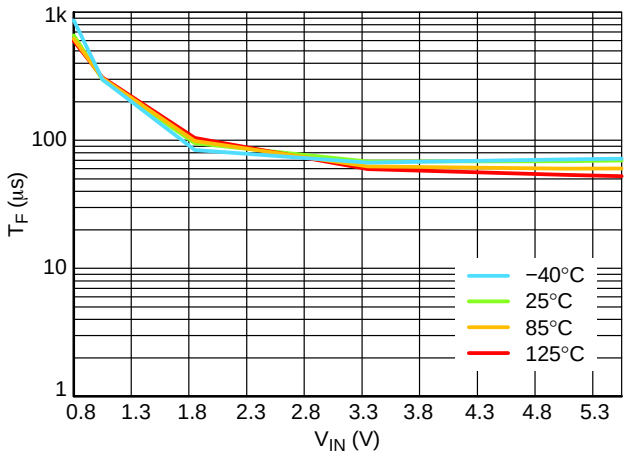


Figure 13. Fall Time vs. V_{IN}, Multi Junction Temperature, V_{BIAS} and V_{IN} Tied Together R_{load} 25 Ω

FUNCTIONAL DESCRIPTION

Overview

The NCV459 are high side N channel MOSFET power distribution switch designed to isolate ICs connected on the LDO or DCDC supplies in order to save energy. The part can be used with a wide range of supply from 0.75 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing NMOS switch off.

The IN/OUT path is activated with a minimum of V_{BIAS} min, Vin min and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at R_{DIS} value.

Vbias Rail

The core of the IC is supplied thanks to Vbias supply rail (common +5 V, 3.3 V, 1.8 V, 1.2 V). Indeed, no current consumption is used on IN pin, allowing to improve power saving of the rail that must be isolated by the power switch.

If Vbias rail is not available or used, Vbias pin and Vin pin can be connected together as close as possible the DUT. A minimum of 1.2 V is necessary to control the IC. It is recommended to connect external capacitor 10 μF due to better EMC immunity.

Output rise time − Gate control

The NMOS is control with internal charge pump and driver. A minimum gate slew rate is internally set to avoid huge inrush current when EN is set from low to high. The default gate slew rate depends on Vin level. The higher Vin level, the longer rise time.

In addition, an external capacitor can be connected between Gate pin and GND in order to slow down the gate rising. See electrical table for more details.

Cin and Cout Capacitors

100 nF external capacitors must be connected as close as possible the DUT for noise immunity and better stability. In case of input hot plug (input voltage connected with fast slew rate − few μs − it’s strongly recommended to avoid big capacitor connected on the input. That allows to avoid input over voltage transients.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2 \quad \text{(eq. 1)}$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A \quad \text{(eq. 2)}$$

T_J = Junction temperature (°C
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCV459NMWTBG	45A	Auto Discharge 230 Ω	DFNW8 3 x 3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

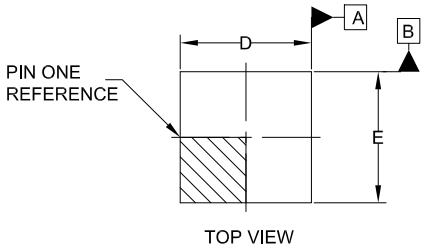
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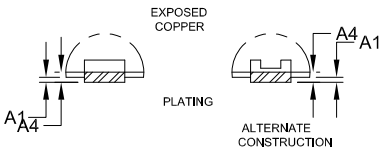
SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E

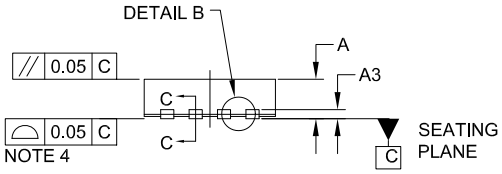
DATE 02 JUL 2021



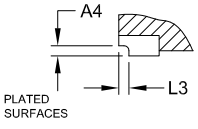
TOP VIEW



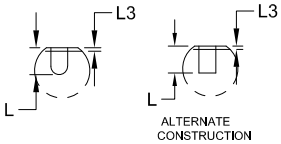
DETAIL B



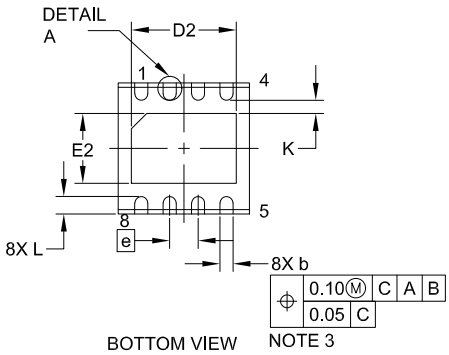
SIDE VIEW



SECTION C-C



DETAIL A

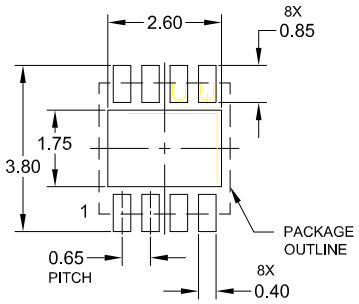


BOTTOM VIEW

NOTES:

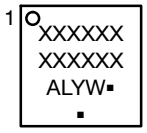
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	—	---	0.05
A3		0.20 REF	
A4	0.10	---	—
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
e		0.65 BSC	
K		0.30 REF	
L	0.35	0.40	0.45
L3	0.00	0.05	0.10



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW8 3x3, 0.65P	PAGE 1 OF 1

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