NCP340

Soft-Start Controlled Load Switch

The NCP340 is a low Ron N−channel MOSFET controlled by a soft−start sequence of 2 ms for mobile applications.

The very low $R_{DS(on)}$ allows system supplying or battery charging up to DC 3A.The device is enable automatically if a Power Supply is connected on Vin pin (active High) and maintained off if no Vin (internal pull down).

Due to a current consumption optimization, leakage current is drastically decreased from the battery connected to the device, allowing long battery life.

Features

- 1.8 V – 5.5 V Operating Range
- 30 mΩ N−MOSFET
- DC Current Up to 3 A
- Built−in Soft−Start 2 ms
- Reverse Voltage Protection
- Active High with Integrated Bridge
- Compliance to IEC61000−4−2 (Level 4)
  8.0 kV (Contact)
  15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 3
- µDFN4 1.2 x 1.6 mm
- This is a Pb−Free Device

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Computers

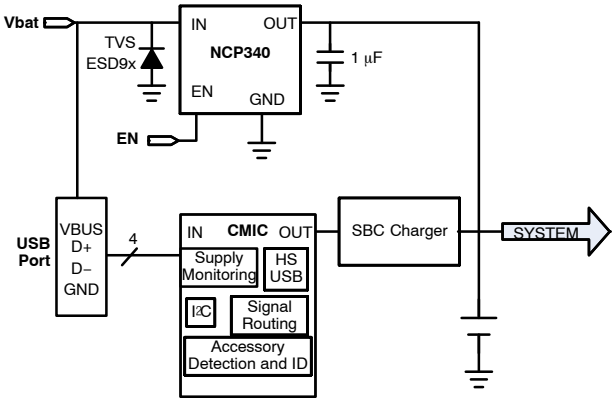


Figure 1. Typical Application Circuit

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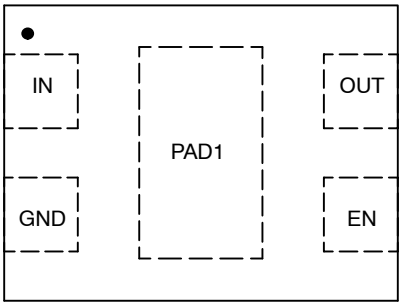
UDFN4
CASE 517CE

MARKING DIAGRAM



34 = Specific Device Code
M = Date Code

PINOUT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	1	POWER	Power−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	2	POWER	Ground connection;
EN	3	INPUT	Enable input, logic high turns on power switch.
OUT	4	OUTPUT	Power−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.
PAD1		POWER	Exposed pad can be connected to GND plane for dissipation purpose or any other thermal plane.

BLOCK DIAGRAM

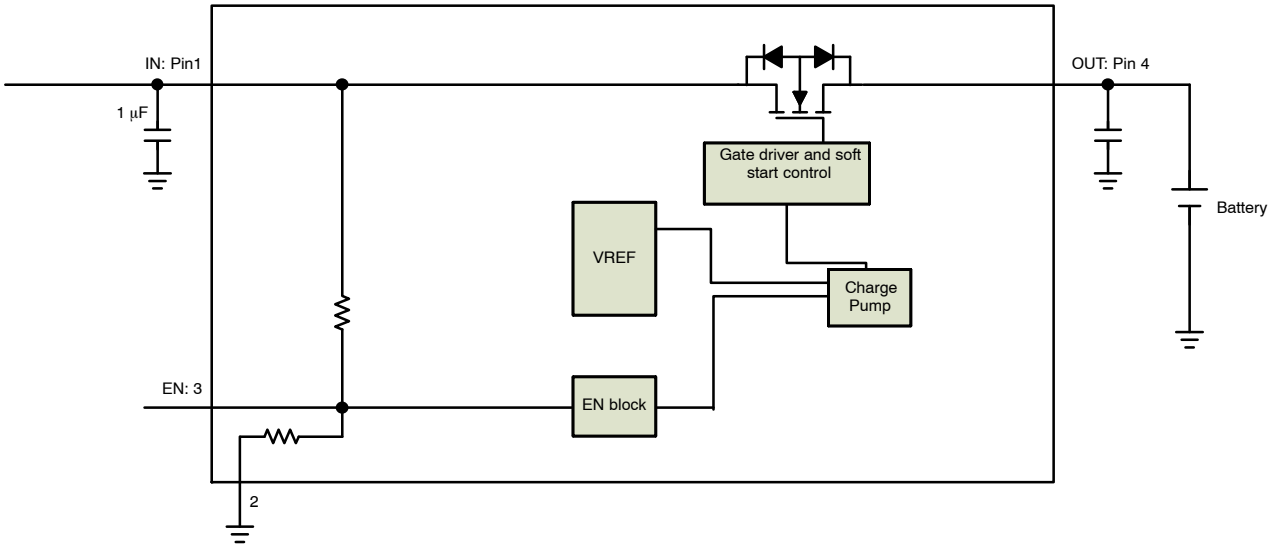


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins:	V_{EN} , V_{IN} , V_{OUT}	−0.3 to + 7.0	V
From IN to OUT Pins: Input/Output	V_{IN} , V_{OUT}	−7.0 to + 7.0	V
ESD Withstand Voltage (IEC 61000−4−2) (Note 1) (IN and OUT when bypassed with 1.0 μF capacitor minimum)	ESD IEC	15 Air, 8 contact	kV
Human Body Model (HBM) ESD Rating are (Notes 2 and 3)	ESD HBM	8000	V
Machine Model (MM) ESD Rating are (Notes 2 and 3)	ESD MM	250	V
Latch−up protection (Note 4) − Pins IN, OUT, EN	LU	100	mA
Maximum Junction Temperature Range	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Guaranteed by design.
2. According to JEDEC standard JESD22−A108.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.8		5.5	V
V_{EN}	Enable Voltage			0		5.5	
T_A	Ambient Temperature Range			− 40	25	+ 85	°C
T_J	Junction Temperature Range			− 40	25	+ 125	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor	USB port per Hub		1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	UDFN4 package (Note 6)			170		°C/W
I_{OUT}	Maximum DC current	UDFN4 package				3	A
I peak	Maximum Peak current	100 μs pulse				15	A
P_D	Power Dissipation Rating (Note 7)	$T_A \le 25°C$	UDFN4 package		0.58		W
		$T_A = 85°C$	UDFN4 package		0.225		

6. The $R_{\theta JA}$ is dependent of the PCB heat dissipation.
7. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125 °C for $_{VIN}$ between 1.8 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and $_{VIN}$ = 5 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 3 V, V_{IN} = 5 V	T_J = 25°C		26		mΩ
			−40°C < T_J < 125°C			50	
T_R	Output rise time	V_{IN} = 5 V	C_{LOAD} = 1 μF, R_{LOAD} = 125 Ω (Note 8)	0.5	2	4	ms
T_F	Output fall time	V_{IN} = 5 V	C_{LOAD} = 100 μF, R_{LOAD} = 40 Ω (Note 8)		4		ms
T_{on}	Gate turn on	V_{IN} = 5 V	From Vin applied to V_{OUT} = 10% of fully on	0.5	2	4	ms
		V_{IN} = 3 V	From Vin applied to V_{OUT} = 10% of fully on (Note 9)			3	
ENABLE INPUT EN							
V_{IH}	High−level input voltage			1.15			V
V_{IL}	Low−level input voltage					0.85	V
R_{pd}	En pull−down resistor				1		MΩ
R_{pu}	En pull−up resistor				1.5		MΩ
REVERSE−LEAKAGE PROTECTION							
I_{REV}	Reverse−current protection	V_{IN} = 0 V, V_{out} = 4.2 V (part disable), T_J = 25°C			0.15	1	μA
QUIESCENT CURRENT							
Iq	Current consumption	No load			100	200	μA

8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.
9. Guaranteed by characterization.

TYPICAL CHARACTERISTICS

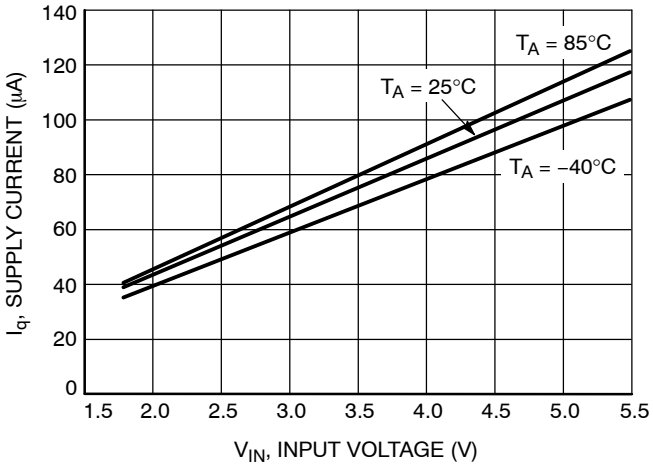


Figure 3. Supply Current vs. Voltage

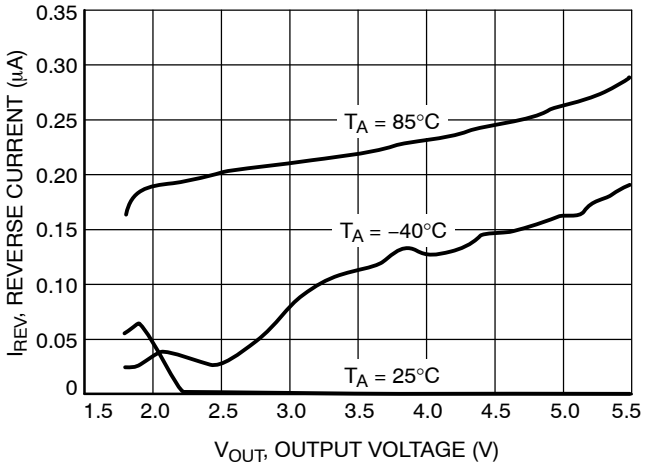


Figure 4. Reverse Current vs. Output Voltage

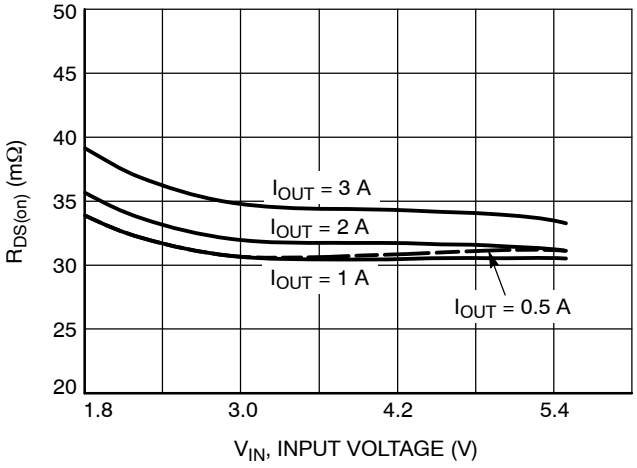


Figure 5. $R_{DS(on)}$ vs. V_{IN} Voltage at 25°C

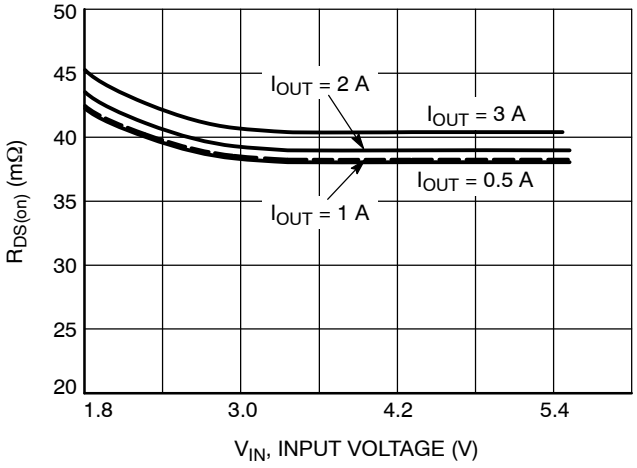


Figure 6. $R_{DS(on)}$ vs. V_{IN} Voltage at 85°C

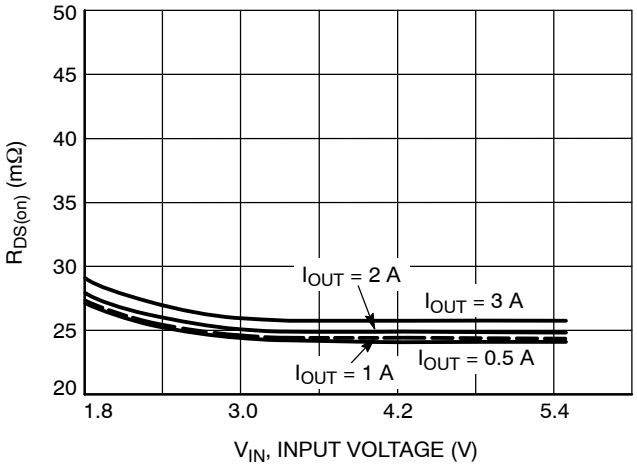


Figure 7. $R_{DS(on)}$ vs. V_{IN} Voltage at −40°C

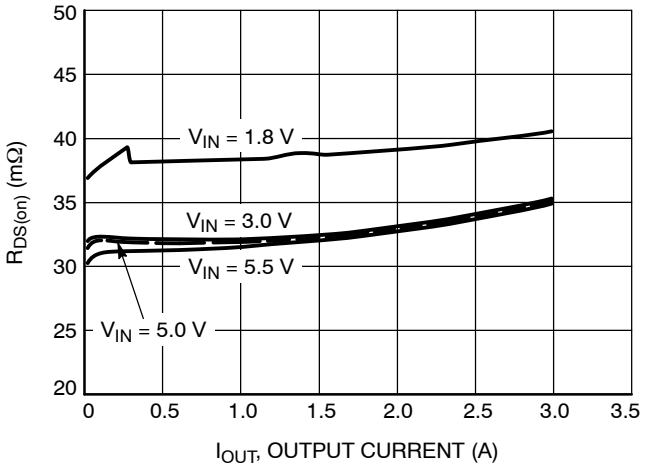


Figure 8. $R_{DS(on)}$ vs. I_{OUT} at 25°C

TYPICAL CHARACTERISTICS

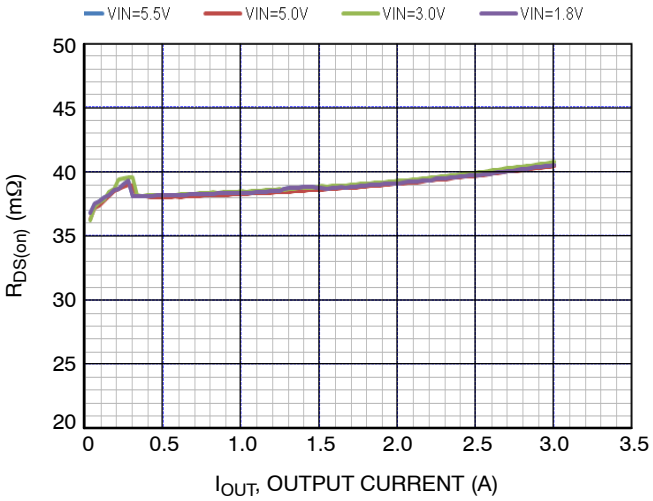


Figure 9. $R_{DS(on)}$ vs. I_{OUT} at 85°C

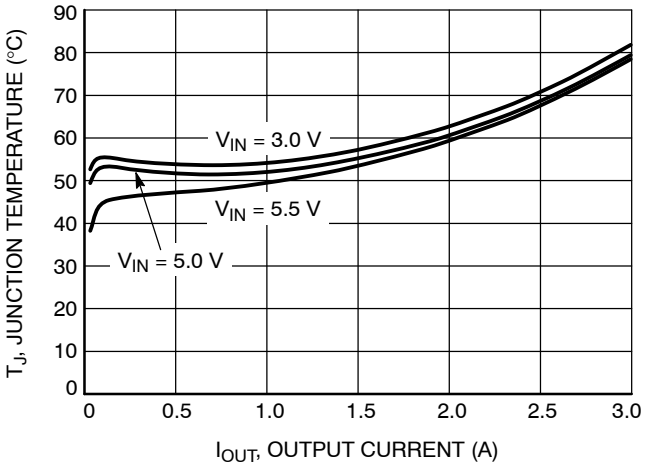


Figure 10. Junction Temperature vs. I_{OUT}

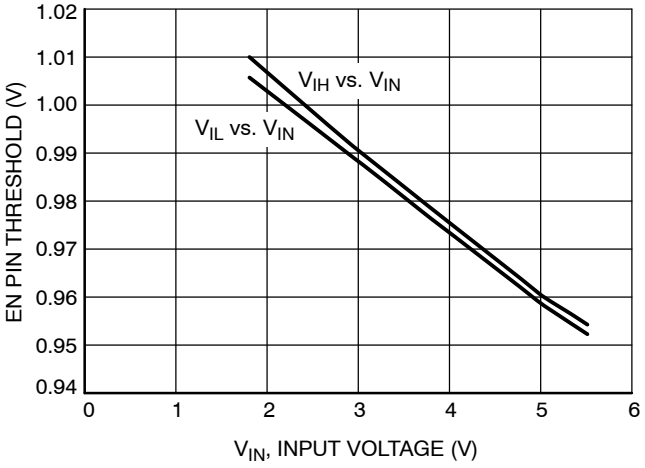


Figure 11. Logic Threshold vs. V_{IN}

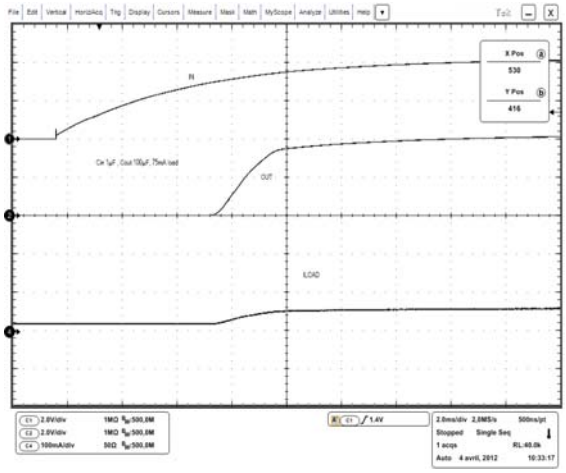


Figure 12. T_{ON} Time on 75 mA Load

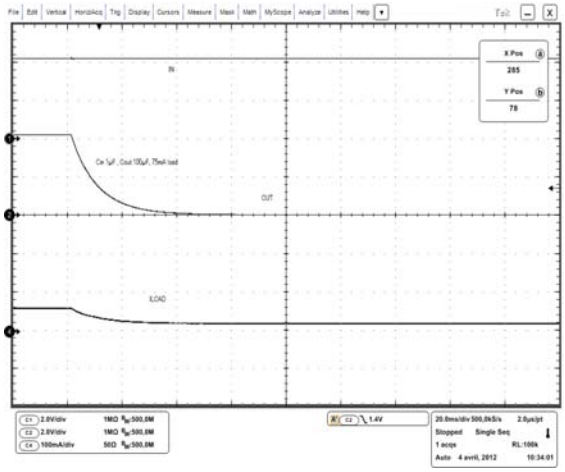


Figure 13. T_{OFF} Time on 75 mA Load

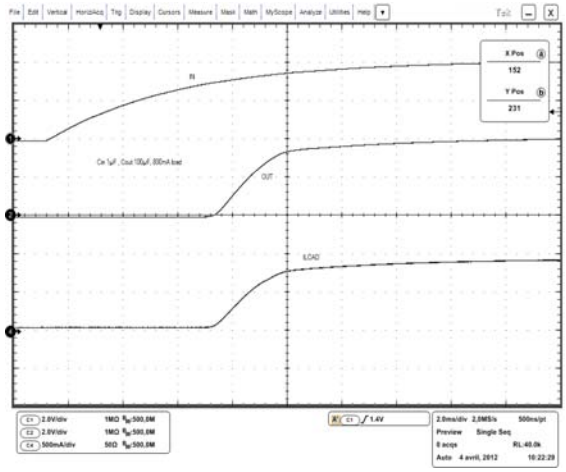


Figure 14. T_{ON} Time on 800 mA Load

TYPICAL CHARACTERISTICS

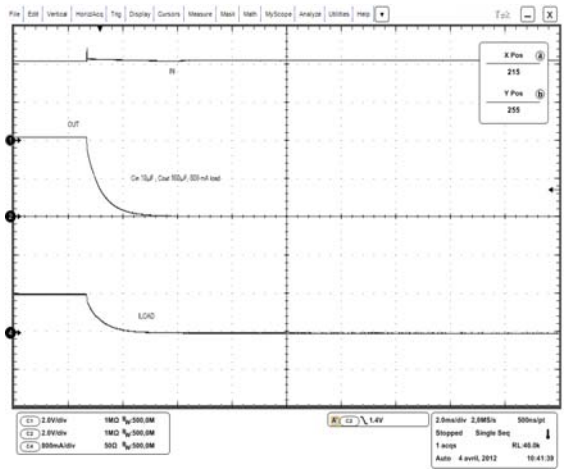


Figure 15. T_{OFF} Time on 800 mA Load

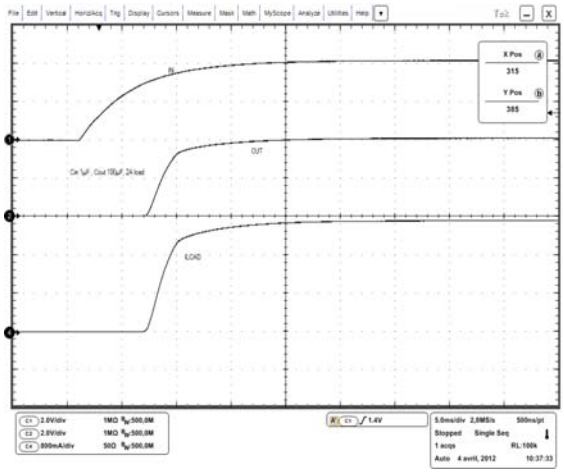


Figure 16. T_{ON} Time on 2 A Load

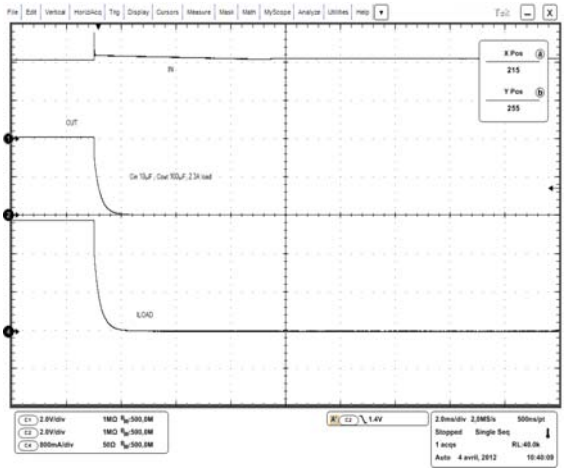


Figure 17. T_{OFF} Time on 2.3 A Load

FUNCTIONAL DESCRIPTION

Overview

The NCP340 is a high side N−channel MOSFET power distribution switch designed to connect external voltage directly to the system. The high side MOSFET is automatically turned on if the Vin voltage is applied thanks to internal pull up connected between Vin and EN pin. The turned off is obtained by Vin removal. Due to the soft start circuitry, NCP340 is able to limit large voltage surges.

Enable input

Enable pin is an active high. The part is off when Vin is not present, limiting current consumption from battery to OUT pin.

In the other side, the part is automatically turned on when V_{IN} is applied.

Blocking Control

The blocking control circuitry switches the bulk of the power NMOS. When the part is off (No V_{IN} or EN tied to GND externally) , the body diode limits the leakage current I_{REV} from OUT to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUT pin. In operating condition, anode of the body diode is connected to OUT pin and cathode is connected to IN pin preventing the discharge of the power supply.

Cin Capacitor

A IN capacitor, 1 μF, at least, capacitor must be placed as close as possible the part to be Compliant with IEC61000−4−2 (Level 4).

Cout Capacitor

Depending on the sinking current during system start up and system turn off, a capacitor must be placed on the output. A 1 μF is strongly recommended but can be decreased down to 100 nF if the above two sequences are well controlled and parasitic inductance connected on the Vout line is negligible.

APPLICATION INFORMATION

Power Dissipation

The device's junction temperature depends on different contributor factor such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)

$R_{DS(on)}$ = Power MOSFET on resistance (Ω)

I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C

$R_{\theta JA}$ = Package thermal resistance (°C/W)

T_A = Ambient temperature (°C)

PCB Recommendations

The NCP340 integrates an up to 3 A rated NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The μDFN4 PAD1 must be connected to ground plane to increase the heat transfer if necessary. By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP340MUTBG	34	μDFN4, 1.2x1.6 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

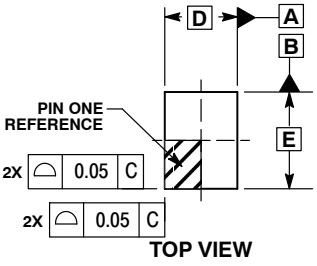
ON Semiconductor®

UDFN4 1.2x1.6, 0.5P
CASE 517CE
ISSUE B

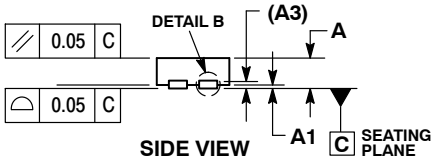
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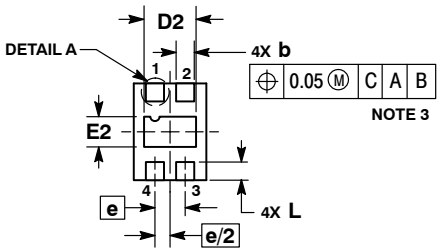
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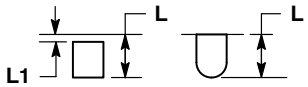
TOP VIEW



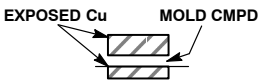
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3		0.13 REF	
b	0.25	0.30	0.35
D		1.20 BSC	
D2	0.76	0.86	0.96
E		1.60 BSC	
E2	0.40	0.50	0.60
e		0.50 BSC	
L	0.20	0.30	0.40
L1	---	---	0.15

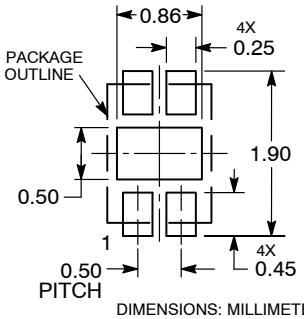
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN4, 1.2X1.6, 0.5P**	**PAGE 1 OF 1**

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