NCP3135

Integrated Synchronous Buck Converter

5 A

NCP3135 is a fully integrated synchronous buck converter for 3.3 V and 5 V step−down applications. It can provide up to 5 A DC load and 6 A instantaneous load current. NCP3135 supports high efficiency, fast transient response and provides power good indicator. The control scheme includes two operation modes: FCCM and automatic CCM/DCM. In automatic CCM/DCM mode, the controller can smoothly switch between CCM and DCM, where converter runs at reduced switching frequency with much higher efficiency. NCP3135 is available in 3 mm x 3 mm QFN−16 pin package.

Features

- High Efficiency in both CCM and DCM
- High Operation Frequency at 1.1 MHz
- Support MLCC Output Capacitor
- Small Footprint, 3 mm x 3 mm, 16−pin QFN Package
- Up to 5 A Continuous Output Current
- 6 A Instantaneous Load Current
- 2.9 V to 5.5 V Wide Conversion Voltage Range
- Output Voltage Range from 0.6 V to 0.84 X Vin
- Internal 1 ms Soft−Start
- Automatic Power−Saving Mode
- Voltage Mode Control
- Support Pre-bias Start−up Functionality
- Output Discharge Operation
- Over−Temperature Protection
- Built−in Over−Voltage, Under−Voltage and Over-Current Protection
- Power Good Indicator
- This is a Pb−Free Device

Applications

- 5 V Step Down Rail
- 3.3 V Step Down Rail

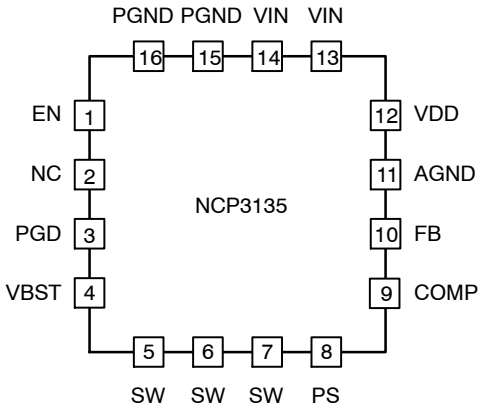
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QFN16 3 x 3, 0.5P
CASE 485DA

SUGGESTED PIN ARRANGEMENT



MARKING DIAGRAM



3135	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 12 of this data sheet.

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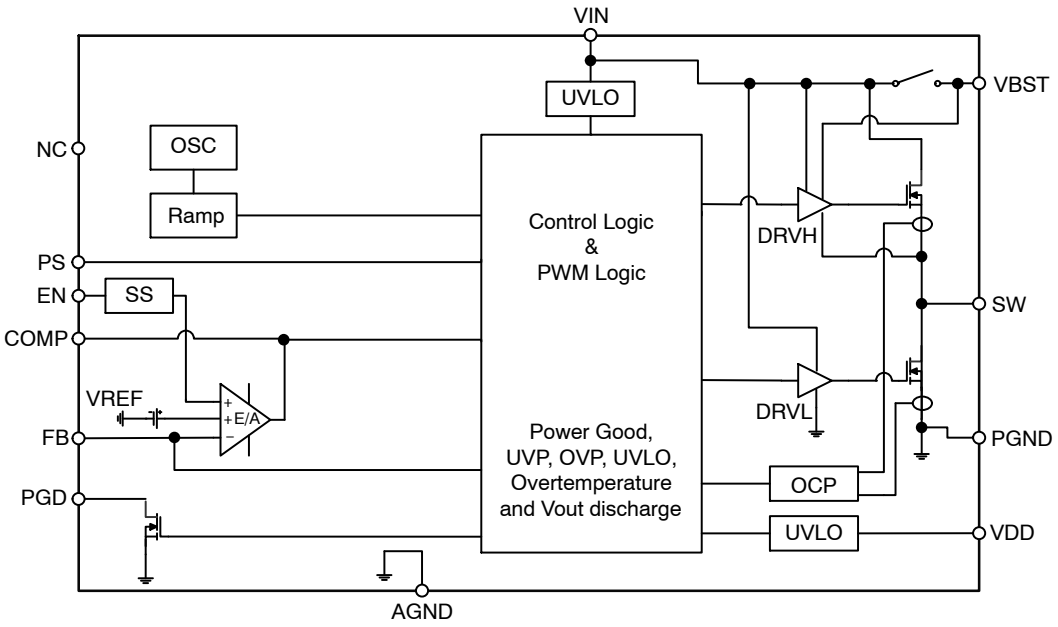


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin No.	Symbol	Description
1	EN	Logic control to enabling the switcher. Internally pulled up to VDD with a 1.35 MΩ resistor
2	NC	Not connected
3	PGD	Open drain power good output
4	VBST	Gate drive voltage for high side FET. Connect capacitor from this pin to SW
5, 6, 7	SW	Switch node between high−side MOSFET and low−side MOSFET
8	PS	Mode configuration pin (with 10 μA current): Pulled high or floating (internally pulled high): Forced Continuous Conduction Mode Connect with resistor equal to or lower than (≤)174 kΩ to GND: Automatic CCM/DCM
9	COMP	Output of the error amplifier
10	FB	Feedback pin. Connect to resistor divider to set up the desired output voltage
11	AGND	Analog ground
12	VDD	Power supply input for control circuitry
13, 14	VIN	Power input for power conversion and gate driver supply
15, 16	PGND	Power ground

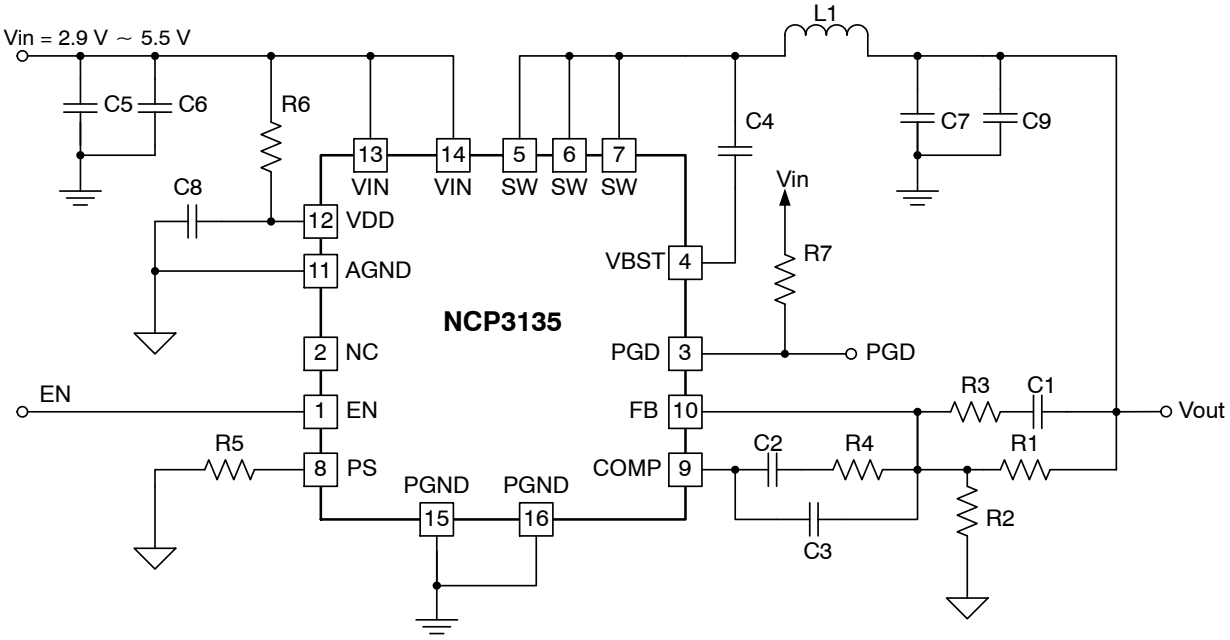


Figure 2. NCP3135 Single Voltage Rail for V_{IN} and V_{DD}

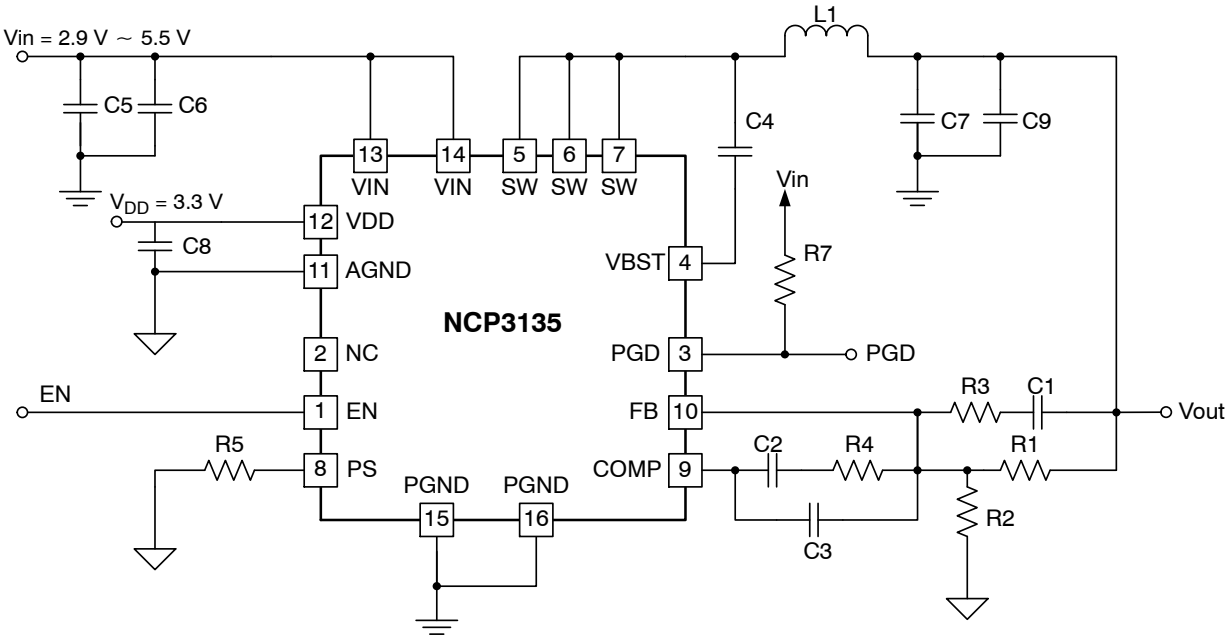


Figure 3. NCP3135 Dual Voltage Rail for V_{IN} and V_{DD}

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol		Value		Units
			Min	Max	
Input Voltage Range	VIN, VDD, PS, EN		−0.3	6.5	V
	VBST		−0.3	17	
	VBST (with respect to SW)		−0.3	6.5	
	FB		−0.3	3.7	
Output Voltage Range	SW	DC	−1	6.5	V
		Pulse < 20 ns, E = 5 μJ	−3	10	
	High−side FET and Low−side FET drain−source voltage	DC		6.5	
		AC, Pulse < 50 ns		7.5	
	PGD		−0.3	6.5	
	COMP		−0.3	6.5	
	PGND		−0.3	0.3	
Operation Ambient Temperature	T_A		−40	125	°C
Storage Temperature	T_S		−55	150	
Junction Temperature	T_J		−40	150	
Electrostatic Discharge	Human Body Model (HBM)		2000		V
	Charged Device Model (CDM)		500		
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATION RATINGS

Rating	Symbol	Value			Units
		Min	Nom	Max	
Input Voltage Range	VIN	2.9		5.5	V
	VDD	2.9		5.5	
	VBST	−0.1		13.5	
	VBST (with respect to SW)	−0.1		6	
	EN	−0.1		3.5	
	FB, PS	−0.1		3.5	
Output Voltage Range	SW	−1		6.5	V
	PGD	−0.1		6	
	COMP	−0.1		3.5	
	PGND	−0.1		0.1	
Junction Temperature range, T_J		−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. THERMAL INFORMATION

Rating	Value	Units
Junction−to−Ambient Thermal Resistance (Note 1)	45	°C/W

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}}$$

Table 5. ELECTRICAL CHARACTERISTICS (V_{DD} = V_{IN} = 3.3 V and V_{DD} = V_{IN} = 5.0 V, T_A = T_J = −40°C to 125°C. Typical values are at T_A = 25°C, PGND = GND unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
VIN operation voltage	V_{IN}	Nominal input voltage range	2.9		5.5	V
VIN UVLO threshold		Ramp up; EN = 'HI'		2.8		V
VIN UVLO hysteresis				130		mV
VDD internal bias voltage		Nominal 3.3 V input voltage range	2.9		5.5	V
VDD UVLO threshold		Ramp up; EN = 'HI'		2.8		V
VDD UVLO hysteresis				75		mV
VOLTAGE MONITOR						
Power good low voltage		Pull−down voltage with 4 mA sink current		200	400	mV
Power good high leakage current			−2.0	0	2.0	μA
Power good threshold		Feedback lower voltage limit	80	83	86	%Vref
		Feedback higher voltage limit	114	117	120	%Vref
Power good high delay	$t_{PGDELAY}$			400		μs
Minimum Vin voltage for valid PGD at start up		Measured at Vin with 1 mA (or 2 mA) sink current on PGD pin at start up		1		V
Output over-voltage protection threshold at FB			114	117	120	%Vref
Over-voltage blanking time	t_{OVPDLY}	Time from FB higher than 20% of Vref to OVP fault	1.0	1.7	2.5	μs
Output under-voltage protection threshold at FB			80	83	86	%Vref
Under-voltage blanking time	t_{UVPDLY}	Time from FB lower than 20% of Vref to UVP fault		11		μs
SUPPLY CURRENT (T_J = +25°C)						
VDD quiescent current	I_{VDD}	EN = 'HI', no switching		2.2	3.5	mA
VDD shutdown supply current	I_{VDD_SD}	EN = 'LO'			8.0	μA
Vin shutdown supply current	I_{QSHDN}	EN = 'LO', Vin = 5 V			3.5	μA
FEEDBACK VOLTAGE & ERROR AMPLIFIER						
Reference voltage at FB	V_{REF}	−40°C < T_A < 85°C	594	600	606	mV
Unity gain bandwidth (Note 1)			14			MHz
Open loop gain (Note 1)			80			dB
FB pin leakage current					100	nA
Output sourcing and sinking current (Note 1)		Ccomp = 20 pF		5		mA
Slew rate (Note 1)				5		V/ μs
OVER CURRENT PROTECTION & ZERO CROSSING						
Over-current limit on high−side FET		When Iout exceeds this threshold for 4 consecutive cycles. Vin = 3.3 V, Vout = 1.5 V with 1 μH inductor, T_A = +25°C	6.9	7.2	8.1	A
One time over-current latch off on the low−side FET		Immediately shut down when sensed current reach this value. Vin = 3.3 V, Vout = 1.5 V with 1 μH inductor, T_A = +25°C	7.0	8.1		A
Zero crossing comparator internal offset (Note 1)		PGND−SWN, Automatic CCM/DCM mode	−4.5	−3.0	−1.5	mV

Table 5. ELECTRICAL CHARACTERISTICS (V_{DD} = V_{IN} = 3.3 V and V_{DD} = V_{IN} = 5.0 V, T_A = T_J = −40°C to 125°C. Typical values are at T_A = 25°C, PGND = GND unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
LOGIC PINS: I/O VOLTAGE AND CURRENT						
EN high threshold voltage			1.1	1.18	1.30	V
EN hysteresis				0.18	0.24	V
EN input pull up resistor				1.35		MΩ
PS mode threshold voltage		Level 1 to Level 2		2.2		V
PS source		10 μA pull−up current when enabled	8	10	12	μA
INTERNAL BST DIODE						
Reverse−bias leakage current		V_{BST} = 6.6 V, V_{in} = 3.3 V, T_A = 25°C			1	μA
SOFT STOP						
Output discharge on−resistance		EN = 0, V_{IN} = 3.3 V, V_{out} = 0.5 V		20		Ω
TIMERS: SOFT START						
Soft start ramp−up time	t_{SS}	Rising from Vss = 0 V to Vss = 0.6 V		1.0		ms
Delay after EN asserting		EN = 'HI'		0.2		ms
Switching frequency control		Forced CCM mode	0.99	1.1	1.21	MHz
PWM						
Minimum OFF time		FCCM mode or Automatic CCM/DCM mode		100	140	ns
PWM ramp amplitude (Note1)		2.9 V < V_{IN} < 5.5 V		VIN/4		V
Maximum duty cycle, FCCM mode or Automatic CCM/DCM mode		Fs_W = 1.1 MHz, 0°C < T_A < 85°C	84%	89%		
THERMAL SHUTDOWN						
Thermal shutdown threshold (Note 1)			130	140	150	°C
Thermal shutdown hysteresis (Note 1)				40		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by design, no production test

TYPICAL CHARACTERISTICS

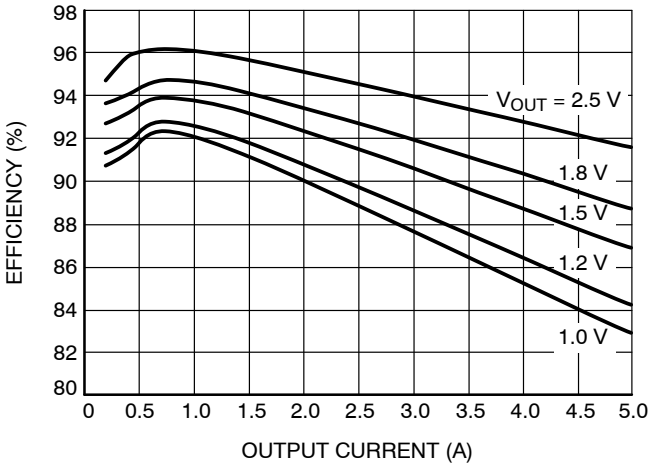


Figure 4. Efficiency at Auto CCM/DCM Mode Vin = 3.3 V

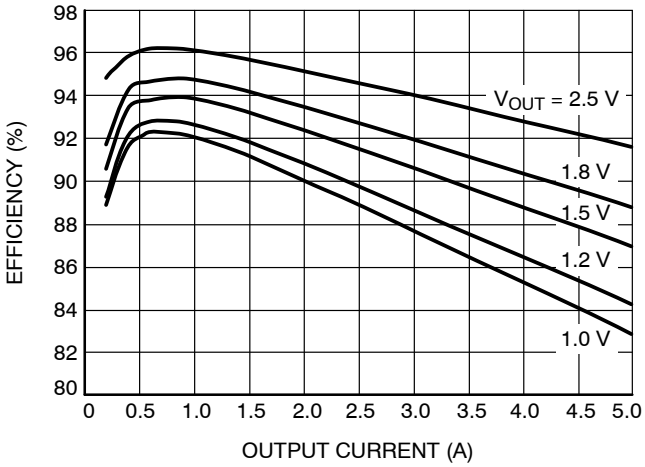


Figure 5. Efficiency at FCCM Mode Vin = 3.3 V

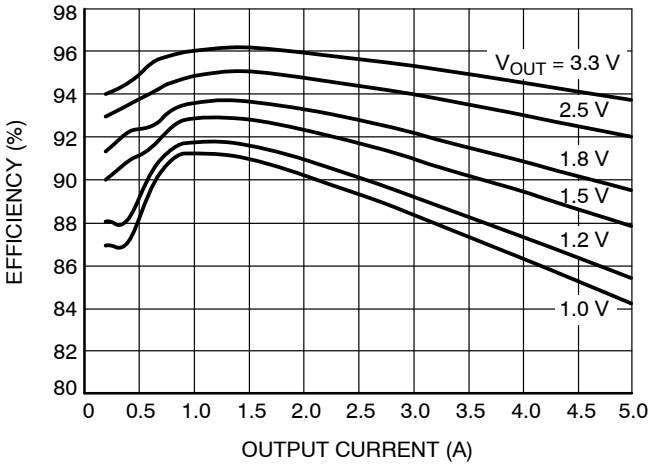


Figure 6. Efficiency at Auto CCM/DCM Mode Vin = 5.0 V

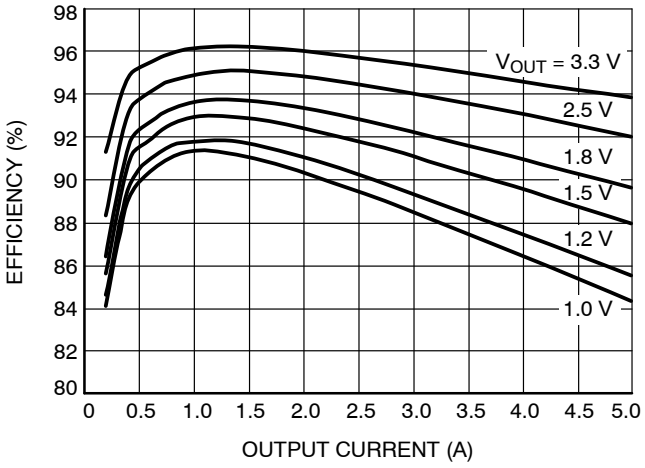


Figure 7. Efficiency at FCCM Mode Vin = 5.0 V

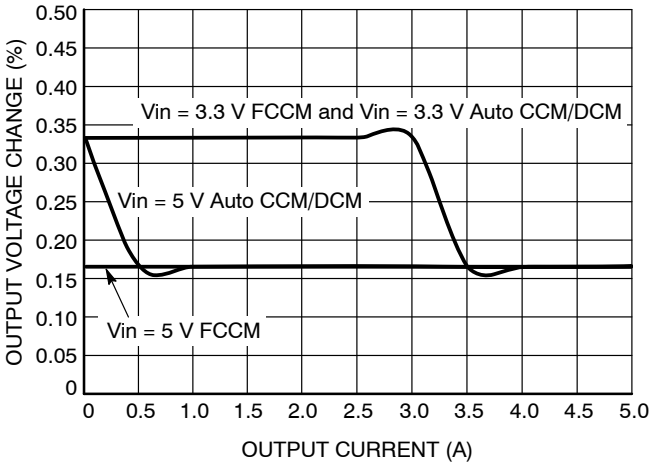


Figure 8. Load Regulation (output current vs. output voltage)

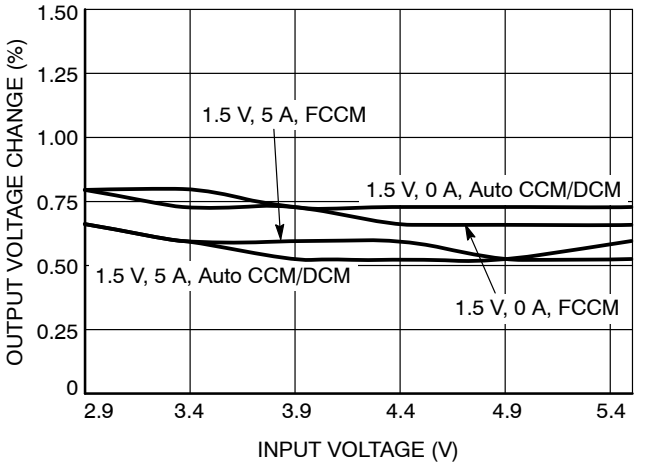


Figure 9. Line Regulation (input voltage vs. output voltage)

TYPICAL CHARACTERISTICS

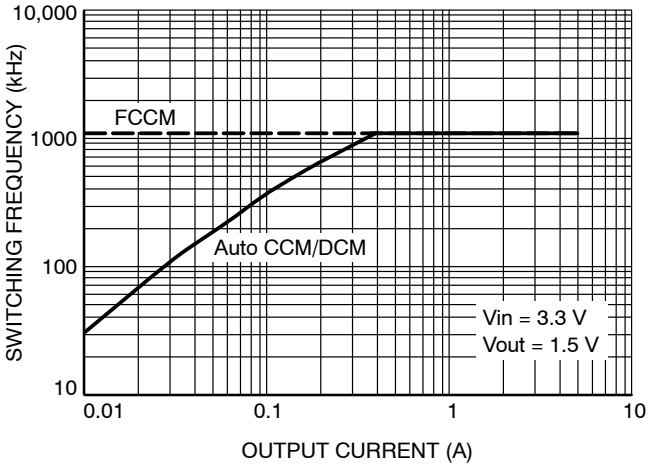


Figure 10. Switching Frequency vs. Output Current at Vin = 3.3 V

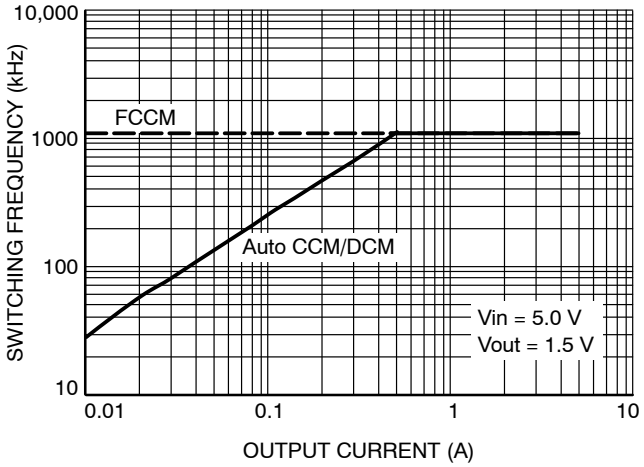


Figure 11. Switching Frequency vs. Output Current at Vin = 5.0 V

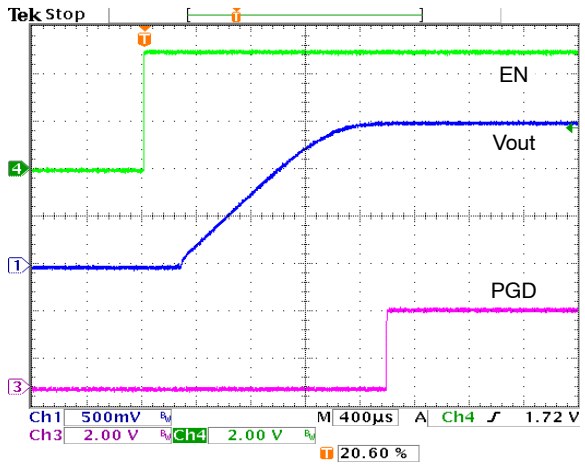


Figure 12. Soft Start−up at Auto CCM/DCM Mode Vin = 3.3 V, No Load

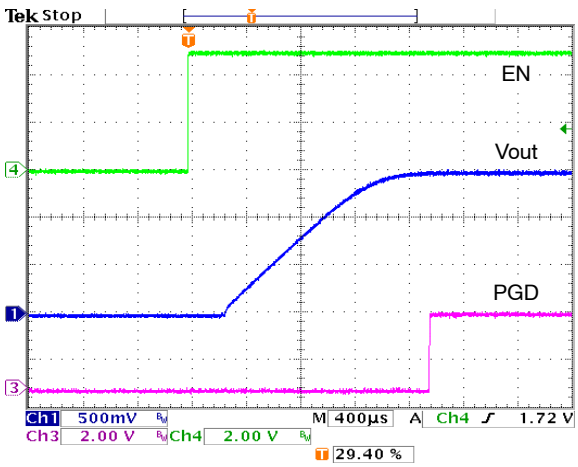


Figure 13. Soft Start−up at Auto CCM/DCM Mode Vin = 3.3 V, 5 A Load

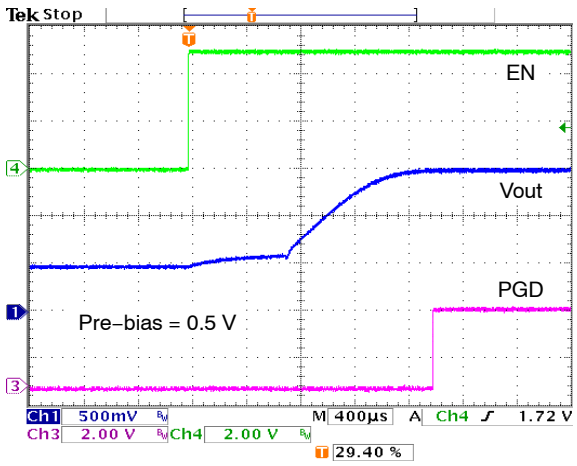


Figure 14. Pre−bias Start−up at Auto CCM/DCM Mode Vin = 3.3 V, No Load

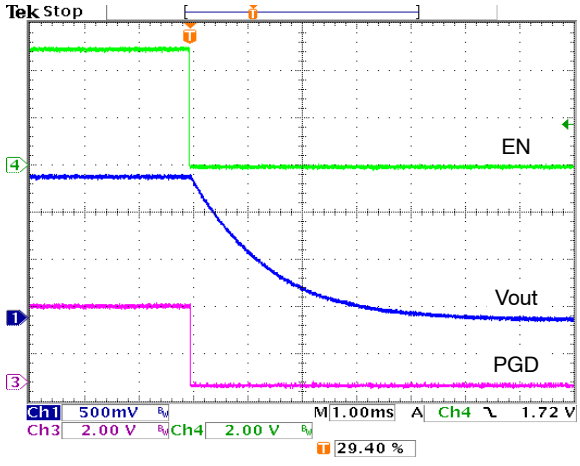


Figure 15. Soft Stop at Auto CCM/DCM Mode Vin = 3.3 V, No Load

TYPICAL CHARACTERISTICS

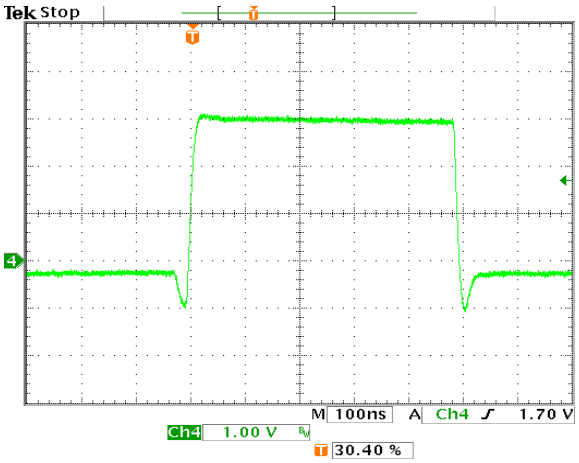


Figure 16. Switching Node Waveform at Auto CCM/DCM Mode Vin = 3.3 V, 5 A Load

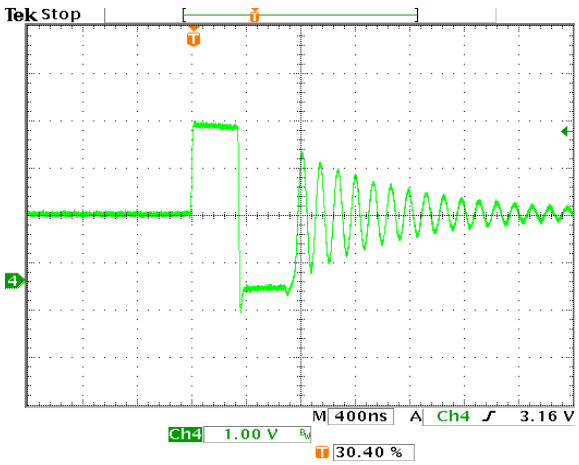


Figure 17. Switching Node Waveform at Auto CCM/DCM Mode Vin = 3.3 V, No Load

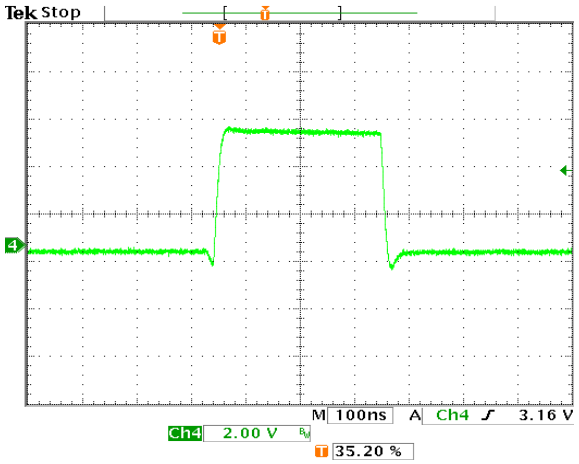


Figure 18. Switching Node Waveform at Auto CCM/DCM Mode Vin = 5.0 V, 5 A Load

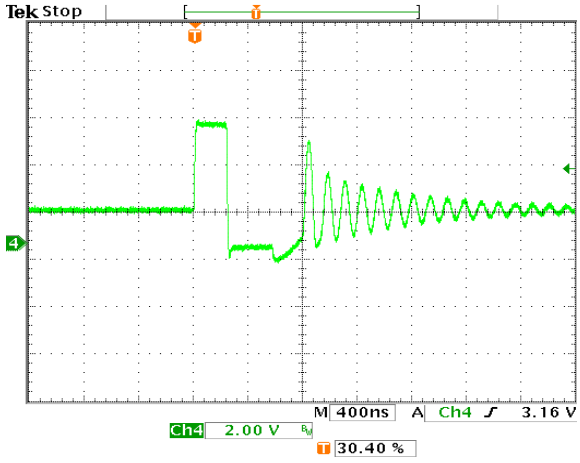


Figure 19. Switching Node Waveform at Auto CCM/DCM Mode Vin = 5.0 V, No Load

DETAILED DESCRIPTION

Overview

NCP3135 is a low input voltage 5 A high performance synchronous buck converter with two integrated N−MOSFETs. NCP3135's output voltage range is from 0.6 V to 0.84 x Vin and it has wide input voltage range from 2.9 V to 5.5 V. The features of NCP3135 include supporting pre−bias start−up to protect sensitive loads, cycle−by−cycle over−current limiting and short circuit protection, power good monitor, over voltage and under voltage protection, built in output discharge and thermal shutdown.

NCP3135 provides two operation modes to fit various application requirements. The automatic CCM/DCM mode operation provides reduced power loss and increases the efficiency at light load. The adaptive power control architecture enables smooth transition between light load and heavy load while maintaining fast response to load transients.

Operation Mode

NCP3135 offers two operation modes programmed by PS pin connections, see table below.

Table 6.

PS pin Connection	Operation Mode	Auto Skip at Light Load
(≤)174 kΩ to GND	Automatic CCM/DCM	Yes
Floating or pulled to VDD	FCCM	

In forced continuous conduction mode (FCCM), the high−side FET is ON during the on−time and the low−side FET is ON during the off−time. The switching is synchronized to an internal clock thus the switching frequency is fixed.

In Automatic CCM/DCM mode, the high−side FET is ON during the on−time and low−side FET is ON during the off−time until the inductor current reaches zero. An internal zero−crossing comparator detects the zero crossing of the inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic circuitry and turns off the low−side FET.

When the load is increased, the inductor current is always positive and the zero−crossing comparator does not send any zero−crossing signal. The converter enters into continuous conduction mode (CCM) when no zero−crossing is detected for two consecutive PWM pulses. In CCM mode, the switching synchronizes to the internal clock and the switching frequency is fixed.

Reference Voltage

The NCP3135 incorporates 600 mV reference voltage with 1.0 % tolerance.

Internal Soft−Start

To limit the start−up inrush current, an internal soft start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal soft start time is 1.0 ms typically.

Soft Stop

Soft−Stop or discharge mode is always on during faults or disable. In this mode, disable (EN) causes the output to be discharged through an internal 20 Ω transistor inside of SW terminal. The time constant of soft−stop is a function of output capacitance and the resistance of the discharge transistor.

Automatic Power Saving Mode

In Automatic CCM/DCM mode when the load current decreases, the converter will enter power saving mode operation. During power saving mode, the low−side MOSFET will turn off when the inductor current reaches zero. So the converter skips switching and operates with reduced frequency, which minimizes the quiescent current and maintains high efficiency.

Forced Continuous Conduction Mode

When PS pin is floating or pulled high, NCP3135 is operating in forced continuous conduction mode in both light load and heavy load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that need tight regulation of switching frequency at a cost of lower efficiency at light load.

PROTECTIONS

Under Voltage Lockout (UVLO)

There is under-voltage lock out protection (UVLO) for both VIN and VDD in NCP3135, which has a typical trip threshold voltage 2.8 V and trip hysteresis 75 mV for VDD and 130 mV for VIN. If UVLO is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

Over Voltage Protection (OVP)

When feedback voltage is above 17% (typical) of nominal voltage for over 1.7 μs blanking time, an OV fault is set. In this case, the converter de−asserts the PGD signal and performs the over−voltage protection function. The top gate drive is turned off and the bottom gate drive is turned on to discharge the output. The bottom gate drive will be turned off until VFB drops below the UVP threshold. The device enters a high−impedance state. This protection is latched.

Under Voltage Protection (UVP)

Output under−voltage protection works in conjunction with the current protection described in the Over−current Protection sections. An UVP circuit monitors the feedback voltage to detect under−voltage event. The under−voltage limit is 17% (typical) below of nominal voltage at FB pin. If the feedback voltage is below this threshold over 11 μs, an UV fault is set and both the high−side and the low−side FETs turn off. This protection is latched.

Power Good Monitor (PGD)

NCP3135 provides window comparator to monitor the output voltage at FB pin. When the output voltage is within ±17% of regulation voltage, the power good pin outputs a high signal. Otherwise, PGD stays low. The PGD pin is open drain 5 mA pull down output. During startup, PGD stays low until the feedback voltage is within the specified range for about 0.4 ms. If feedback voltage falls outside the tolerance band, the PG pin goes low after 10 μs delay.

The PGD pin de−asserts as soon as the EN pin is pulled low or an under−voltage event on VDD is detected.

Over Current Protection (OCP)

NCP3135 provides both high−side and low−side MOSFET current limiting. When the current through the high−side FET exceeds 7.5 A, the high−side FET turns off and the low−side FET turns on until next PWM cycle. An over−current counter is triggered and starts to increment each occurrence of an over−current event. Both the high−side and the low−side FETs turn off when the OC counter reaches four. The OC counter resets if the detected current is less than 7.5 A after an OC event.

Another set of over−current circuitry monitors the current flowing through the low−side FET. If the current through the low−side FET exceeds 8.1 A, the over−current protection is enabled and immediately turns off both the high−side and the low−side FETs. The device is fully protected against over−current during both on−time and off−time. This protection is latched.

Pre−Bias Startup

In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP3135 supports pre−bias start up by holding low−side FETs off until soft start ramp reaches the FB pin voltage.

Thermal Shutdown

The NCP3135 protects itself from over heating with an internal thermal monitoring circuit. When the die temperature goes beyond a threshold value 135°C, both the high−side and the low−side FETs turn off until the temperature falls 40°C below of the threshold value. Then the converter restarts.

Application Note

For higher output voltage application cases (Vout = 3.3 V), choose the inductor value not to be lower than 1 μH to avoid over-current protection being triggered by inductor current ripple; For Vin = 5 V and Vout = 3.3 V case, add a voltage divider between Vin and EN to ensure that the part can start up without triggering UVP. Use Figure 20 as design reference for schematics. For other lower output voltage cases, it is not necessary to add this divider.

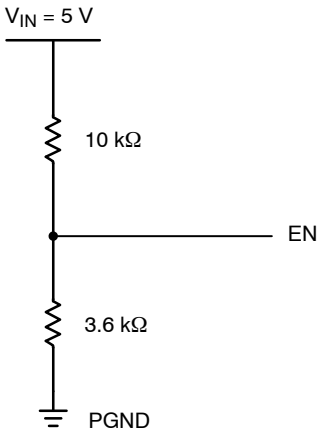


Figure 20. Voltage divider between VIN and EN for start−up in VIN = 5 V and VOUT = 3.3 V case

Layout Guidelines

When laying out a power PCB for the NCP3135 there are several key points to consider.

Use four vias to connect the thermal pad to power ground.

Separate the power ground and analog ground planes; connect them together at a single point.

Increase the thickness of PCB copper, it can help to lower the die temperature and improve the overall efficiency but meanwhile increase the cost of the board fabrication.

Use wide traces for the nodes conducting high current such as VIN, VOUT, PGND and SW.

Place feedback and compensation network components close to the IC.

Keep FB, COMP away from noisy signals such as SW, BST.

Place VIN and VDD decoupling capacitors as close to the IC as possible.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP3135MNTXG	3135	QFN16, 3 x 3, 0.5P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

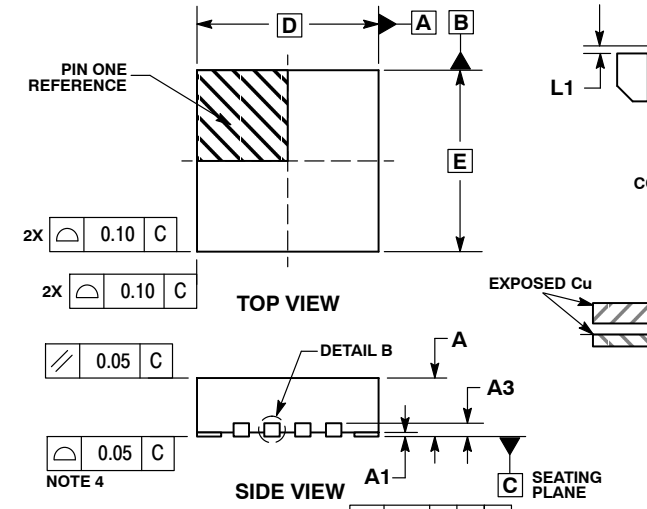
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

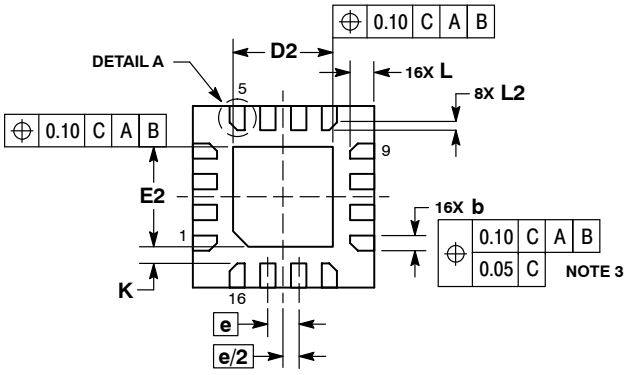
ON Semiconductor®

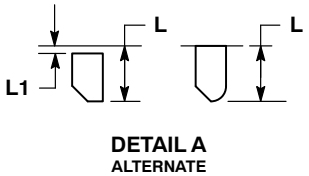
QFN16 3x3, 0.5P
CASE 485DA
ISSUE A

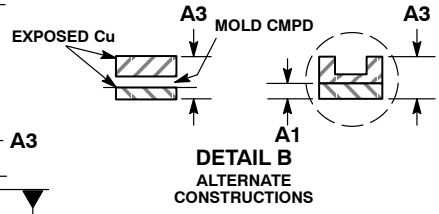
DATE 22 SEP 2015

SCALE 2:1









NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.55	1.75
E	3.00 BSC	
E2	1.55	1.75
e	0.50 BSC	
K	0.275 REF	
L	0.30	0.50
L1	0.00	0.15
L2	0.09 REF	

GENERIC MARKING DIAGRAM*

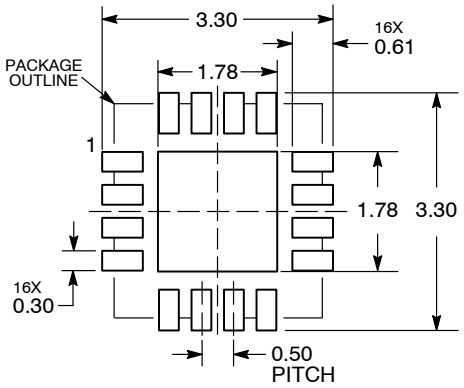


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**QFN16, 3X3, 0.5P**	**PAGE 1 OF 1**

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