NCP700C

LDO Regulator - Ultra Low Noise, High PSRR, BiCMOS RF

200 mA

Noise sensitive RF applications such as Power Amplifiers in cell phones and precision instrumentation require very clean power supplies. The NCP700C is 200 mA LDO that provides the engineer with a very stable, accurate voltage with ultra low noise and very high Power Supply Rejection Ratio (PSRR) suitable for RF applications. In order to optimize performance for battery operated portable applications, the NCP700C employs an advanced BiCMOS process to combine the benefits of low noise and superior dynamic performance of bipolar elements with very low ground current consumption at full loads offered by CMOS.

Furthermore, in order to provide a small footprint for space constrained applications, the NCP700C is stable with small, low value capacitors and is available in a very small WDFN6 1.5 mm x 1.5 mm.

Features

- Output Voltage Options:
  - 4.5 V
  - Contact Factory for Other Voltage Options
- Excellent Line and Load Regulation
- Ultra Low Noise (typ. 10 μVrms)
- High PSRR (typ 70 dB @ 1 kHz)
- Stable with Ceramic Output Capacitors as low as 1 μF
- Very Low Ground Current (typ. 70 μA @ no load)
- Low Disable Mode Current (max. 1 μA)
- Current Limit Protection
- Thermal Shutdown Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Smartphones / PDAs / Palmtops / GPS
- Cellular Telephones (Power Amplifier)
- Noise Sensitive Applications (RF, Video, Audio)
- Analog Power Supplies
- Battery Supplied Devices

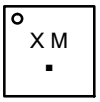
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

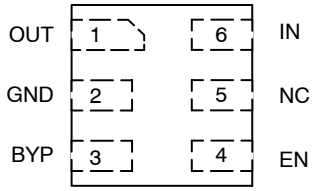


WDFN6
CASE 511BJ



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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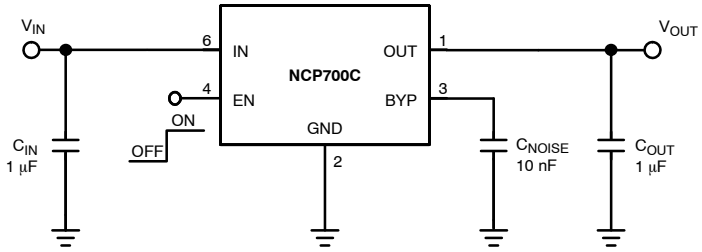


Figure 1. NCP700C Typical Application

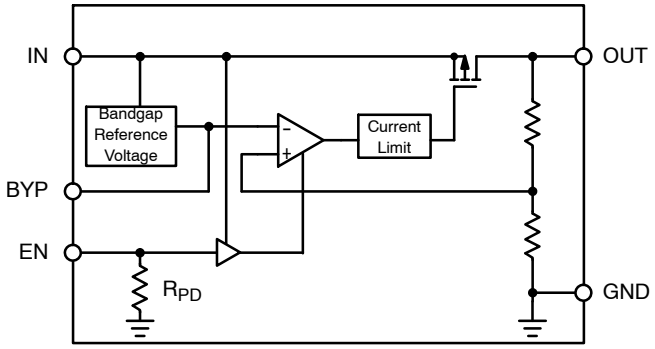


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated Output Voltage
2	GND	Power Supply Ground
3	BYP	Noise reduction pin. (Connect 10 nF or 100 nF capacitor to GND)
4	EN	Enable pin: This pin allows on/off control of the regulator. To disable the device, connect to GND. If this function is not in use, connect to Vin. Internal 5 MΩ Pull Down resistor is connected between EN and GND.
5	N/C	Not connected
6	IN	Input Voltage

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	IN	−0.3 V to 6 V	V
Chip Enable Voltage	EN	−0.3 V to V_{IN} +0.3 V	
Noise Reduction Voltage	BYP	−0.3 V to V_{IN} +0.3 V	V
Output Voltage	OUT	−0.3 V to V_{IN} +0.3 V	V
Output short−circuit duration	Infinity		
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V tested per MIL−STD−883, Method 3015
   Machine Model Method 200 V

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Electrostatic Discharge (Note 1)	Human Body Model	ESD	2000	V
	Machine Model		200	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V tested per MIL−STD−883, Method 3015
   Machine Model Method 200 V

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Package Thermal Resistance, WDFN6: (Note 2)			°C/W
Junction−to−Ambient (Note 3)	θ_{JA}	185	
Package Thermal Characterization Parameter, WDFN6:			
Junction−to−Lead (Pin 2) (Note 3)	Ψ_{JL2}	123	
Junction−to−Board (Note 3)	Ψ_{JB}	111	

2. Refer to APPLICATION INFORMATION for Safe Operating Area
3. Single component mounted on 1 oz, FR4 PCB with 645mm^2 Cu area.

ELECTRICAL CHARACTERISTICS V_{IN} = V_{OUT} + 0.5 V or 2.5 V (whichever is greater), V_{EN} = 1.2 V, C_{IN} = C_{OUT} = 1 μF, C_{NOISE} = 10 nF, I_{OUT} = 1 mA, T_J = −40°C to 125°C, unless otherwise specified (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT							
Input Voltage Range			V_{IN}	2.5	–	5.5	V
Output Voltage Accuracy	T_J = −40°C to 125°C, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V I_{OUT} = 1 mA to 200 mA		V_{OUT}	−2.5%	–	+2.5%	V
Line Regulation	V_{IN} = (V_{OUT} +0.5 V) to 5.5 V, I_{OUT} = 1 mA		ΔV_{OUT} / ΔV_{IN}	–	1200	–	μV/V
Load Regulation	I_{OUT} = 0 mA to 200 mA		ΔV_{OUT} / ΔI_{OUT}	–	1.0	–	μV/mA
Dropout Voltage (Note 5)	I_{OUT}= 200 mA	$V_{OUT(NOM)}$ = 4.5 V	V_{DO}	–	80	150	mV
Output Current Limit	V_{OUT} = $V_{OUT(NOM)}$ − 0.1 V		I_{LIM}	200	310	470	mA
Output Short Circuit Current	V_{OUT} = 0V		I_{SC}	205	320	490	mA
Ground Current	I_{OUT} = 0 mA I_{OUT} = 200 mA		I_{GND}	– –	70 75	110 130	μA
Disable Current	V_{EN} = 0 V		I_{DIS}	–	0.1	1	μA
Power Supply Rejection Ratio	V_{IN} = V_{OUT} +0.5 V, V_{OUT} = 4.5 V, I_{OUT} = 150 mA	f = 100 Hz	PSRR	–	66	–	dB
		f = 1 kHz		–	70	–	
		f = 10 kHz		–	55	–	
		f = 100 kHz		–	37	–	
		f = 1 MHz		–	26	–	
Output Noise Voltage	f = 10 Hz to 100 kHz, I_{OUT} = 150 mA, V_{OUT} = 4.5 V	C_{NOISE} = 10 nF C_{NOISE} = 100 nF	V_N	– –	23 10	– –	μV_{RMS}
Turn−On Time (Note 6)	I_{OUT} = 150 mA, C_{NOISE} = 10 nF		t_{ON}	–	400	–	μs
Enable Threshold Low High			$V_{th(EN)}$	– 1.2	– –	0.4 –	V
Enable Internal Pull−Down Resistance (Note 7)			R_{PD}	2.5	5	10	MΩ
Thermal Shutdown	Shutdown, Temperature increasing		T_{SDU}	–	150	–	°C
	Reset, Temperature decreasing		T_{SDD}	–	135	–	°C
Operating Junction Temperature			T_J	−40		125	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Measured when the output voltage falls 100 mV below the nominal output voltage (nominal output voltage is the voltage at the output measured under the condition V_{IN} = V_{OUT} + 0.5 V). In the case of devices having the nominal output voltage V_{OUT} = 1.8 V the minimum input to output voltage differential is given by the $V_{IN(MIN)}$ = 2.5 V.
6. The turn−on time is the time from asserting the EN to the point where output voltage reaches 98% nominal voltage level.
7. Expected to disable the device when EN pin is floating.

TYPICAL CHARACTERISTICS

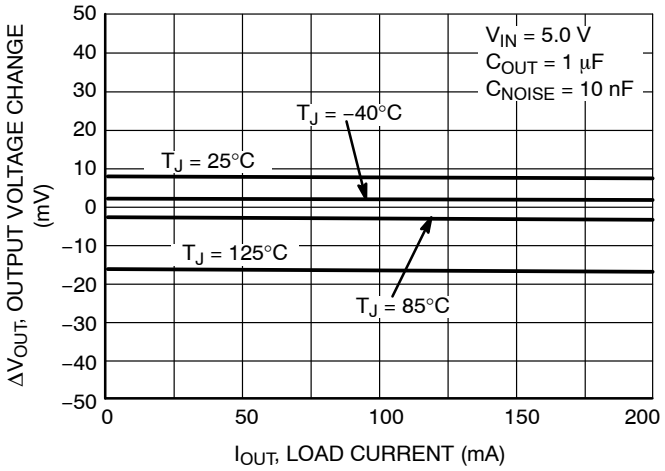


Figure 3. Load Regulation

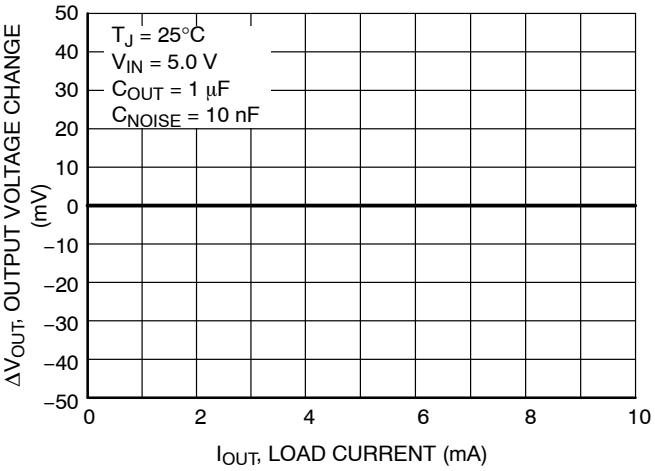


Figure 4. Load Regulation Under Light Loads

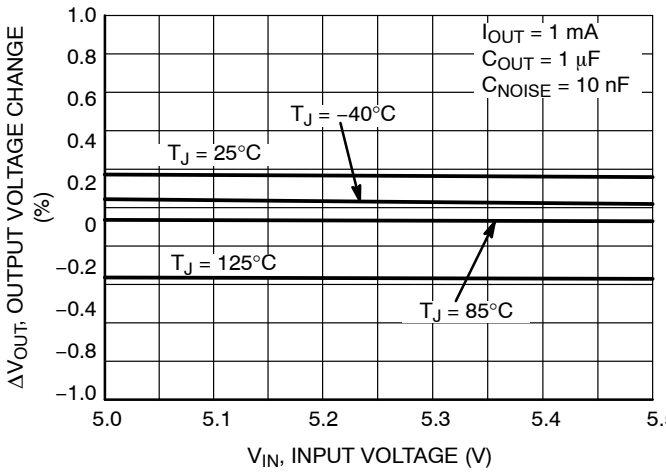


Figure 5. Line Regulation

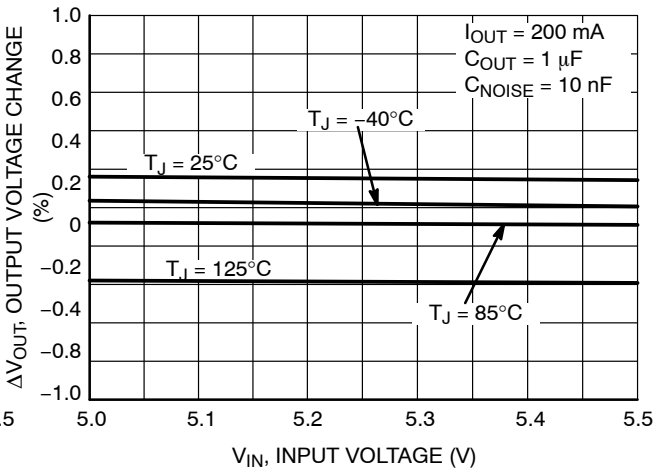


Figure 6. Line Regulation

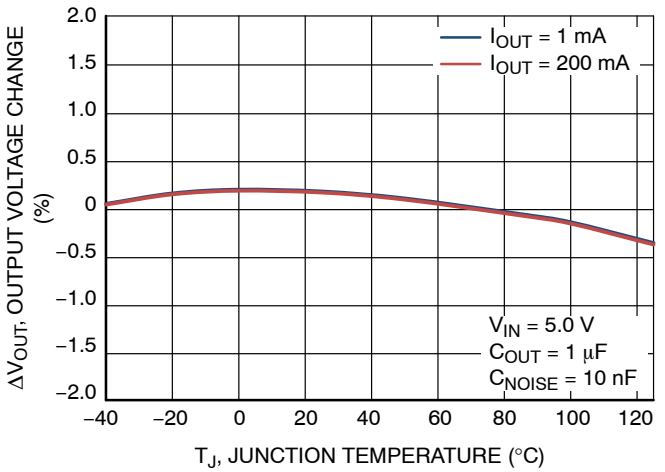


Figure 7. Output Voltage vs. Temperature

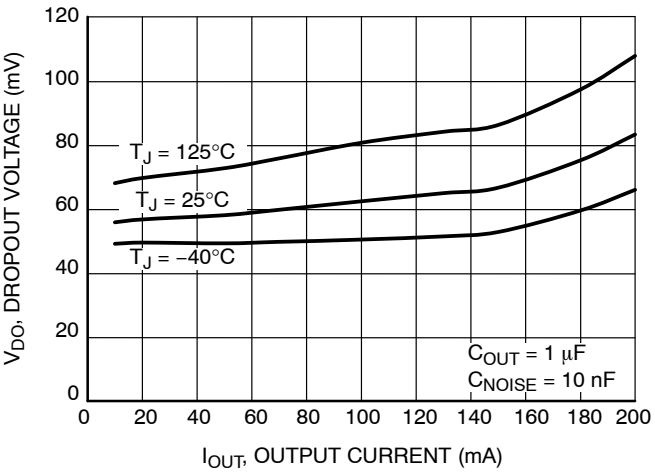


Figure 8. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

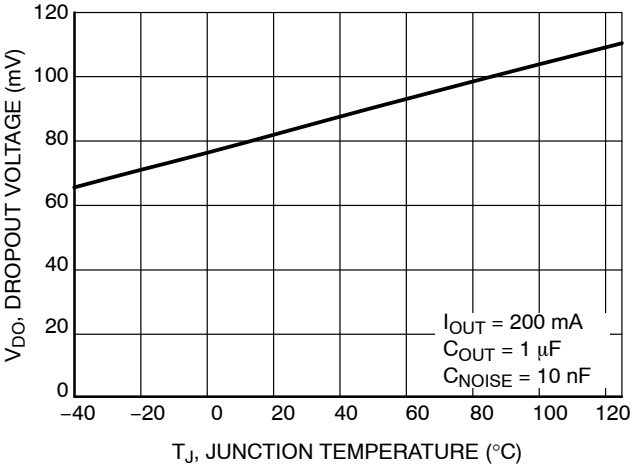


Figure 9. Dropout Voltage vs. Temperature

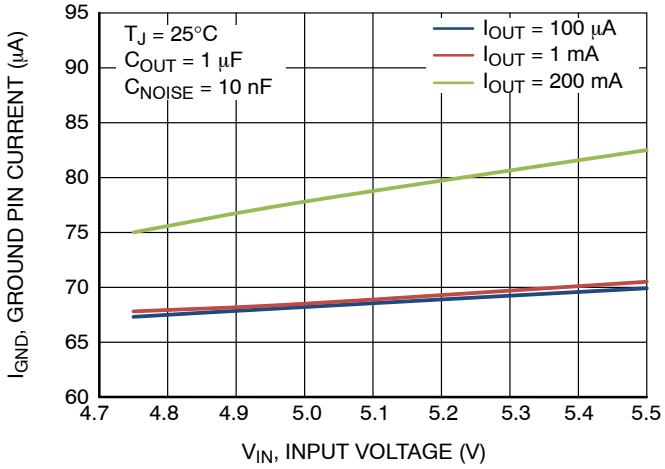


Figure 10. Ground Pin Current vs. Input Voltage

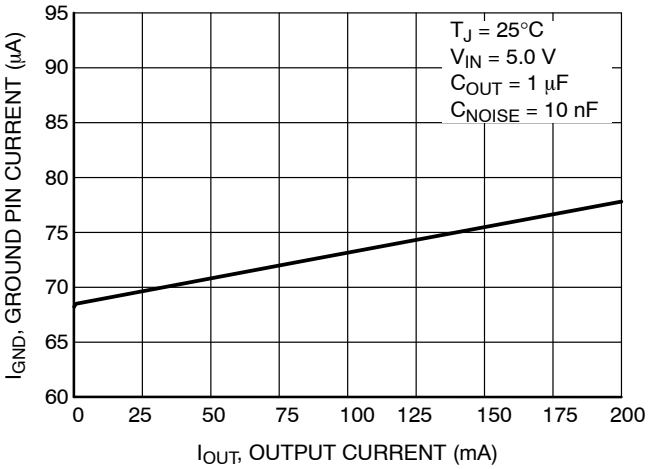


Figure 11. Ground Pin Current vs. Output Current

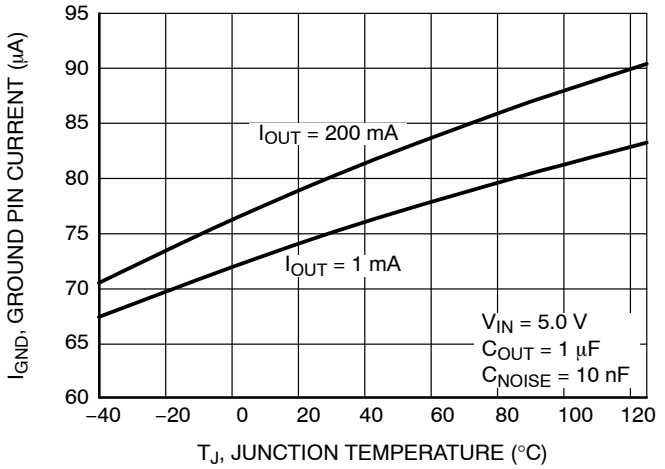


Figure 12. Ground Pin Current vs. Temperature

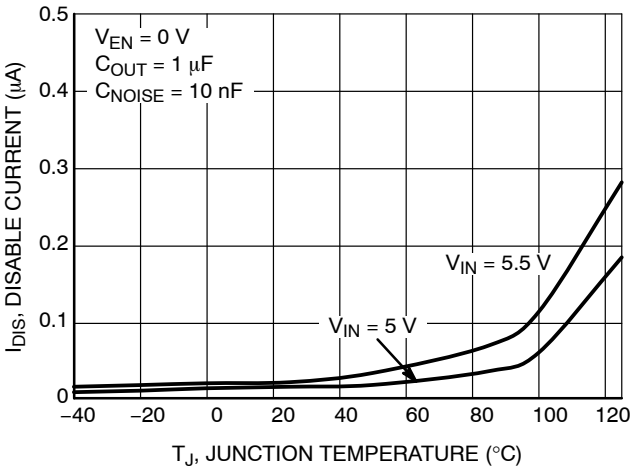


Figure 13. Disable Ground Pin Current vs. Temperature

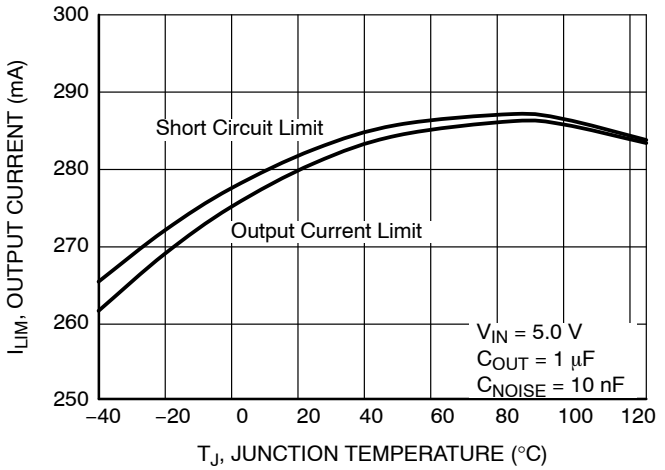


Figure 14. Output Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

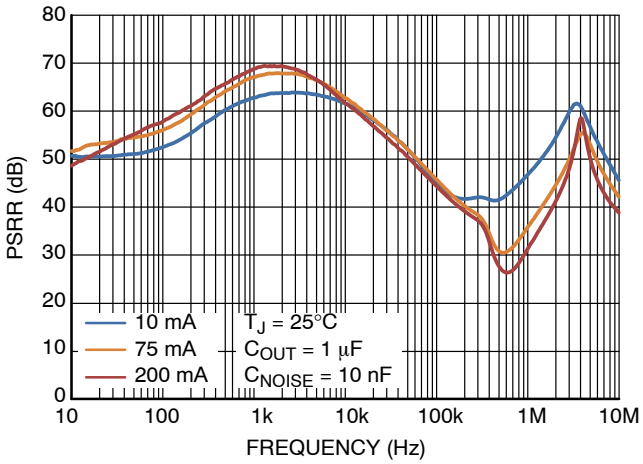


Figure 15. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 1.0 V

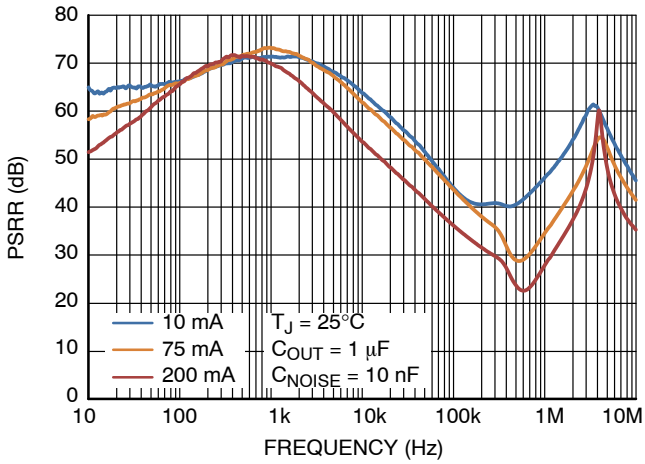


Figure 16. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 0.5 V

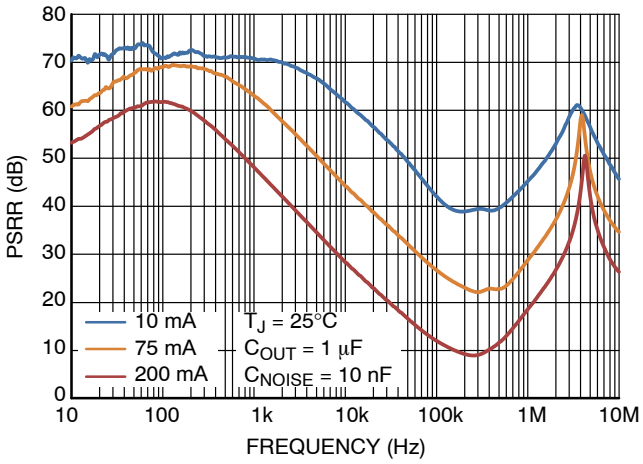


Figure 17. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 0.25 V

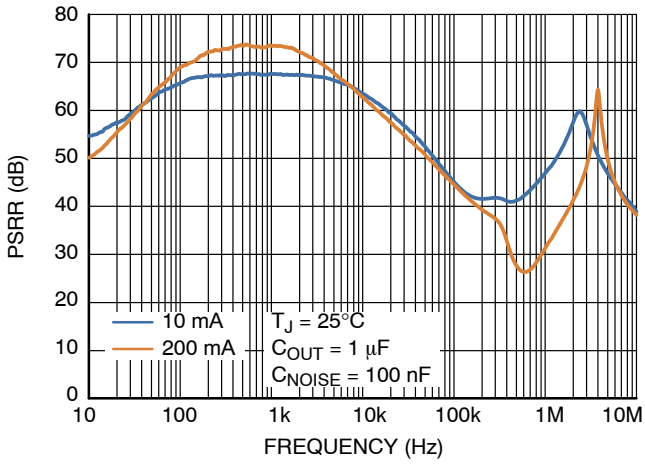


Figure 18. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 1.0 V

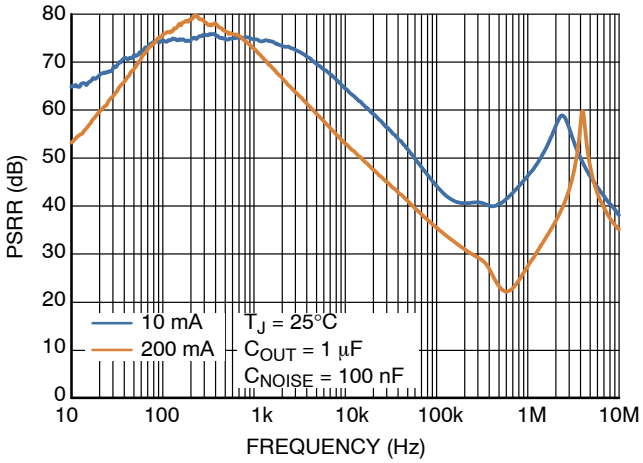


Figure 19. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 0.5 V

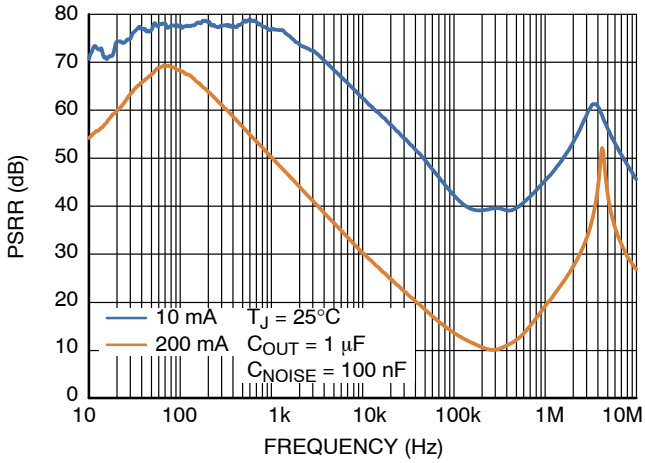


Figure 20. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 0.25 V

TYPICAL CHARACTERISTICS

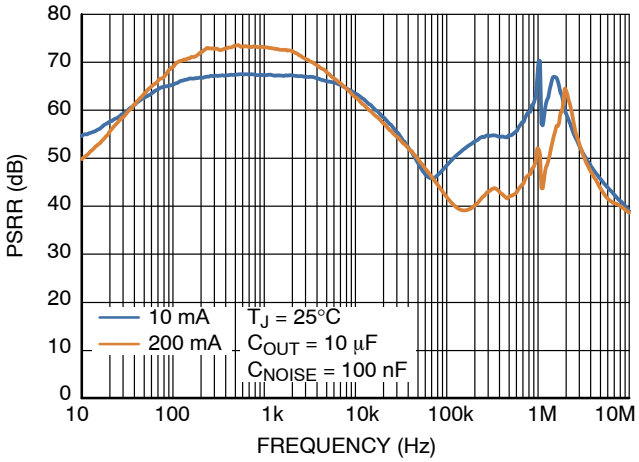


Figure 21. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 1.0 V

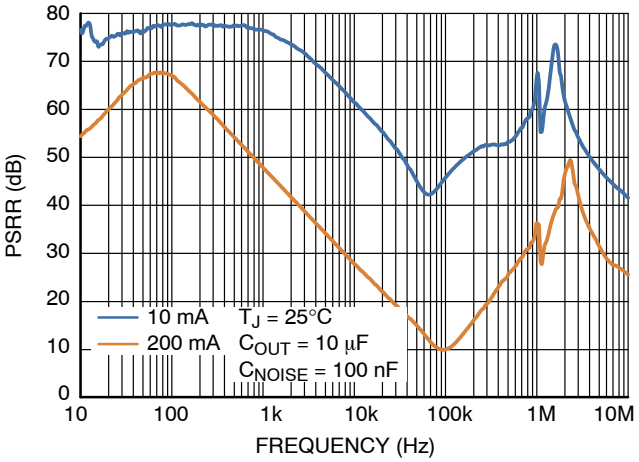


Figure 22. PSRR vs. Frequency, $V_{IN} - V_{OUT}$ = 0.25 V

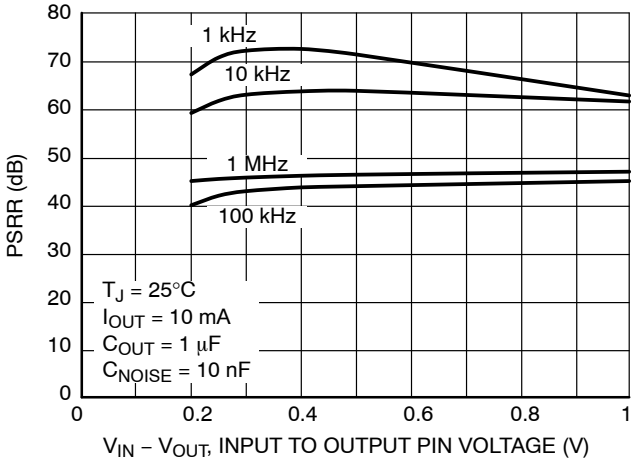


Figure 23. PSRR vs. ($V_{IN} - V_{OUT}$)

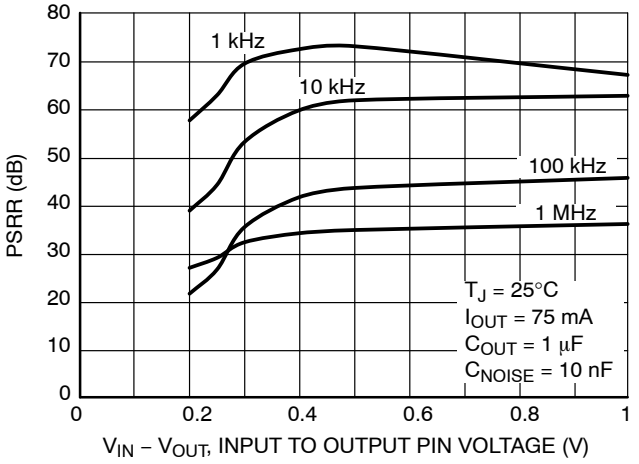


Figure 24. PSRR vs. ($V_{IN} - V_{OUT}$)

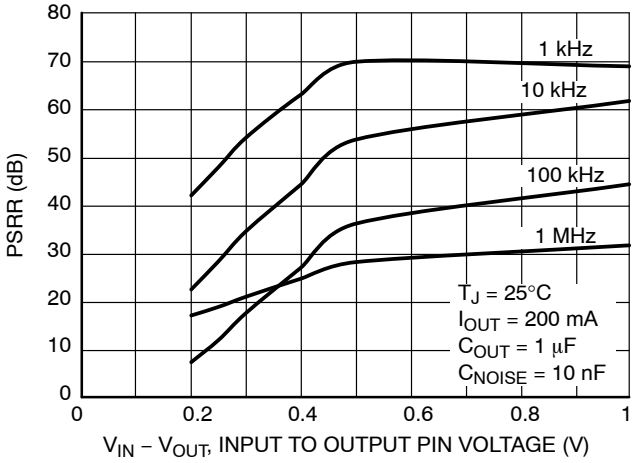


Figure 25. PSRR vs. ($V_{IN} - V_{OUT}$)

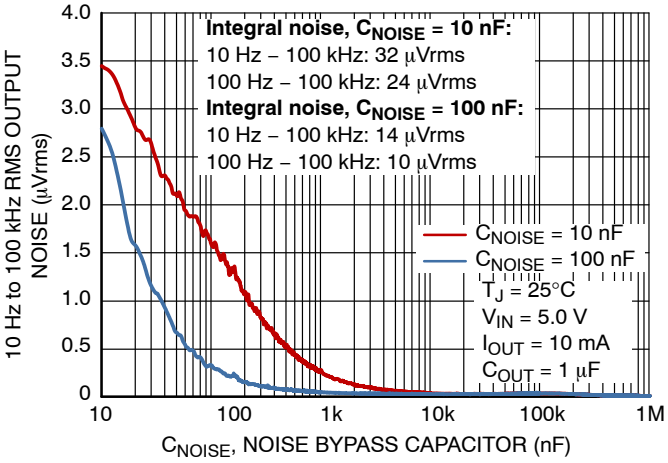


Figure 26. Output Noise vs. Noise Bypass Capacitor

TYPICAL CHARACTERISTICS

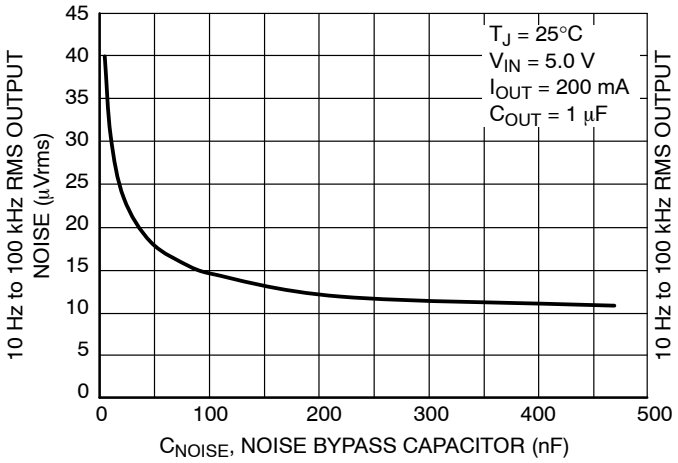


Figure 27. Output Noise vs. Noise Bypass Capacitor

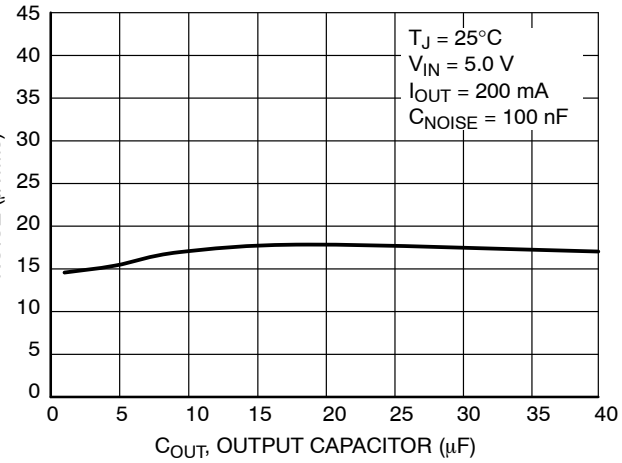


Figure 28. Output Noise vs. Output Capacitor

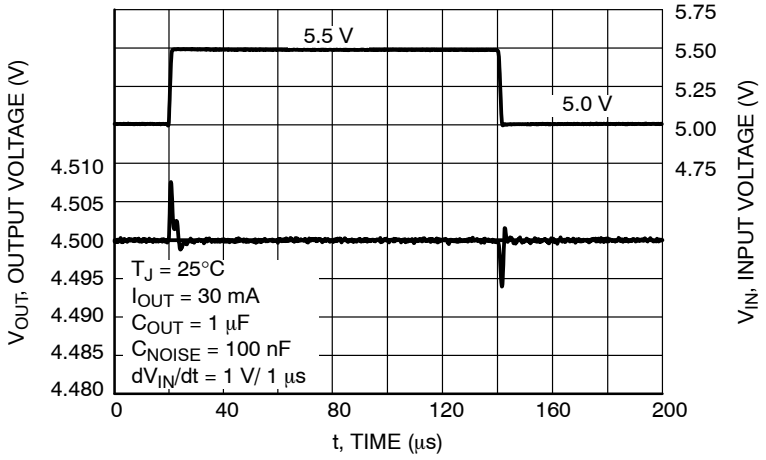


Figure 29. Line Transient Response

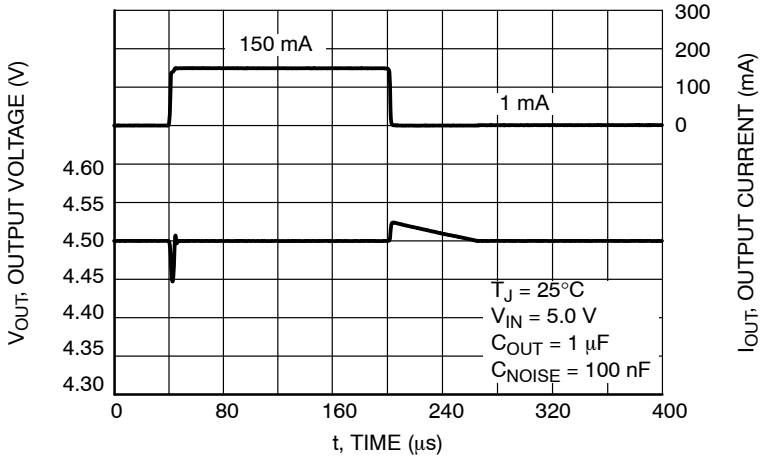


Figure 30. Load Transient Response

TYPICAL CHARACTERISTICS

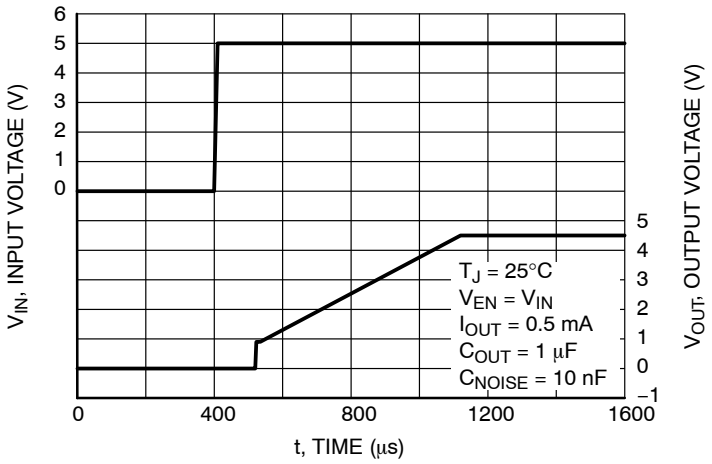


Figure 31. Power−Up

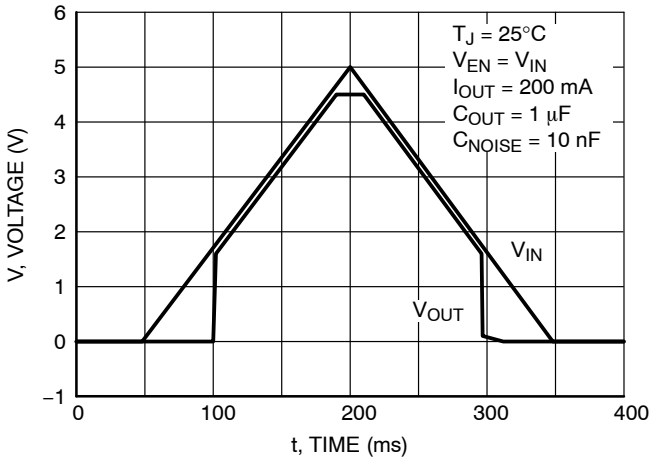


Figure 32. Power−Up / Down

TYPICAL CHARACTERISTICS

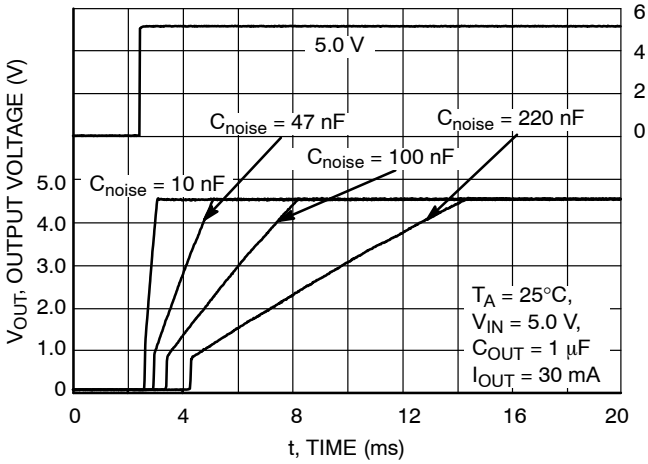


Figure 33. Turn−On Response

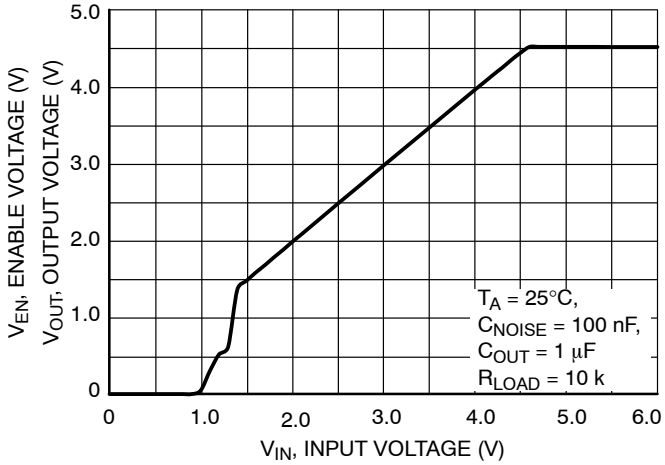


Figure 34. Output Voltage vs. Input Voltage

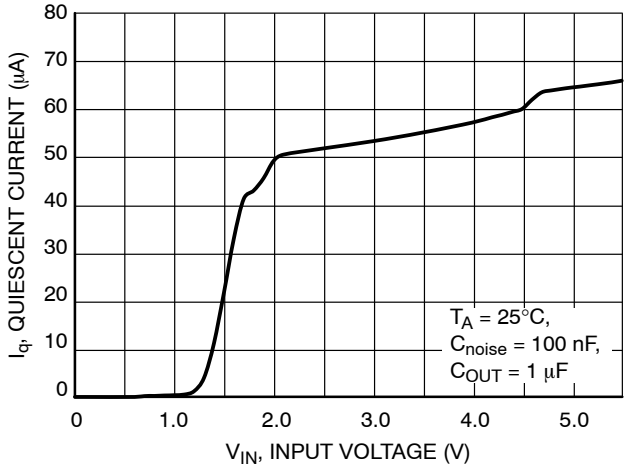


Figure 35. Quiescent Current vs. Input Voltage

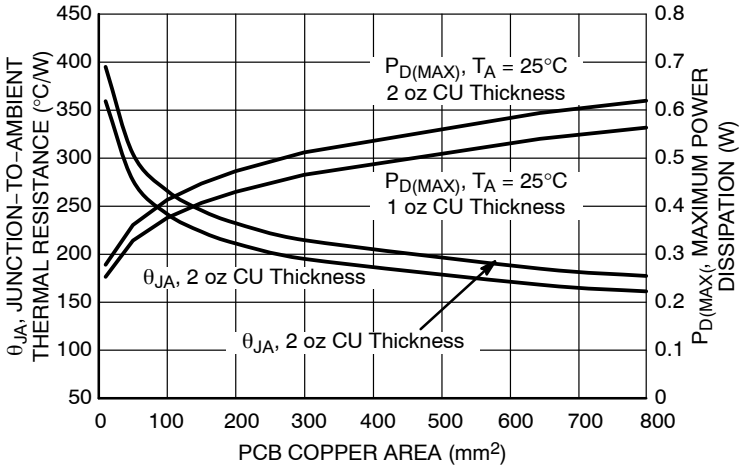


Figure 36. Thermal Resistance and Maximum Power Dissipation vc. Copper Area (WDFN6)

APPLICATIONS INFORMATION

General

The NCP700C is a high performance 200 mA low dropout linear regulator. This device delivers excellent noise and dynamic performance consuming only 75 μA (typ) quiescent current at full load, with the PSRR of (typ) 82 dB at 1 kHz. Excellent load transient performance and small package size makes the device ideal for portable applications.

Logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typically 0.1 μA.

Access to the major contributor of noise within the integrated circuit – Bandgap Reference is provided through the BYP pin. This allows bypassing the source of noise by the noise reduction capacitor and reaching noise levels below 10 μV_{RMS}.

The device is fully protected in case of output short circuit condition and overheating assuring a very robust design.

Input Capacitor Requirements (C_{IN})

It is recommended to connect a 1 μF ceramic capacitor between IN pin and GND pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise present on the input voltage. The input capacitor will also limit the influence of input trace inductances and Power Supply resistance during sudden load current changes. Higher capacitances will improve the line transient response.

Output Capacitor Requirements (C_{OUT})

The NCP700C has been designed to work with low ESR ceramic capacitors on the output. The device will also work with other types of capacitors until the minimum value of capacitance is assured and the capacitor ESR is within the specified range. Generally it is recommended to use 1 μF or larger X5R or X7R ceramic capacitor on the output pin.

Noise Bypass Capacitor Requirements (C_{NOISE})

The C_{NOISE} capacitor is connected directly to the high impedance node. Any loading on this pin like the connection of oscilloscope probe, or the C_{NOISE} capacitor leakage will cause a voltage drop in regulated output voltage. The minimum value of noise bypass capacitor is 10 nF. Values below 10 nF should be avoided due to possible Turn−On overshoot. Particular value should be chosen based on the output noise requirements. Larger values of C_{NOISE} will improve the output noise and PSRR but will increase the regulator Turn−On time.

Enable Operation

The enable function is controlled by the logic pin EN. The voltage threshold of this pin is set between 0.4 V and 1.2 V. Voltage lower than 0.4 V guarantees the device is off. Voltage higher than 1.2 V guarantees the device is on. The NCP700C enters a sleep mode when in the off state drawing less than typically 0.1 μA of quiescent current. The internal 5 MΩ pull−down resistor (R_{PD}) assures that the device is turned off when EN pin is not connected.

The device can be used as a simple regulator without use of the chip enable feature by tying the EN to the IN pin.

Turn−On Time

The Turn−On time of the regulator is defined as the time needed to reach the output voltage which is 98% V_{OUT} after assertion of the EN pin. This time is determined by the noise bypass capacitance C_{NOISE} and nominal output voltage level V_{OUT} according the following formula:

$$t_{ON}\,[s] = C_{NOISE}\,[F] \cdot \frac{V_{OUT}\,[V]}{68 \cdot 10^{-6}\,[A]} \qquad \text{(eq. 1)}$$

Example:
Using C_{NOISE} = 100 nF, V_{OUT} = 3 V, C_{OUT} = 1 μF,

$$t_{ON} = 100 \cdot 10^{-9} \cdot \frac{3}{68 \cdot 10^{-6}} = 4.41\ ms$$

The Turn−On time is independent of the load current and output capacitor C_{OUT}. To avoid output voltage overshoot during Turn−On please select $C_{NOISE} \geq 10$ nF.

Current Limit

Output Current is internally limited within the IC to a typical 310 mA. The NCP700C will source this amount of current measured with a voltage 100 mV lower than the typical operating output voltage. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 320 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} = 5.5 V at T_A = 25°C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SDU} − 150°C typical), Thermal Shutdown event is detected and the output (V_{OUT}) is turned off.

The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 135°C typical). Once the IC temperature falls below the 135°C the LDO is turned−on again.

The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Reverse Current

The PMOS pass transistor has an inherent body diode which will conduct the current in case that the $V_{OUT} > V_{IN}$.

Such condition could exist in the case of pulling the V_{IN} voltage to ground. Then the output capacitor voltage will be partially discharged through the PMOS body diode. It have been verified that the device will not be damaged if the output capacitance is less than 22 μF. If however larger output capacitors are used or extended reverse current

condition is anticipated the device may require additional external protection against the excessive reverse current.

Output Noise

If we neglect the noise coming from the (IN) input pin of the LDO, the main contributor of noise present on the output pin (OUT) is the internal bandgap reference. This is because any noise which is generated at this node will be subsequently amplified through the error amplifier and the PMOS pass device. Access to the bandgap reference node is supplied through the BYP pin. For the 1.8 V output voltage option Noise can be reduced from a typical value of 15 μVrms by using 10 nF to less than 10 μVrms by using a 100 nF from the BYP pin to ground.

Minimum Load Current

NCP700C does not require any minimum load current for stability. The minimum load current is assured by the internal circuitry.

Power Dissipation

For given ambient temperature T_A and thermal resistance $R_{\theta JA}$ the maximum device power dissipation can be calculated by:

$$P_{D(MAX)} = \frac{125 - T_A}{\theta_{JA}} \qquad \text{(eq. 2)}$$

For reliable operation junction temperature should be limited to +125°C.

Load Regulation

The NCP700C features very good load regulation of 5 mV Max. in 0 mA to 200 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause 20 mV voltage drop at full load current, deteriorating the excellent load regulation.

Power Supply Rejection Ratio

The NCP700C features excellent Power Supply Rejection ratio. The PSRR can be tuned by selecting proper C_{NOISE} and C_{OUT} capacitors.

In the frequency range from 10 Hz up to about 10 kHz the larger noise bypass capacitor C_{NOISE} will help to improve the PSRR. At the frequencies above 10 kHz the addition of higher C_{OUT} output capacitor will result in improved PSRR.

PCB Layout Recommendations

Connect the input (C_{IN}), output (C_{OUT}) and noise bypass capacitors (C_{NOISE}) as close as possible to the device pins.

The C_{NOISE} capacitor is connected to high impedance BYP pin and thus the length of the trace between the capacitor and the pin should be as small as possible to avoid noise pickup. In order to minimize the solution size use 0402 or 0603 capacitors. To obtain small transient variations and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. Larger copper area connected to the pins will also improve the device thermal resistance.

The actual power dissipation can be calculated by the formula:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN}I_{GND} \qquad \text{(eq. 3)}$$

Line Regulation

The NCP700C features very good line regulation of 0.6mV/V (typ). Furthermore the detailed Output Voltage vs. Input Voltage characteristics show that up to V_{IN} = 5 V the Output Voltage deviation is typically less than 250 μV for 1.8 V output voltage option and less than 150 μV for higher output voltage options. Above the V_{IN} = 5 V the output voltage falls rapidly which leads to the typical 0.6 mV/V.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP700CMT45TBG	4.5 V	T	WDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

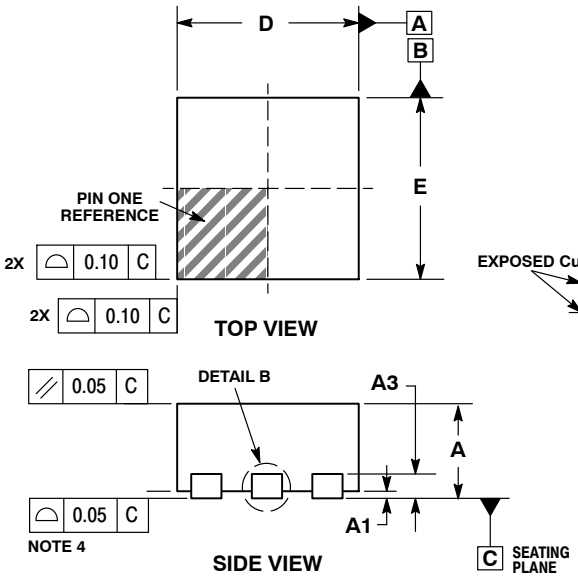
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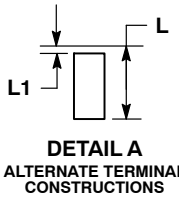
WDFN6 1.5x1.5, 0.5P
CASE 511BJ
ISSUE C

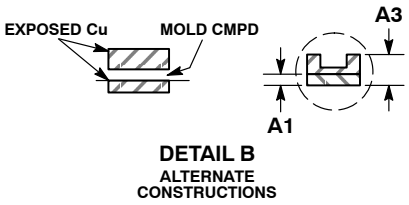
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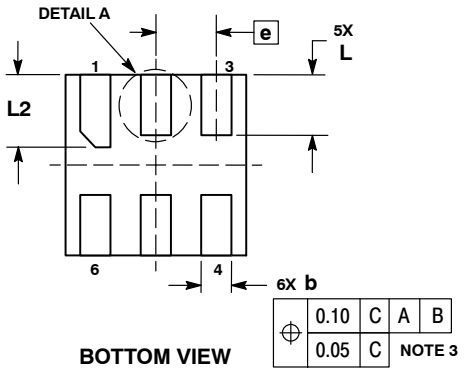


SCALE 4:1





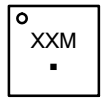




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

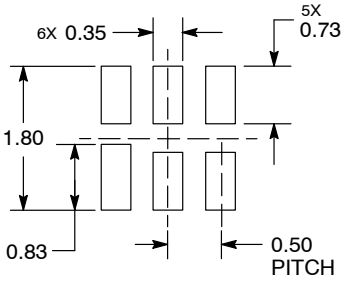
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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