

# Single-Phase Voltage Regulator

High Efficiency, Integrated Power MOSFETs

## NCP3284, NCP3284A

The NCP3284/A, a single-phase synchronous buck regulator, integrates power MOSFETs to provide a high-efficiency and compact-footprint power management solution. The NCP3284 is able to deliver up to 30 A TDC output current, 35 A TDC for NCP3284A, over a wide input and output operating voltage range. Operating in high switching frequency up to 1 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. It provides differential voltage sense, flexible soft-start programming, and comprehensive protections.

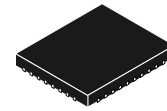
### Features

- $V_{IN} = 4.5\text{ V} \sim 18\text{ V}$  with Input Feedforward
- $V_{OUT} = 0.8\text{ V} \sim 5.5\text{ V}$  with Remote Voltage Sense
- $f_{sw} = 500\text{ k}/600\text{ k}/800\text{ k}/1\text{ MHz}$  Switching Frequency
- Output Current: NCP3284 up to 30 A Continuous, 45 A Pulsed  
NCP3284A up to 35 A Continuous, 50 A Pulsed
- Integrated 5 V LDO or External 5 V Supply
- Enable with Programmable  $V_{IN}$  UVLO
- Selectable Forced CCM and Auto DCM/CCM for High Efficiency at Light Load
- Programmable Soft Start
- Output Discharge in Shutdown
- Programmable Current Limit
- Under-Voltage Protection and Over-Voltage Protection
- Recoverable Thermal Shutdown Protection
- Selectable Protection Mode (Latch-off or Hiccup)
- Power Good Indicator
- PQFN37, 5x6 mm, 0.5 mm Pitch Package
- This Device is Pb-Free and is RoHS Compliant

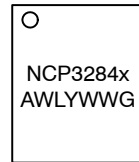
### Typical Applications

- Point of Load
- Telecom and Networking
- Server and Storage System
- Computing Applications

### MARKING DIAGRAM

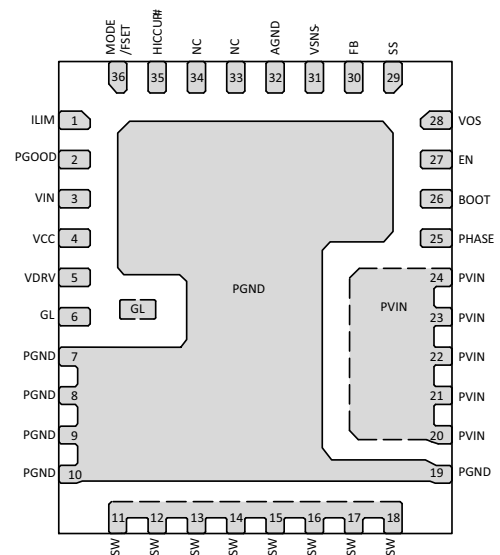


PQFN37 5x6, 0.5P  
CASE 483BZ



A = Assembly Site  
 WL = Wafer Lot Number  
 Y = Year of Production  
 WW = Work Week Number  
 G = Pb-Free Designator

### PINOUT



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

## NCP3284, NCP3284A

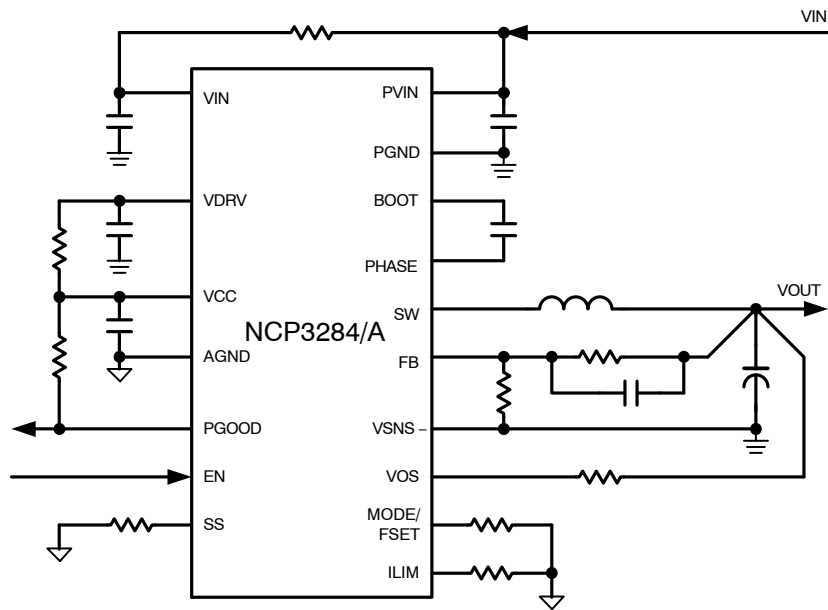


Figure 1. Typical Application Circuit with Single Input Power Supply (LDO Enabled)

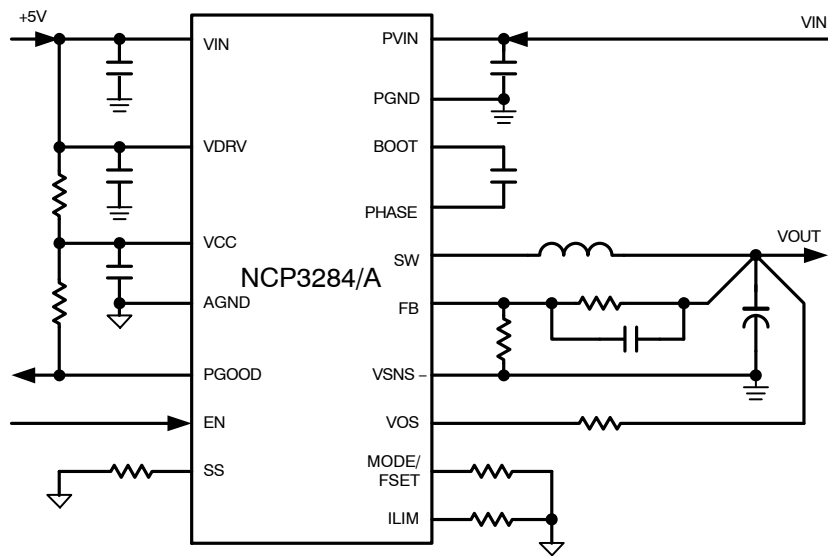


Figure 2. Typical Application Circuit with External 5 V Supply for VCC (LDO Disabled)

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# NCP3284, NCP3284A

## PIN DESCRIPTION

| Pin     | Name      | Type                | Description                                                                                                                                                                                                                                                                                                                                                           |
|---------|-----------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | ILIM      | Analog Output       | Current Limit. A resistor between this pin and AGND to program current limit.                                                                                                                                                                                                                                                                                         |
| 2       | PGOOD     | Logic Output        | Power Good. Open-drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.                                                                                                                                                                                                                       |
| 3       | VIN       | Power Input         | Power Supply Input of LDO. Power supply input pin of internal 5 V LDO. A 1.0 $\mu$ F or more ceramic capacitor must bypass this input to power ground. The capacitor should be placed as close as possible to this pin. A direct short from this pin to VDRV (pin 5) disables the internal LDO for applications with an external 5 V supply as power of VDRV and VCC. |
| 4       | VCC       | Analog Power        | Supply Voltage Input of Controller. A 2.2 $\mu$ F or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.                                                                                                                                                                                           |
| 5       | VDRV      | Analog Power        | Output of LDO and Supply Voltage Input of Gate Drivers. Output of integrated 5.0 V LDO and power supply input of gate drivers. A 4.7 $\mu$ F/25 V or larger ceramic capacitor bypasses this pin to PGND. The capacitor should be placed as close as possible to this pin.                                                                                             |
| 6       | GL        | Analog Output       | Gate of Low-Side MOSFET. Internally connected to the gate of the low-side power MOSFET. No external connection required.                                                                                                                                                                                                                                              |
| 7~10,19 | PGND      | Power Ground        | Power Ground. These pins are the power supply ground pins of the device, which are connected to source of internal low-side power MOSFET. Must be connected to the system ground.                                                                                                                                                                                     |
| 11~18   | SW        | Power Bidirectional | Switch Node. Pins to be connected to an external inductor. These pins are interconnection between internal high-side MOSFET and low-side MOSFET.                                                                                                                                                                                                                      |
| 20~24   | PVIN      | Power Input         | Power Supply Input. These pins are the power supply input pins of the device, which are connected to drain of internal high-side power MOSFET. A 22 $\mu$ F or more ceramic capacitor must bypass this input to PGND. The capacitors should be placed as close as possible to these pins.                                                                             |
| 25      | PHASE     | Power Return        | Phase Node. Provides a return path for integrated high-side gate driver. It is internally connected to source of high-side MOSFET.                                                                                                                                                                                                                                    |
| 26      | BOOT      | Power Bidirectional | Bootstrap. Provides bootstrap voltage for high-side gate driver. A 0.22 $\mu$ F/25 V ceramic capacitor is required from this pin to PHASE (pin 25).                                                                                                                                                                                                                   |
| 27      | EN        | Logic Input         | Enable. Logic high enables controller while logic low disables controller. Input supply UVLO can be programmed at this pin.                                                                                                                                                                                                                                           |
| 28      | VOS       | Analog Input        | Voltage Sense. Remote output voltage sense. Connect to VOUT through 1 k $\Omega$ series resistor.                                                                                                                                                                                                                                                                     |
| 29      | SS        | Analog Input        | Soft Start. A resistor between this pin and GND to program the soft-start slew rate and options.                                                                                                                                                                                                                                                                      |
| 30      | FB        | Analog Input        | Feedback. Inverting input to error amplifier.                                                                                                                                                                                                                                                                                                                         |
| 31      | VSNS-     | Analog Input        | Voltage Sense Negative Input. Connect this pin to remote voltage negative sense point.                                                                                                                                                                                                                                                                                |
| 32      | AGND      | Analog Ground       | Analog Ground. Ground of controller. Must be connected to the system ground.                                                                                                                                                                                                                                                                                          |
| 33~34   | NC        | -                   | No Connection.                                                                                                                                                                                                                                                                                                                                                        |
| 35      | HICCUP#   | Analog Input        | Latch-Off / Hiccup#. Float this pin to enable latch-off mode protections (OCP/ UVP/OVP); Ground this pin to ground to enable hiccup mode protections.                                                                                                                                                                                                                 |
| 36      | MODE/FSET | Analog Input        | Mode and Frequency Set. A resistor between this pin and AGND to program operation mode and nominal switching frequency.                                                                                                                                                                                                                                               |

# NCP3284, NCP3284A

## MAXIMUM RATINGS

| Rating                                            | Symbol              | Value                |                   | Unit |
|---------------------------------------------------|---------------------|----------------------|-------------------|------|
|                                                   |                     | MIN                  | MAX               |      |
| Power Supply Voltage to PGND                      | $V_{PVIN}, V_{VIN}$ |                      | 25                | V    |
| PHASE/SW to PGND                                  | $V_{PHASE}, V_{SW}$ | -0.6<br>-5 (<50 ns)  | 25<br>28 (<10 ns) | V    |
| PVIN to SW/PHASE                                  | $V_{PVIN\_SW}$      | -0.3<br>-5 (<10 ns)  | 25<br>33 (<10 ns) | V    |
| Driver Supply Voltage to PGND                     | $V_{VDRV}$          | -0.3                 | 5.5               | V    |
| Analog Supply Voltage to AGND                     | $V_{VCC}$           | -0.3                 | 6.5               | V    |
| BOOT to PGND                                      | BOOT_PGND           | -0.3                 | 30<br>33 (<10 ns) | V    |
| BOOT to PHASE/SW                                  | BOOT_PHASE/SW       | -0.3                 | 6.5               | V    |
| GL to PGND                                        | GL                  | -0.3<br>-2 (<200 ns) | VDRV+0.3          | V    |
| VSNS- to AGND                                     | VSNS-               | -0.2                 | 0.2               | V    |
| PGND to AGND                                      | PGND                | -0.3                 | 0.3               | V    |
| Other Pins                                        |                     | -0.3                 | VCC+0.3           | V    |
| Human Body Model (HBM) ESD Rating are (Note 1)    | ESD HBM             |                      | 2000              | V    |
| Charge Device Model (CDM) ESD Rating are (Note 1) | ESD CDM             |                      | 2000              | V    |
| Latch up Current: (Note 2)                        | $I_{LU}$            | -100                 | 100               | mA   |
| Operating Junction Temperature Range              | $T_J$               | -40                  | 125               | °C   |
| Operating Ambient Temperature Range               | $T_A$               | -40                  | 100               | °C   |
| Storage Temperature Range                         | $T_{STG}$           | -55                  | 150               | °C   |
| Thermal Resistance Junction to Top Case(Note 3)   | $R_{\Psi JC}$       | 0.8                  |                   | °C/W |
| Thermal Resistance Junction to Board (Note 3)     | $R_{\Psi JB}$       | 0.9                  |                   | °C/W |
| Thermal Resistance Junction to Ambient (Note 3)   | $R_{\theta JA}$     | 26.7                 |                   | °C/W |
| Maximum Power Dissipation (Note 4)                | $P_D$               | 3.75                 |                   | W    |
| Moisture Sensitivity Level (Note 5)               | MSL                 | 1                    |                   | -    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.

2. Latch up Current per JEDEC standard: JESD78 class II.

3. The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4-layer FR-4 PCB board, which has two, 1-ounce copper internal power and ground planes and 2-ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors etc.)

4. The maximum power dissipation ( $P_D$ ) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on  $T_{JMAX} = 125^\circ\text{C}$  and  $T_A = 25^\circ\text{C}$ .

5. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J-STD-020A.

# NCP3284, NCP3284A

**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ , typical values are referenced to  $T_A = T_J = 25^\circ\text{C}$ , Min and Max values are referenced to  $T_A = T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless other noted.)

| Characteristics | Test Conditions | Symbol | MIN | TYP | MAX | UNITS |
|-----------------|-----------------|--------|-----|-----|-----|-------|
|-----------------|-----------------|--------|-----|-----|-----|-------|

## SUPPLY VOLTAGE MONITOR

|                                    |             |             |     |     |     |    |
|------------------------------------|-------------|-------------|-----|-----|-----|----|
| VCC Under-Voltage (UVLO) Threshold | VCC falling | $V_{DDUV-}$ | 4.0 |     |     | V  |
| VCC OK Threshold                   | VCC rising  | $V_{DDOK}$  |     |     | 4.5 | V  |
| VCC UVLO Hysteresis                |             | $V_{DDHYS}$ |     | 200 |     | mV |

## SUPPLY CURRENT

|                                                             |                                                    |                                                             |              |   |     |     |               |
|-------------------------------------------------------------|----------------------------------------------------|-------------------------------------------------------------|--------------|---|-----|-----|---------------|
| PVIN Shutdown Current                                       | EN low                                             |                                                             | $I_{SDPVIN}$ | – | 4.8 | 20  | $\mu\text{A}$ |
| $V_{IN}$ Quiescent Supply Current<br>(VCC Current Included) | EN high, no switching                              | LDO enabled,<br>$V_{IN} = 18\text{ V}$ , $V_{CC} = V_{DRV}$ | $I_{QVIN}$   | – | 3.5 | 6.4 | mA            |
|                                                             |                                                    | LDO disabled,<br>$V_{IN} = V_{DRV} = V_{CC} = 4.5\text{ V}$ |              | – | 3.5 | 6.4 |               |
| $V_{IN}$ Shutdown Current<br>(VCC Current Included)         | EN low<br>$T_A = T_J = 25\text{ }^{\circ}\text{C}$ | LDO enabled,<br>$V_{IN} = 18\text{ V}$ , $V_{CC} = V_{DRV}$ | $I_{SDVIN}$  | – | 42  | 60  | $\mu\text{A}$ |
|                                                             |                                                    | LDO disabled,<br>$V_{IN} = V_{DRV} = V_{CC} = 4.5\text{ V}$ |              | – | 63  | 150 |               |

## 5 V LINEAR REGULATOR

|                 |                                                                                                           |           |     |      |     |    |
|-----------------|-----------------------------------------------------------------------------------------------------------|-----------|-----|------|-----|----|
| Output Voltage  | $6\text{ V} < V_{IN} < 18\text{ V}$ , $I_{DRV} = 0$ to $30\text{ mA}$ (External)<br>EN high, no switching | $V_{DRV}$ | 4.8 | 5.07 | 5.4 | V  |
| Dropout Voltage | $V_{IN} = 5\text{ V}$ , $I_{DRV} = 50\text{ mA}$ (External), EN high,<br>no switching                     | $V_{DO}$  |     |      | 200 | mV |

## PWM MODULATION

|                  |          |                |  |     |  |    |
|------------------|----------|----------------|--|-----|--|----|
| Minimum On Time  | (Note 6) | $T_{on\_min}$  |  | 50  |  | ns |
| Minimum Off Time | (Note 6) | $T_{off\_min}$ |  | 150 |  | ns |

## VOLTAGE REGULATION

|                            |                  |          |     |     |     |    |
|----------------------------|------------------|----------|-----|-----|-----|----|
| Regulated Feedback Voltage | FB to $V_{SNS-}$ | $V_{FB}$ | 795 | 800 | 805 | mV |
|----------------------------|------------------|----------|-----|-----|-----|----|

## VOLTAGE ERROR AMPLIFIER

|                             |                                     |          |     |  |    |    |
|-----------------------------|-------------------------------------|----------|-----|--|----|----|
| FB, $V_{SNS-}$ Bias Current | $V_{FB} = V_{VSNS-} = 1.0\text{ V}$ | $I_{FB}$ | –50 |  | 50 | nA |
|-----------------------------|-------------------------------------|----------|-----|--|----|----|

## CURRENT-SENSE AMPLIFIER

|                      |                                         |             |      |     |     |               |
|----------------------|-----------------------------------------|-------------|------|-----|-----|---------------|
| Closed-Loop DC Gain  |                                         | $GAIN_{CA}$ |      | –10 |     | V/V           |
| –3 dB Gain Bandwidth | (Note 6)                                | $BW_{CA}$   |      | 10  |     | MHz           |
| Input Offset Voltage | $V_{osCS} = V_{SW} - V_{PGND}$ (Note 6) | $V_{osCS}$  | –500 | –   | 500 | $\mu\text{V}$ |

## ENABLE

|                          |                  |               |      |      |      |               |
|--------------------------|------------------|---------------|------|------|------|---------------|
| EN On Threshold          | $V_{EN}$ rising  | $V_{EN\_THR}$ | 1.32 | 1.43 | 1.54 | V             |
| EN Off Threshold         | $V_{EN}$ falling | $V_{EN\_TH}$  | 1.11 | 1.22 | 1.31 | V             |
| Hysteresis Resistance    |                  | $R_{HYS}$     |      | 40   |      | k $\Omega$    |
| Hysteresis Current       |                  | $I_{EN\_HYS}$ |      | 5.4  |      | $\mu\text{A}$ |
| EN Input Leakage Current | EN = 5 V         | $I_{EN\_LK}$  |      |      | 1.0  | $\mu\text{A}$ |

## SWITCHING FREQUENCY

|                                   |                                                                               |                |            |    |      |    |               |
|-----------------------------------|-------------------------------------------------------------------------------|----------------|------------|----|------|----|---------------|
| Switching Frequency in CCM        | 1% Resistor from MODE/FSET Pin to AGND,<br>$V_{out} = 5\text{ V}$<br>(Note 6) | 2.49k or 14.0k | $F_{SW}$   |    | 1000 |    | kHz           |
|                                   |                                                                               | 12.1k or float |            |    | 800  |    |               |
|                                   |                                                                               | 0 or 10.5k     |            |    | 600  |    |               |
|                                   |                                                                               | 4.99k or 7.50k |            |    | 500  |    |               |
| Source Current from Mode/FSET Pin |                                                                               |                | $I_{FSET}$ | 45 | 50   | 55 | $\mu\text{A}$ |

## SOFT START

|                   |                                         |           |  |     |  |    |
|-------------------|-----------------------------------------|-----------|--|-----|--|----|
| System Reset Time | Measured from EN to start of soft start | $T_{RST}$ |  | 0.7 |  | ms |
|-------------------|-----------------------------------------|-----------|--|-----|--|----|

# NCP3284, NCP3284A

**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ , typical values are referenced to  $T_A = T_J = 25^\circ\text{C}$ , Min and Max values are referenced to  $T_A = T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless other noted.)

| Characteristics | Test Conditions | Symbol | MIN | TYP | MAX | UNITS |
|-----------------|-----------------|--------|-----|-----|-----|-------|
|-----------------|-----------------|--------|-----|-----|-----|-------|

## SOFT START

|                            |                                 |                |          |    |     |     |               |
|----------------------------|---------------------------------|----------------|----------|----|-----|-----|---------------|
| Soft Start Time            | 1% Resistor from SS Pin to AGND | 0 or 4.53k     | $T_{SS}$ |    | 1.0 | 1.1 | ms            |
|                            |                                 | 1.5k or 5.76k  |          |    | 2.0 | 2.2 |               |
|                            |                                 | 12.1k or float |          |    | 4.0 | 4.4 |               |
|                            |                                 | 3.48k or 8.87k |          |    | 8.0 | 8.8 |               |
| Source Current from SS Pin |                                 |                | $I_{SS}$ | 45 | 50  | 55  | $\mu\text{A}$ |

## PGOOD

|                       |                                        |                |  |     |     |               |
|-----------------------|----------------------------------------|----------------|--|-----|-----|---------------|
| PGOOD Shutdown Delay  | From EN to PGOOD de-assertion (Note 6) |                |  | 1.0 |     | $\mu\text{s}$ |
| PGOOD Low Voltage     | $I_{PGOOD} = 4\text{ mA Sink}$         | $V_{IPGOOD}$   |  |     | 0.3 | V             |
| PGOOD Leakage Current | PGOOD = 5 V                            | $I_{lkgPGOOD}$ |  |     | 1.0 | $\mu\text{A}$ |

## PROTECTIONS

|                                                                                                           |                                                               |                                 |                |      |      |      |                    |
|-----------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------|----------------|------|------|------|--------------------|
| Valley Current Limit Threshold<br><br>$T_A = T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (Note 6) | NCP3284                                                       | $R_{LIM} = 24.9\text{ k}\Omega$ | $I_{OC}$       |      | 36.5 |      | A                  |
|                                                                                                           |                                                               | $R_{LIM} = 21.5\text{ k}\Omega$ |                |      | 31.5 |      |                    |
|                                                                                                           |                                                               | $R_{LIM} = 16.2\text{ k}\Omega$ |                |      | 24.0 |      |                    |
|                                                                                                           |                                                               | $R_{LIM} = 12.1\text{ k}\Omega$ |                |      | 18.0 |      |                    |
|                                                                                                           | NCP3284A                                                      | $R_{LIM} = 33.2\text{ k}\Omega$ | $I_{OC}$       |      | 49.5 |      | A                  |
|                                                                                                           |                                                               | $R_{LIM} = 30.1\text{ k}\Omega$ |                |      | 45.5 |      |                    |
|                                                                                                           |                                                               | $R_{LIM} = 24.9\text{ k}\Omega$ |                |      | 37.5 |      |                    |
|                                                                                                           |                                                               | $R_{LIM} = 21.5\text{ k}\Omega$ |                |      | 32.5 |      |                    |
|                                                                                                           |                                                               | $R_{LIM} = 16.2\text{ k}\Omega$ |                |      | 24.5 |      |                    |
|                                                                                                           |                                                               | $R_{LIM} = 12.1\text{ k}\Omega$ |                |      | 18.0 |      |                    |
| Valley Current Limit Accuracy                                                                             | $T_J = 25^{\circ}\text{C}$                                    |                                 | $I_{OC\_ACCY}$ | -5   |      | 5    | %                  |
|                                                                                                           | $T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (Note 6) |                                 |                | -10  |      | 10   |                    |
| Fast Under Voltage Protection (FUV) Threshold                                                             | FB to AGND                                                    |                                 |                | 0.15 | 0.2  | 0.25 | V                  |
| Fast Under Voltage Protection (FUV) Delay                                                                 | (Note 6)                                                      |                                 |                |      | 1.0  |      | $\mu\text{s}$      |
| Slow Under Voltage Protection (SUV) Threshold                                                             | COMP to GND (Note 6)                                          |                                 |                |      | 3.0  |      | V                  |
| Slow Under Voltage Protection (SUV) Delay                                                                 | (Note 6)                                                      |                                 |                |      | 50   |      | $\mu\text{s}$      |
| Over Voltage Threshold                                                                                    | FB rising                                                     |                                 |                | 0.95 | 1.0  | 1.05 | V                  |
| Over Voltage Protection Hysteresis                                                                        | FB falling (Note 6)                                           |                                 |                |      | -10  |      | mV                 |
| Over Voltage Debounce Time                                                                                | FB rising to GL high                                          |                                 |                |      | 1.0  |      | $\mu\text{s}$      |
| Hiccup Idle Time                                                                                          | Pin 35 is grounded (Note 6)                                   |                                 |                |      | 32   |      | ms                 |
| Thermal Shutdown (TSD) Threshold                                                                          | (Note 6)                                                      |                                 | $T_{sd}$       | 140  | 150  |      | $^{\circ}\text{C}$ |
| Recovery Temperature Threshold                                                                            | (Note 6)                                                      |                                 | $T_{rec}$      |      | 125  |      | $^{\circ}\text{C}$ |
| Thermal Shutdown (TSD) Debounce Time                                                                      | (Note 6)                                                      |                                 |                |      | 50   |      | ns                 |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by design, not tested in production.

# NCP3284, NCP3284A

## DETAILED DESCRIPTION

### General

The NCP3284/A, a single-phase synchronous buck regulator, integrates power MOSFETs to provide a high-efficiency and compact-footprint power management solution. The NCP3284/A is able to deliver up to 30 A TDC output current on a wide output voltage range. Operating in high switching frequency up to 1 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance

power MOSFETs. It provides differential voltage sense, flexible soft-start programming, and comprehensive protections.

### Operation Modes

Operation mode and switching frequency are programmed at MODE/FSET pin with a  $\pm 1\%$  tolerance resistor as shown in Table 1.

**Table 1. MODE AND SWITCHING FREQUENCY CONFIGURATION**

| Resistance @ MODE/FSET Pin ( $\Omega$ , $\pm 1\%$ ) | Frequency (kHz) | Operation Mode |
|-----------------------------------------------------|-----------------|----------------|
| 0                                                   | 600             | FCCM           |
| 2.49k                                               | 1000            | FCCM           |
| 4.99k                                               | 500             | Auto CCM/DCM   |
| 7.5k                                                | 500             | FCCM           |
| 10.5k                                               | 600             | Auto CCM/DCM   |
| 12.1k                                               | 800             | Auto CCM/DCM   |
| 14.0k                                               | 1000            | Auto CCM/DCM   |
| Float                                               | 800             | FCCM           |

### Current-Mode RPM Operation

The NCP3284/A operates with the current-mode Ramp-Pulse-Modulation (RPM) scheme. In Forced CCM mode, the inductor current is always continuous and the device operates in quasi-fixed switching frequency, which has a typical value programmed by users through a resistor at the MODE/FSET pin. In Auto CCM/DCM mode, the

inductor current is continuous and the device operates in quasi-fixed switching frequency in medium and heavy load range, while the inductor current becomes discontinuous and the device automatically operates in PFM mode with an adaptive fixed on time and variable switching frequency in light load range.

## NCP3284, NCP3284A

### Soft Start and Shut Down

The NCP3284/A has a soft start function which also operates well under a pre-biased output condition. The NCP3284/A's soft start time is externally programmed at SS pins. The output starts to ramp up following a system reset

period  $T_{RST}$ , 0.7 ms typical, after the device is enabled. When the device is disabled or UVLO happens, the device shuts down immediately and both high-side and low-side MOSFETs are off. A timing diagram of power up/down is shown in Figure 4.

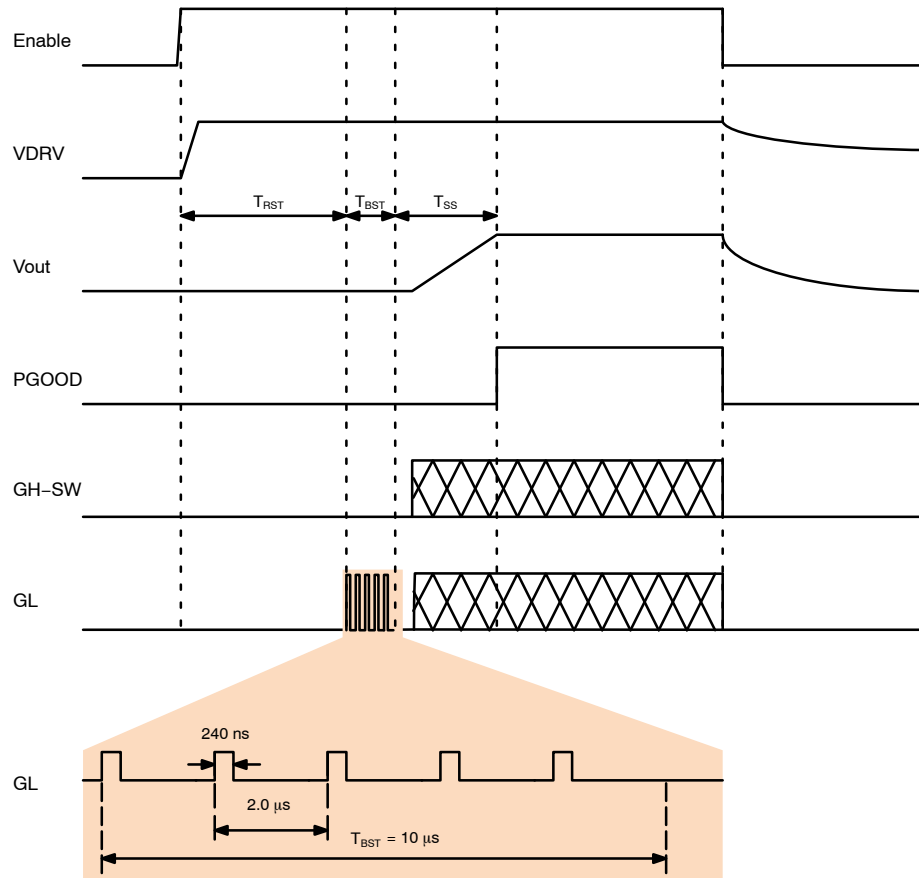


Figure 4. Timing Diagram of Power Up/Down Sequence

### Bootstrap Capacitor Voltage Refreshing

In the NCP3284/A, a bootstrap circuit is employed to provide supply voltage for the high-side gate driver. An external 0.22  $\mu$ F/25 V ceramic capacitor is connected between BOOT pin and PHASE pin to hold up the bootstrap voltage. In order to charge up this capacitor just before a soft start, 5 consecutive pulses are sent to GL, gate of the low-side MOSFET, as shown in Figure 4.

In forced CCM mode, the bootstrap voltage is refreshed cycle-by-cycle and always fully charged. However, a

special care needs to be taken in applications with  $V_{out} \geq 1.8$  V and auto DCM/CCM mode enabled. To make sure the bootstrap capacitor has an enough voltage level for proper operation of high-side gate driver, there is a minimum load requirement to limit the minimum switching frequency not to go below 2 kHz. For a typical 5 V output application with auto DCM/CCM mode enabled, the minimum load current may need to be higher than 2 mA.

### Enable and Input UVLO

The NCP3284/A is enabled when the voltage at EN pin is higher than a summing voltage level of an internal threshold  $V_{EN\_TH}$  and a hysteresis. The hysteresis can be programmed by an external resistor  $R_{EN}$  connected to EN pin as shown in Figure 5. The high threshold  $V_{EN\_H}$  in ENABLE signal is

$$V_{EN\_H} = V_{EN\_TH} + V_{EN\_HYS} \quad (\text{eq. 1})$$

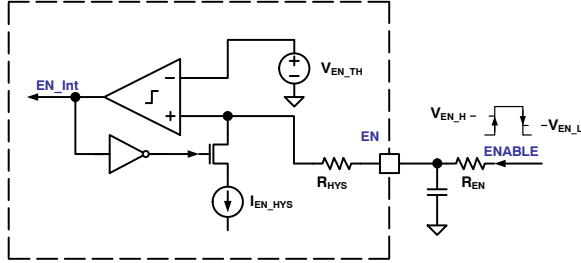


Figure 5. Enable and Hysteresis Programming

The low threshold  $V_{EN\_L}$  in ENABLE signal is

$$V_{EN\_L} = V_{EN\_TH} \quad (\text{eq. 2})$$

The hysteresis  $V_{EN\_HYS}$  is

$$V_{EN\_HYS} = I_{EN\_HYS} \times (R_{HYS} + R_{EN}) \quad (\text{eq. 3})$$

A UVLO function for input power supply can be implemented at EN pin. As shown in Figure 6, the UVLO threshold can be programmed by two external resistors. The low threshold  $V_{IN\_L}$  in  $V_{IN}$  signal is

$$V_{IN\_L} = \left( \frac{R_{EN1}}{R_{EN2}} + 1 \right) \times V_{EN\_TH} \quad (\text{eq. 4})$$

The high threshold  $V_{IN\_H}$  in  $V_{IN}$  signal is

$$V_{IN\_H} = V_{IN\_L} + V_{IN\_HYS} \quad (\text{eq. 5})$$

The hysteresis  $V_{IN\_HYS}$  is

$$V_{IN\_HYS} = I_{EN\_HYS} \times \left( R_{HYS} \left( 1 + \frac{R_{EN1}}{R_{EN2}} \right) + R_{EN1} \right) \quad (\text{eq. 6})$$

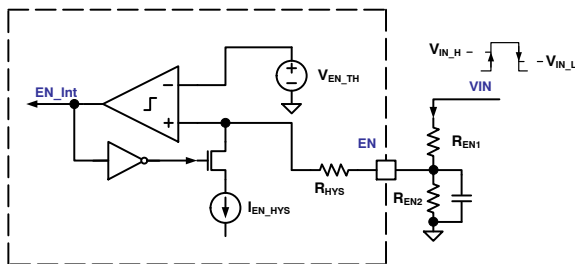


Figure 6. Enable and Input Supply UVLO Circuit

To avoid undefined operation, EN pin should not be left floating in applications.

### Over Current Protection (OCP)

The NCP3284/A protects the converter from over current using a cycle-by-cycle current limit. The average current

limit  $I_{LMT}$  can be calculated from the programmed valley current limit  $I_{LMT\_Valley}$  and inductor current ripple.

$$I_{LMT} = I_{LMT\_Valley} + \frac{V_o \times (V_{IN} - V_o)}{2 \times V_{IN} \times L \times F_{SW}} \\ = 1.5412 \times R_{Ilim} + \frac{V_o \times (V_{IN} - V_o)}{2 \times V_{IN} \times L \times F_{SW}} \quad (\text{eq. 7})$$

where  $R_{Ilim}$  is resistance of the programming resistor at ILIM pin,  $V_{IN}$  is input voltage,  $V_o$  is output voltage,  $L$  is filter inductance, and  $F_{SW}$  is nominal switching frequency.

OCP detection starts from the beginning of soft-start time  $T_{SS}$ , and it ends in shutdown, latch-off, and hiccup idle time. The inductor current is monitored by voltage sensing between the SW pin and PGND pin. If over current happens and lasts for more than 50  $\mu s$ , the device turns to either latch-off or hiccup. The device may enter into under voltage protection before OCP latch-off/hiccup happens if the output voltage drops down very fast.

### Under Voltage Protection (UVP)

UVP detection starts when PGOOD delay  $T_{d\_PGOOD}$  is expired right after a soft start, and it ends in shutdown, latch-off, and hiccup idle time. The NCP3284/A pulls PGOOD low and turns off both high-side and low-side MOSFETs once FB voltage drops below 0.2 V for more than 1.0  $\mu s$ .

### Over Voltage Protection (OVP)

OVP detection starts from the beginning of soft-start time  $T_{SS}$ , and it ends in shutdown, latch-off, and hiccup idle time. During normal operation the output voltage is monitored at the FB pin. If FB voltage exceeds the OVP threshold for more than 1  $\mu s$ , OVP is triggered and PGOOD is pulled low. Meanwhile, the high-side MOSFET is latched off and the low-side MOSFET is turned on. After the OVP trips, the DAC ramps slowly down to zero, having a negative slew rate at the same value of soft start to reduce the negative output voltage spike. The low-side MOSFET toggles between on and off as the output voltage follows the DAC ramping down. After the DAC gets to zero, the high-side MOSFET holds off and the low-side MOSFET remains on.

### Latch-Off or Hiccup in Protections

The NCP3284/A can be configured to have either latch-off mode or hiccup mode, for the protections (OCP, UVP, and OVP), by means of leaving pin 35 float or shorting it to ground.

To restart the device after latch-off, the system needs to cycle either VCC or EN to an off state, then restore, before a normal power-up sequence follows including system reset and auto calibration.

If hiccup mode is selected, the NCP3284/A starts to count idle time of 32 ms once PGOOD is pulled low due to any of the protections. After the end of the hiccup idle time, a normal power up sequence occurs, including system reset and auto calibration.

## Thermal Shutdown (TSD)

The NCP3284/A has an internal thermal shutdown protection to protect the device from overheating in an extreme case that the die temperature exceeds 150°C. T<sub>SD</sub> detection is activated when VCC and EN are valid. Once the thermal protection is triggered, the whole chip shuts down. If the temperature drops below 125°C, the system automatically recovers and a normal power-up sequence follows.

## Power Good (PGOOD)

PGOOD is asserted in normal operation after soft start ends, and it is pulled low in protections and shutdown. The PGOOD pin is an open-drain pin and its internal pull-down control circuit is powered by VCC. To avoid an invalid PGOOD indication when VCC is not ready, it is recommended to have the external pull-up resistor at the PGOOD pin connected to VCC. If VCC is provided by an external source, it should be applied prior to VIN to avoid erroneous PGOOD glitches.

## LAYOUT GUIDELINES

### Electrical Layout Considerations

Good electrical layout is key to ensure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- **Power Paths:** Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance, high-frequency loop area, and undesirable copper losses.
- **Power Supply Decoupling:** The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low-ESL MLCC is placed very close to PVIN and PGND pins

- **VCC Decoupling:** Place decoupling caps as close as possible to the controller VCC and VDRV pins. The filter resistor at the VCC pin should not be higher than 2.2 Ω to prevent large voltage drops.
- **Switching Node:** SW node should be a copper pour, but compact because it is also a noise source
- **Bootstrap:** The bootstrap cap and optional resistor need to be very close and directly connected between pin 26 (BST) and pin 25 (PHASE). No need to externally connect pin 25 to SW node because it has been internally connected to other SW pins.
- **Ground:** It is good to have multiple layers of GND planes on the PCB. Directly connect the exposed PGND pad to GND planes through multiple vias. Connect AGND pin to GND planes through a via close to the AGND pin.
- **Voltage Sense:** Use a Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense. Keep the FB trace short to minimize its capacitance to ground.

### Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pads must be well soldered to the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome around the IC and underneath the exposed pads to connect the inner ground layers to reduce the IC thermal impedance path.
- Use large area copper pours to help thermal conduction and radiation.
- Do not put the inductor too close to the IC, thus the heat sources are distributed.

## DEVICE ORDERING INFORMATION

| Device        | Current | Package             | Shipping†          |
|---------------|---------|---------------------|--------------------|
| NCP3284MNTXG  | 30 A    | PQFN37<br>(Pb-Free) | 3000 / Tape & Reel |
| NCP3284AMNTXG | 35 A    |                     |                    |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

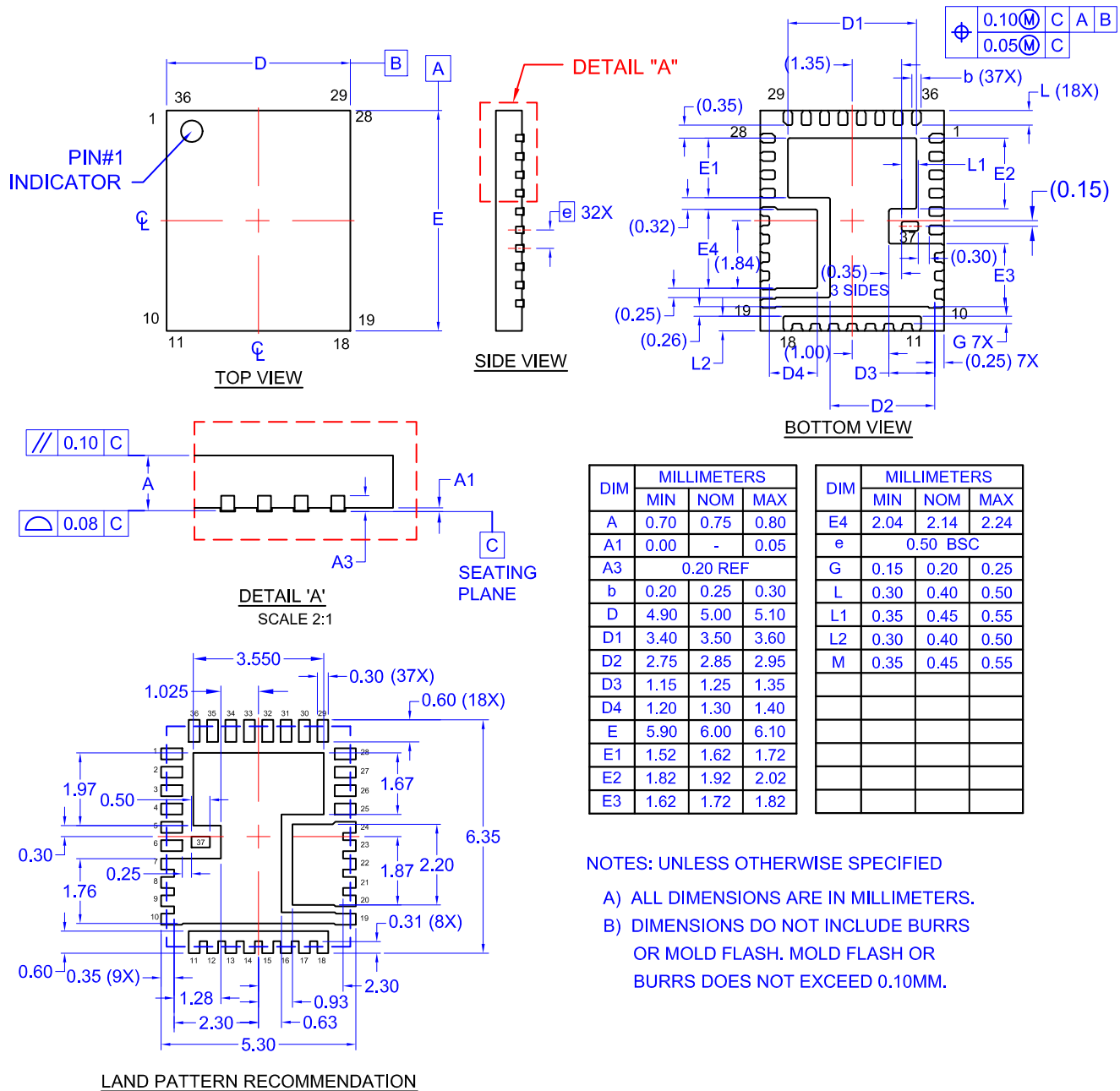
## PACKAGE DIMENSIONS

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