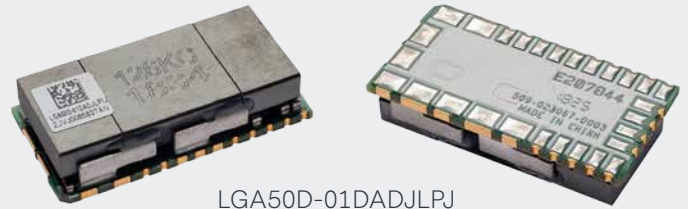


ARTESYN LGA50D LOW PROFILE SERIES

Dual O/P Non-isolated 50 A Digital DC/DC
Converter



LGA50D-01DADJLPJ

Advanced Energy's Artesyn LGA50D is a non-isolated DC-DC converter that is designed for cost and space sensitive applications.

This non-isolated unit offers two independent and configurable 25 amp, 50 watt outputs, which can also be combined to a single configurable 50 amp, 100 watt output. With a footprint of 1 x 0.5 inches or 25.4 x 12.5 mm.

SPECIAL FEATURES

- Two-phase design
- Dual or single output configuration possible
- High efficiency up to 92%
- Small size 1" x 0.5" x 0.51" (LxWxH)
- No minimum load requirement
- Wide operating temperature range
- Exceptional power density
- Analog or digital control
- Automatic loop compensation
- IPC9592B compliant @ $V_{in} = 12 \text{ Vdc}$
- Tape and reel packaging
- Reflow compatible
- Possible to stack up to 4 for 200 A
- I-mon and T-mon supported
- Low-profile version
- Two year shelf life

SAFETY

- Designed to meet IEC62368-1

DATA SHEET

Total Current:

50 A (single)
25 A (dual)

Input Voltage:

7.5 - 14 Vdc

Variable Output:

0.6 - 3.3 V
(low profile)



ELECTRICAL SPECIFICATIONS

Input		
Input voltage range	7.5 -14 Vdc (0.6 Vo ≤ Vo ≤ 3.3 Vo)	
Max input current	20 A	
Input capacitor (internal)	28.2 μF	
Input capacitor (external)	132 μF (See Note 1, Page 2)	
Output		
Independent output 1 and 2	Low profile	
0.6 - 1 V	25 A	
1.8 V	22 A	
2.5 V	17 A	
3.3 V	14 A	
Combined output 1 and 2	Low profile (TBC)	
0.6 - 1 V	50 A	
1.8 V	44 A	
2.5 V	34 A	
3.3 V	28 A	
Efficiency @ Vin=12 V, Freq=615 KHz & Ta=25 °C	Low profile (TBC)	
	Min	Nom
1.0 V	84%	85%
1.8 V	87.5%	88.5%
2.5 V	89%	90.5%
3.3 V	90%	91.1%
Max output power	92 W	
Output capacitor (external) required	2,200 μF, dual O/P mode Vo1 & Vo2 2,400 μF in single O/P mode (See Note 2, Page 2)	

Control and ambient temperatures	
Operating ambient temperature	-40 °C to +85 °C
Storage temperatures	-40 °C to +125 °C
Switching frequency	JLPJ: 615 KHz @ $0.6 V_o \leq V_o \leq 1 V_o$ 800 KHz @ $1 V_o < V_o \leq 3.3 V_o$

Note 1:

6 x 22 μ F/16 V ceramic cap (C2012X6S1C226M125AC or equivalent)

Note 2:

Dual mode (2 outputs): 2 x 680 μ F/6.3 V Polymer Tan caps (T530X687M006ATE010 or equivalent) + 8 x 100 μ F/6.3 V ceramic caps (GRM32EC80J107ME20L or equivalent) + 4 x 10 μ F/10 V ceramic caps (GRM31CR71A106KA01L or equivalent)Single mode (1 output): 2 x 680 μ F/6.3 V Polymer Tan caps (T530X687M006ATE010 or equivalent) + 10 x 100 μ F/6.3 V ceramic caps (GRM32EC80J107ME20L or equivalent) + 4 x 10 μ F/10 V ceramic caps (GRM31CR71A106KA01L or equivalent)

MODEL NUMBERS

Model Number	Input Voltage	Output Voltage Set Point	Output Current	Efficiency
LGA50D-01DADJLPJ	7.5 - 14 Vdc	0.6 - 3.3 V	50 A max	See table
LGA50D-01DADJLP1J	7.5 - 14 Vdc	0.6 - 3.3 V	50 A max	See table

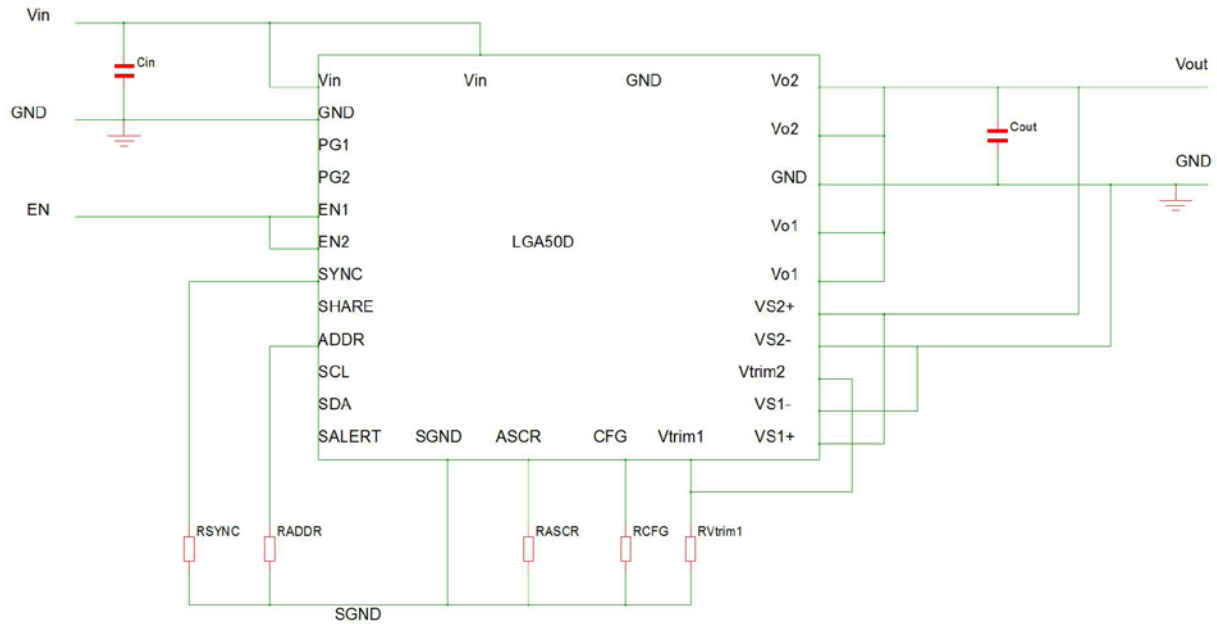
ORDERING INFORMATION

Product Family	Rated Output Current	Performance		Input Voltage	Number of Outputs	Output Type	Pin Termination Type	Protection Mode	RoHS Compliance
LGA	50	D	-	01	D	ADJ	LP	Blank, 1*	J
Series Name	Rated output current = 50 A	Digital POL		7.5 - 14.0 V input voltage range	Dual Outputs	Adjustable output	LP = Low-profile solder bump	Blank; Latching 1*; Auto-recovery	Pb free (RoHS 6/6 compliant)

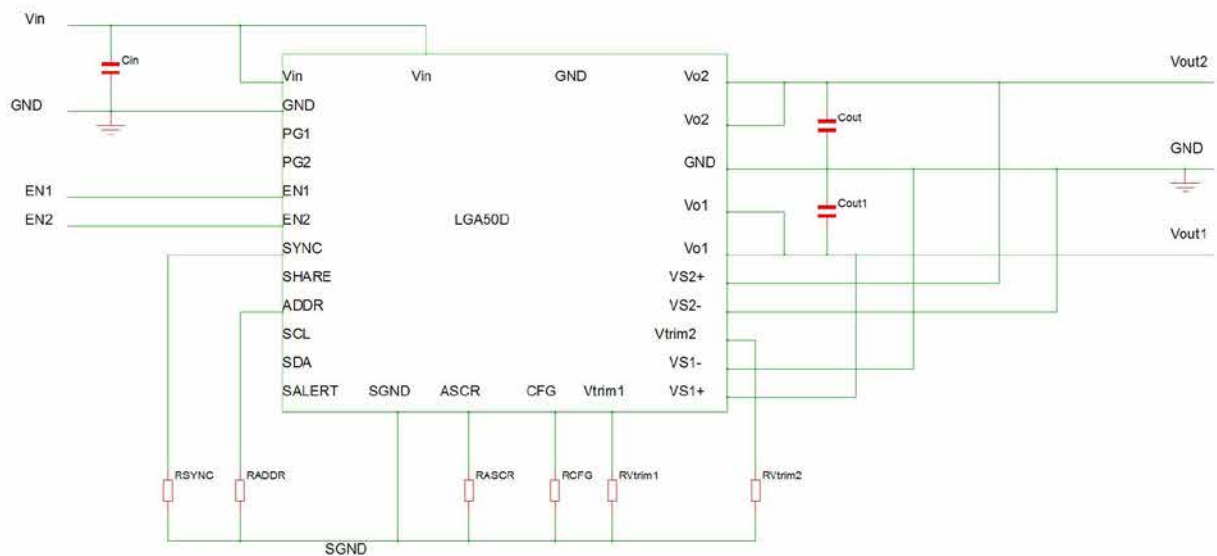
*Current sharing with auto-recovery mode for 1 module only

BLOCK DIAGRAMS

Single Unit, Single O/P Configuration



Single Unit, Dual O/P Configuration

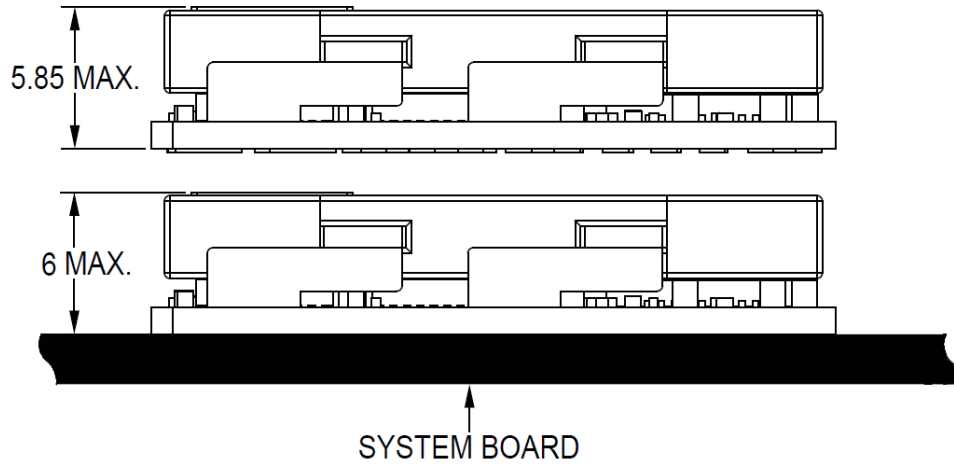


The diagram shows two LGA500 modules connected to a common input and output. The top module is connected to Vin, GND, and Enable. The bottom module is connected to Vin, GND, and a common output Vout. Both modules have internal resistors labeled RSYNC, RADOR, RASCR, RCFG, and RVtrim.

Pin Assignments Single Output			
Pin #	Function	Pin #	Function
1	Vin	15	CFG
2	GND	16	Vtrim1
3	PG1	17	VS1+
4	PG2	18	VS1-
5	EN1	19	Vtrim2
6	EN2	20	VS2-
7	SYNC	21	VS2+
8	SHARE	22	Vo1
9	ADDR	23	Vo1
10	SCL	24	GND
11	SDA	25	Vo2
12	SALERT	26	Vo2
13	SGND	27	GND
14	ASCRCFG	28	Vin

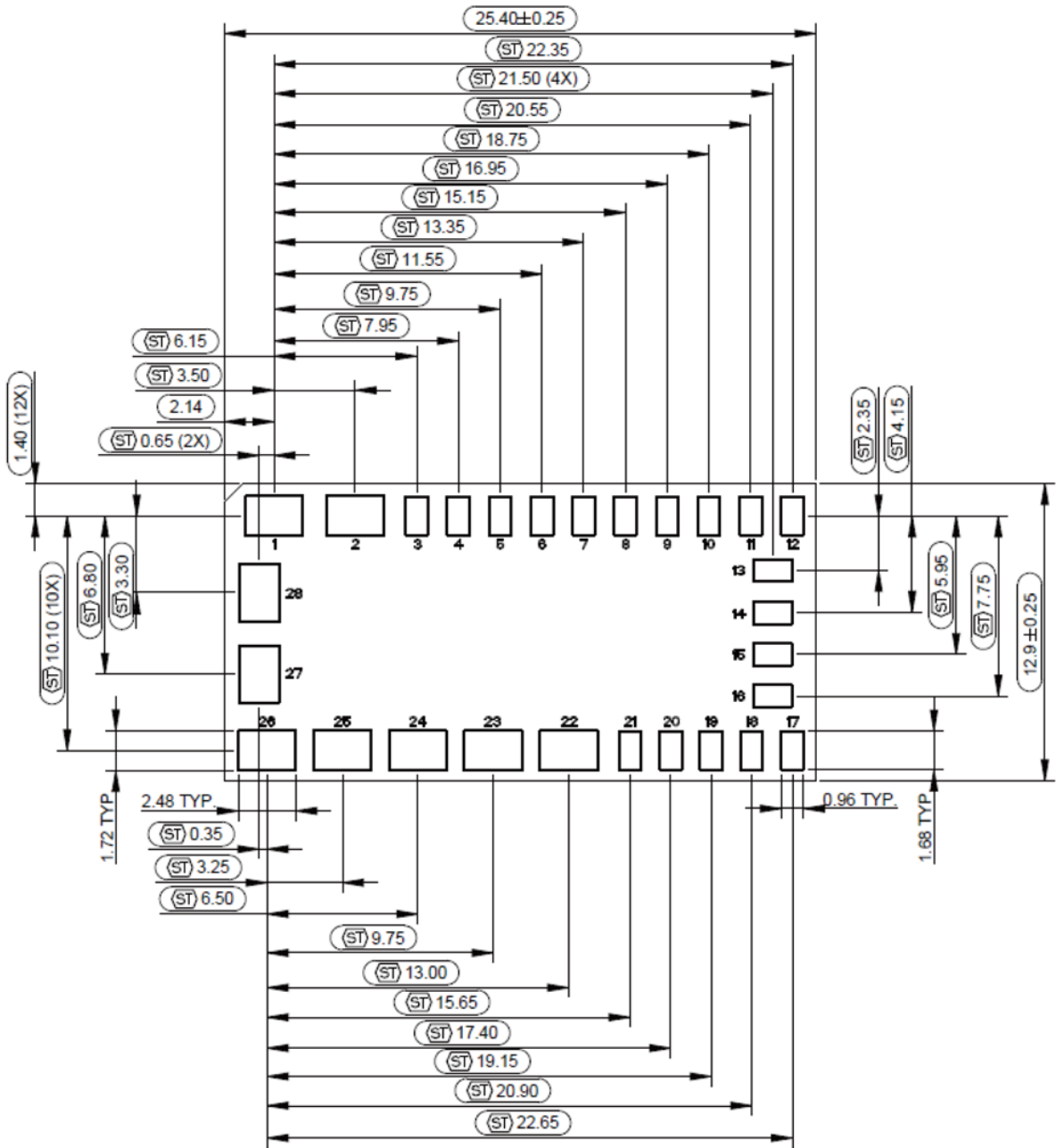
MECHANICAL DRAWINGS

Side view of low-profile solder bump termination type (LGA50D-01DADJLPJ, LGA50D-01DADJLP1J)



MECHANICAL DRAWINGS (CONTINUED)

For low-profile solder bump termination (LGA50D-01DADJLPJ, LGA50D-01DADJLP1J)

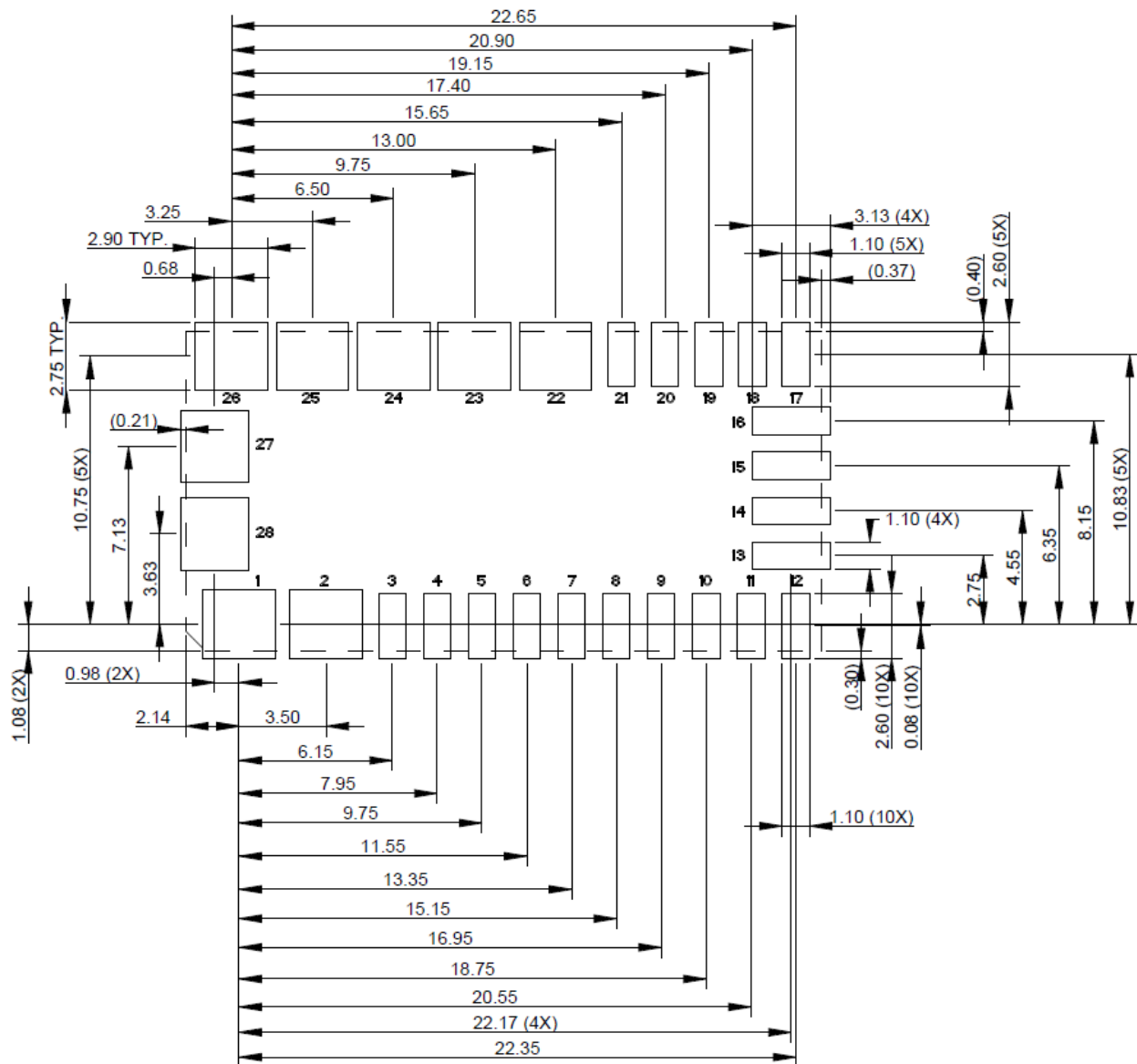


FOOTPRINT DRAWING OF SOLDER BUMP (BOTTOM VIEW)

Dimensions are in millimeters
Tolerances: Decimal .XX ±0.25

MECHANICAL DRAWINGS (CONTINUED)

Proposed solder pad macros (TBC after Artesyn Internal qualification) for low-profile solder bump termination (LGA50D-01DADJLPJ, LGA50D-01DADJLP1J).



PROPOSED PAD LAYOUT

Dimensions are in millimeters

Tolerances: Decimal .XX ±0.25

Dotted line represents LGA50D module outline



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