

# Thyristor

$$V_{RRM} = 2 \times 1600 \text{ V}$$

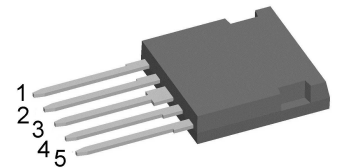
$$I_{TAV} = 50 \text{ A}$$

$$V_T = 1.23 \text{ V}$$

Phase leg

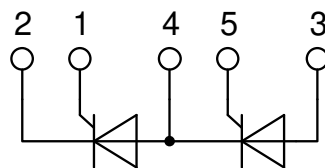
Part number

**CMA50P1600FC**



Backside: isolated

 E72873



### Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

### Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

### Package: i4-Pac

- Isolation Voltage: 3000 V~
- Industry convenient outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Soldering pins for PCB mounting
- Backside: DCB ceramic
- Reduced weight
- Advanced power cycling

### Disclaimer Notice

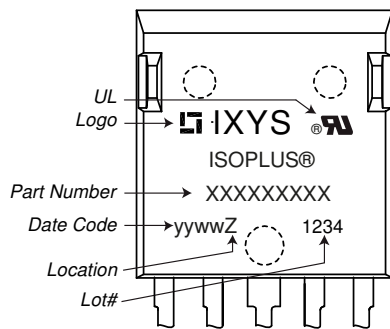
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Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1600	V
$I_{RD}$	reverse current, drain current	$V_{R/D} = 1600 V$	$T_{VJ} = 25^{\circ}C$		50	$\mu A$
		$V_{R/D} = 1600 V$	$T_{VJ} = 125^{\circ}C$		3	mA
$V_T$	forward voltage drop	$I_T = 50 A$	$T_{VJ} = 25^{\circ}C$		1.30	V
		$I_T = 100 A$			1.58	V
		$I_T = 50 A$	$T_{VJ} = 125^{\circ}C$		1.23	V
		$I_T = 100 A$			1.56	V
$I_{TAV}$	average forward current	$T_C = 90^{\circ}C$	$T_{VJ} = 150^{\circ}C$		50	A
$I_{T(RMS)}$	RMS forward current	180° sine			79	A
$V_{T0}$	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.88	V
$r_T$	slope resistance				6.7	m $\Omega$
$R_{thJC}$	thermal resistance junction to case				0.7	K/W
$R_{thCH}$	thermal resistance case to heatsink			0.2		K/W
$P_{tot}$	total power dissipation		$T_C = 25^{\circ}C$		170	W
$I_{TSM}$	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		720	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		780	A
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		610	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		660	A
$I^2t$	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		2.59	kA <sup>2</sup> s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		2.53	kA <sup>2</sup> s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		1.86	kA <sup>2</sup> s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		1.81	kA <sup>2</sup> s
$C_J$	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		32	pF
$P_{GM}$	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
$P_{GAV}$	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}C; f = 50 \text{ Hz}$ repetitive, $I_T = 150 A$			150	A/ $\mu s$
		$t_p = 200 \mu s; di_G/dt = 0.3 A/\mu s;$ $I_G = 0.45 A; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 50 A$			500	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; \text{ method 1 (linear voltage rise)}$	$T_{VJ} = 125^{\circ}C$		1000	V/ $\mu s$
$V_{GT}$	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.4	V
			$T_{VJ} = -40^{\circ}C$		1.6	V
$I_{GT}$	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		80	mA
			$T_{VJ} = -40^{\circ}C$		200	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0.2	V
$I_{GD}$	gate non-trigger current				5	mA
$I_L$	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		450	mA
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
$I_H$	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	$\mu s$
		$I_G = 0.5 A; di_G/dt = 0.5 A/\mu s$				
$t_q$	turn-off time	$V_R = 100 V; I_T = 50 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		150	$\mu s$



Package i4-Pac		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$I_{RMS}$	RMS current	per terminal			70	A
$T_{VJ}$	virtual junction temperature		-40		150	°C
$T_{op}$	operation temperature		-40		125	°C
$T_{stg}$	storage temperature		-40		150	°C
<b>Weight</b>				6		g
$F_C$	mounting force with clip		20		120	N
$d_{Spp/ App}$	creepage distance on surface / striking distance through air	terminal to terminal	1.7			mm
$d_{Spb/ Apb}$		terminal to backside	5.1			mm
$V_{ISOL}$	isolation voltage	t = 1 second	3000			V
		t = 1 minute	2500			V

**Product Marking**



**Part description**

- C = Thyristor (SCR)
- M = Thyristor
- A = (up to 1800V)
- 50 = Current Rating [A]
- P = Phase leg
- 1600 = Reverse Voltage [V]
- FC = i4-Pac (5)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CMA50P1600FC	CMA50P1600FC	Tube	25	507603

Similar Part	Package	Voltage class
CMA30P1600FC	i4-Pac (5)	1600

**Equivalent Circuits for Simulation**

\* on die level

$T_{VJ} = 150^{\circ}C$



**Thyristor**

$V_{0 \max}$	threshold voltage	0.88	V
$R_{0 \max}$	slope resistance *	4.2	mΩ

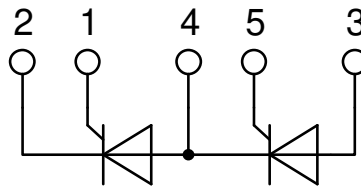


**Outlines i4-Pac**



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.83	5.21	0.190	0.205
A1	2.59	3.00	0.102	0.118
A2	1.17	2.16	0.046	0.085
b	1.14	1.40	0.045	0.055
b2	1.47	1.73	0.058	0.068
b4	2.54	2.79	0.100	0.110
c	0.51	0.74	0.020	0.029
D	20.80	21.34	0.819	0.840
D1	14.99	15.75	0.590	0.620
D2	1.65	2.03	0.065	0.080
D3	20.30	20.70	0.799	0.815
E	19.56	20.29	0.770	0.799
E1	16.76	17.53	0.660	0.690
e	3.81 BSC		0.150 BSC	
L	19.81	21.34	0.780	0.840
L1	2.11	2.59	0.083	0.102
Q	5.33	6.20	0.210	0.244
R	2.54	4.57	0.100	0.180
W	-	0.10	-	0.004

Die konvexe Form des Substrates ist typ. <math>< 0.05\text{ mm}</math> über der Kunststoffoberfläche der Bauteilunterseite  
The convexbow of substrate is typ. <math>< 0.05\text{ mm}</math> over plastic surface level of device bottom side



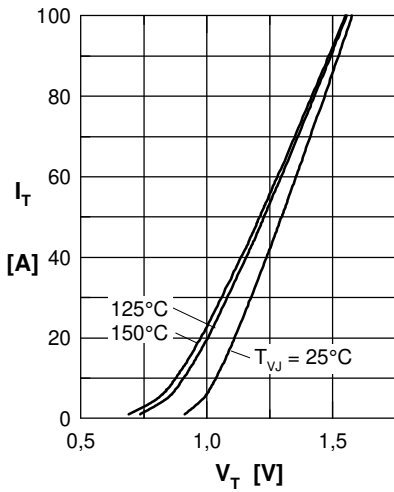
**Thyristor**


Fig. 1 Forward characteristics

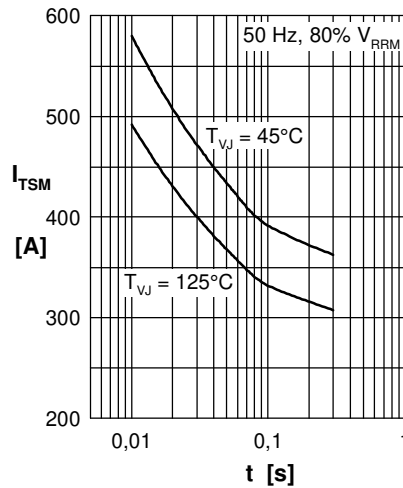


Fig. 2 Surge overload current

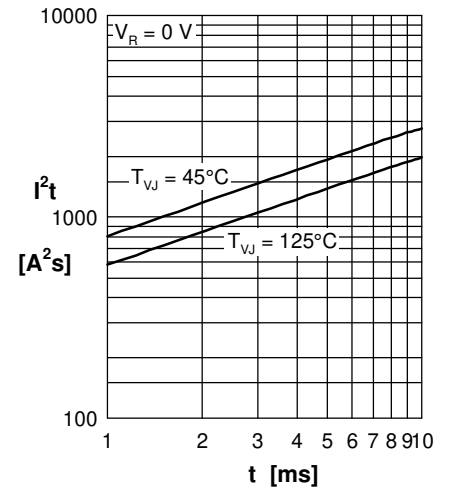
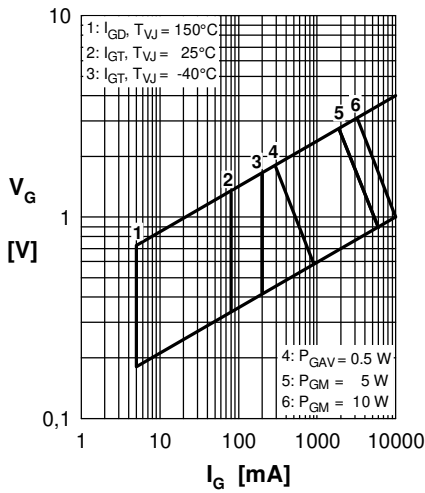

 Fig. 3  $I^2t$  versus time (1-10 ms)


Fig. 4 Gate trigger characteristics

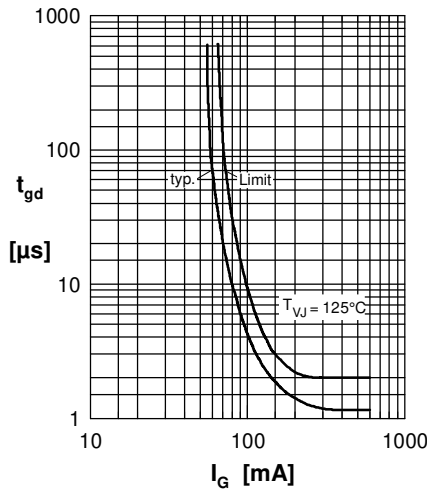


Fig. 5 Gate controlled delay time

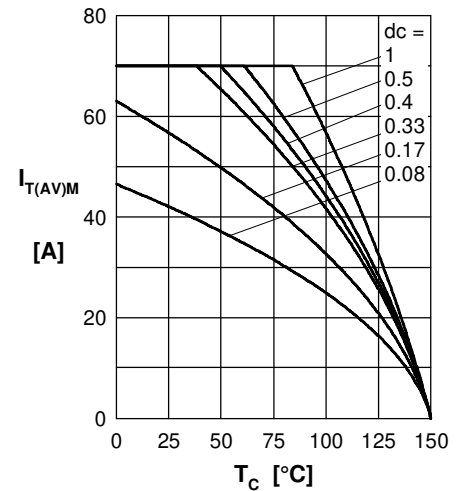


Fig. 6 Max. forward current at case temperature

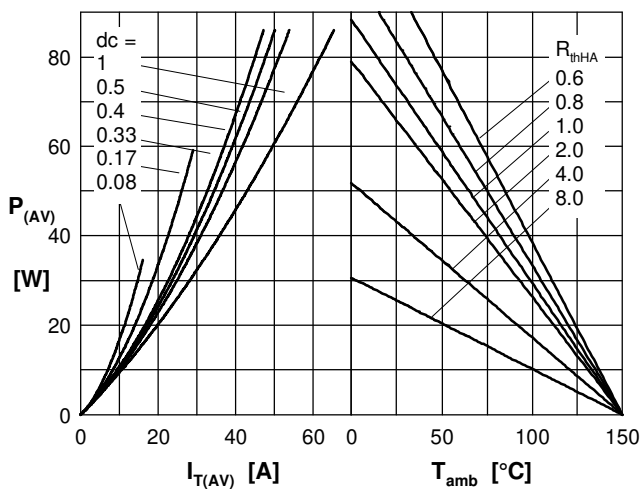
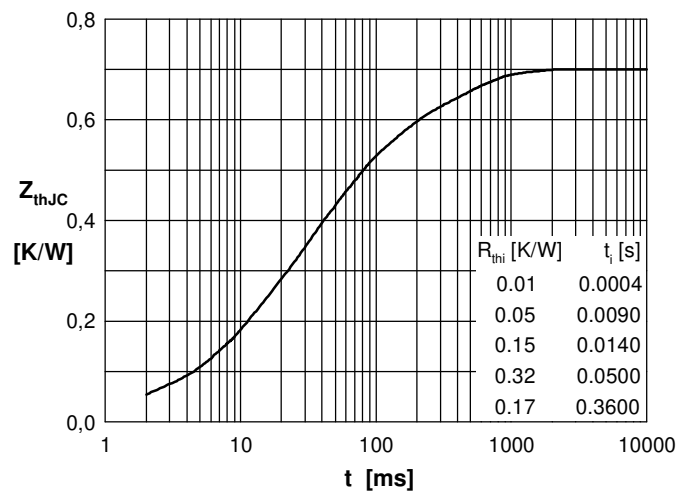

 Fig. 7a Power dissipation versus direct output current  
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance