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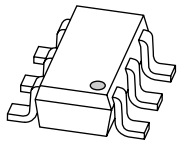
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Kind regards,

Team Nexperia



PBL4005D

40 V PNP BISS loadswitch

Rev. 03 — 6 January 2009

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

1.2 Features

- Low V_{CEsat} (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

Table 1. Quick reference data

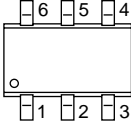
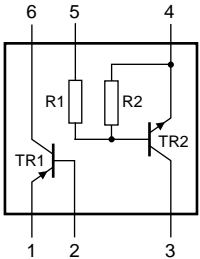
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-40	V
I_C	collector current		[1]	-	-1	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500$ mA; $I_B = -50$ mA	[2]	240	340	m Ω
TR2; NPN resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)		33	47	61	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

[1] Device mounted on a ceramic Printed-Circuit Board (PCB), Al_2O_3 , standard footprint.

[2] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

sym036

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS4005D	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PBLS4005D	R5

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

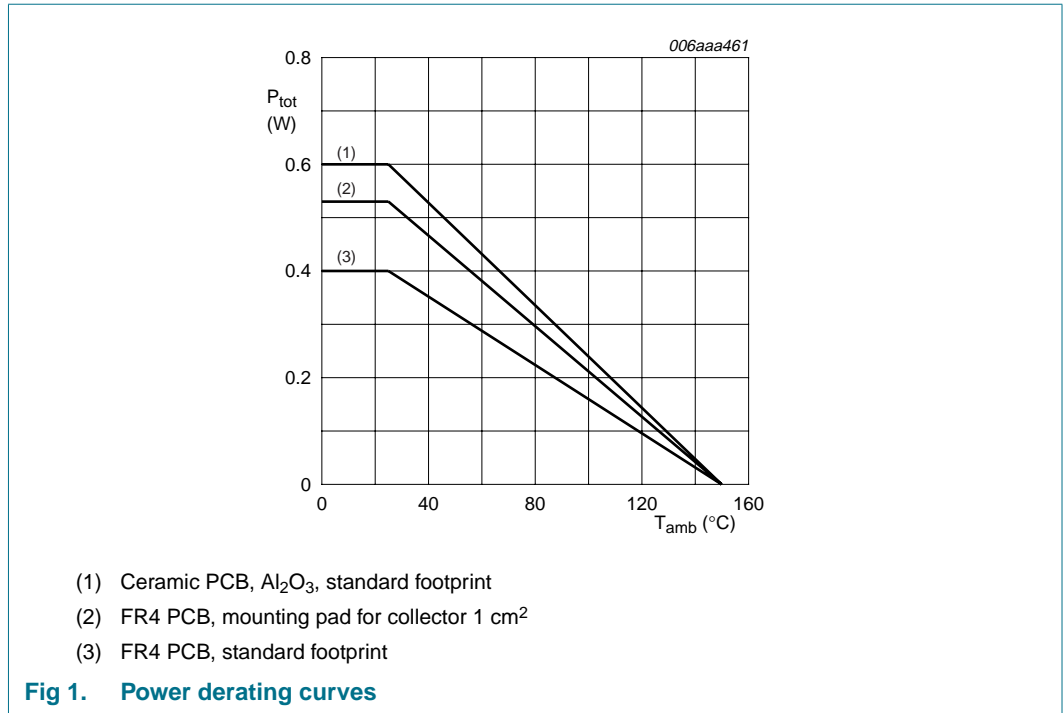
Symbol	Parameter	Conditions	Min	Max	Unit
TR1; PNP low V_{CEsat} transistor					
V_{CBO}	collector-base voltage	open emitter	-	-40	V
V_{CEO}	collector-emitter voltage	open base	-	-40	V
V_{EBO}	emitter-base voltage	open collector	-	-5	V
I_C	collector current	[1]	-	-0.7	A
		[2]	-	-0.85	A
		[3]	-	-1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-2	A
I_B	base current		-	-0.3	A
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	-	-1	A

Table 5. Limiting values ...continued*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW
TR2; NPN resistor-equipped transistor						
V _{CBO}	collector-base voltage	open emitter	-	50	V	
V _{CEO}	collector-emitter voltage	open base	-	50	V	
V _{EBO}	emitter-base voltage	open collector	-	10	V	
V _I	input voltage					
			positive	-	+40	V
			negative	-	-10	V
I _O	output current		-	100	mA	
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	100	mA	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	-	200	mW	
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	400	mW
			[2]	-	530	mW
			[3]	-	600	mW
T _j	junction temperature		-	150	°C	
T _{amb}	ambient temperature		-65	+150	°C	
T _{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

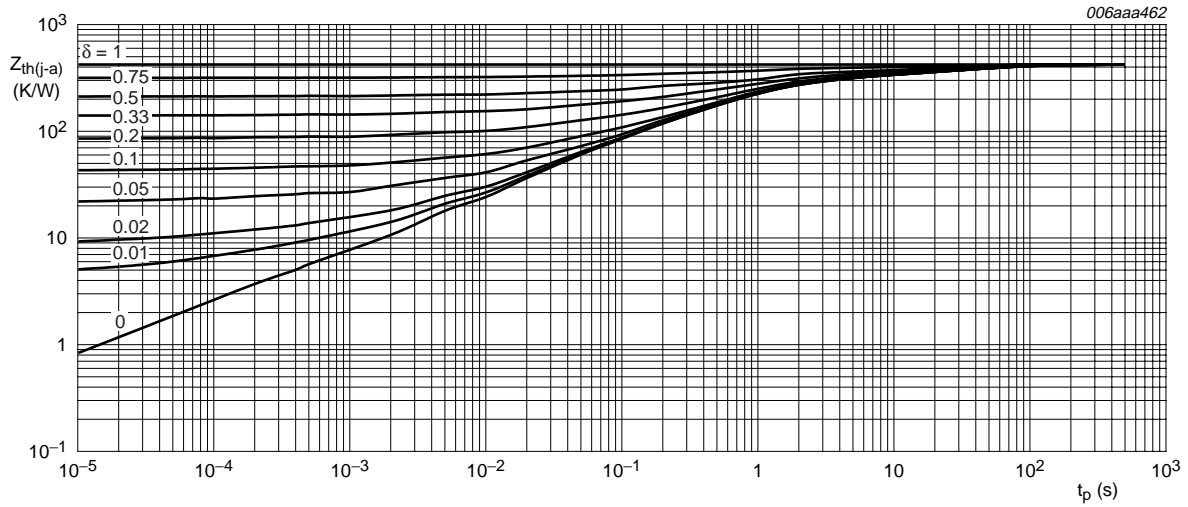


6. Thermal characteristics

Table 6. Thermal characteristics

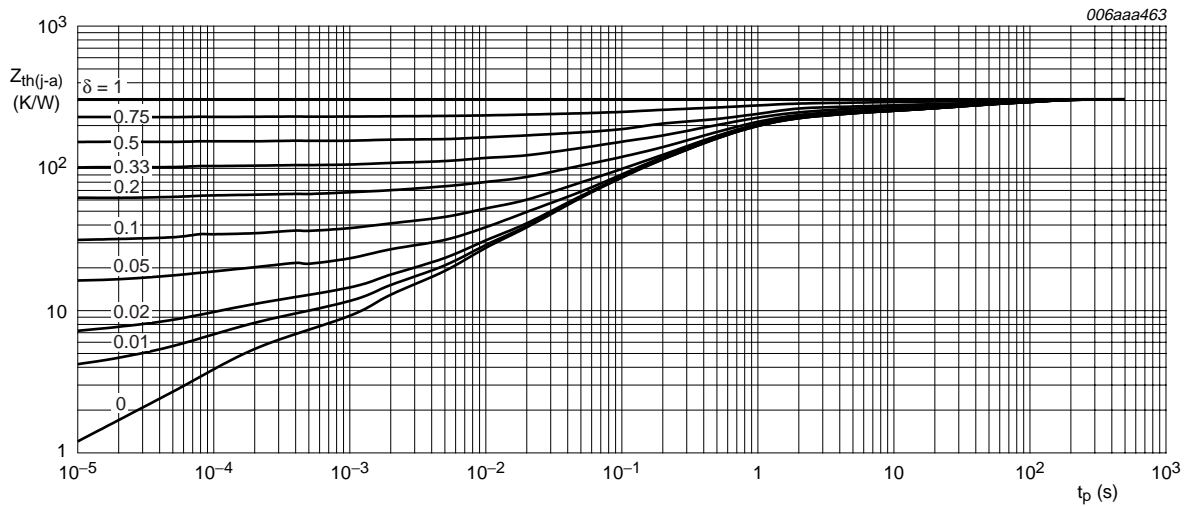
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	312	K/W
			[2]	-	-	236	K/W
			[3]	-	-	210	K/W
Per TR1; PNP low V_{CEsat} transistor							
R _{th(j-sp)}	thermal resistance from junction to solder point		-	-	105	K/W	

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



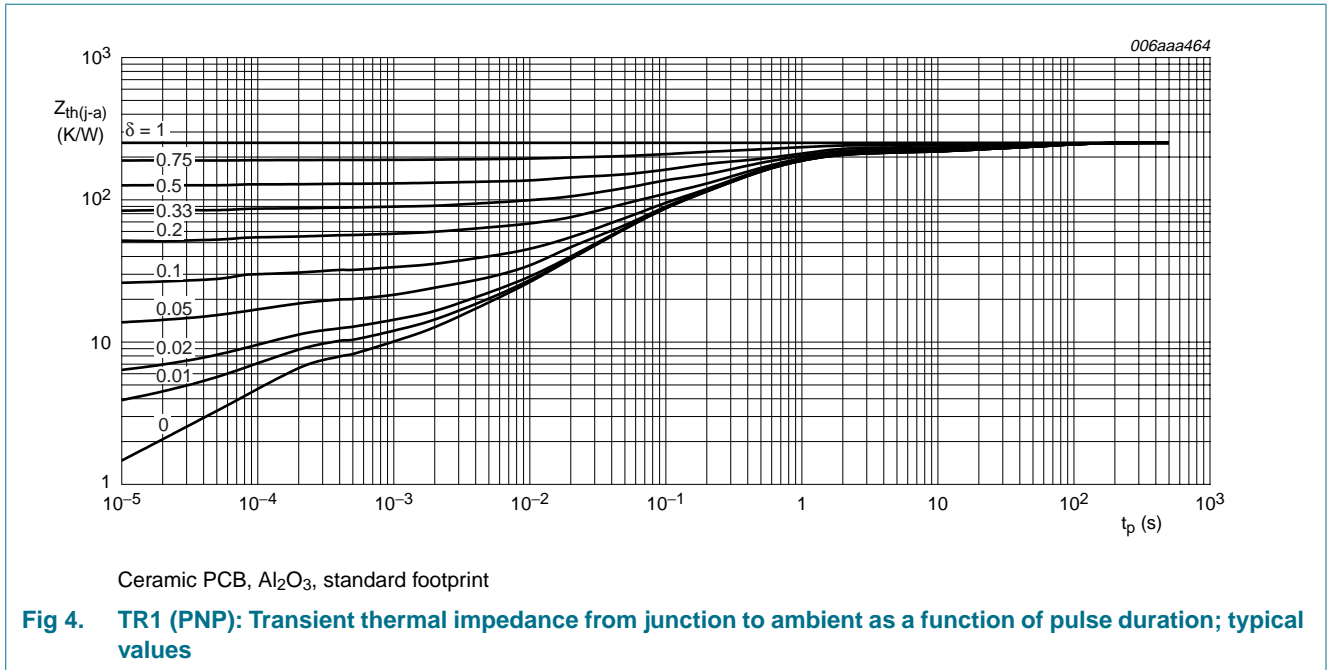
FR4 PCB, standard footprint

Fig 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm²

Fig 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



7. Characteristics

Table 7. Characteristics

T_{amb} = 25 °C unless otherwise specified.

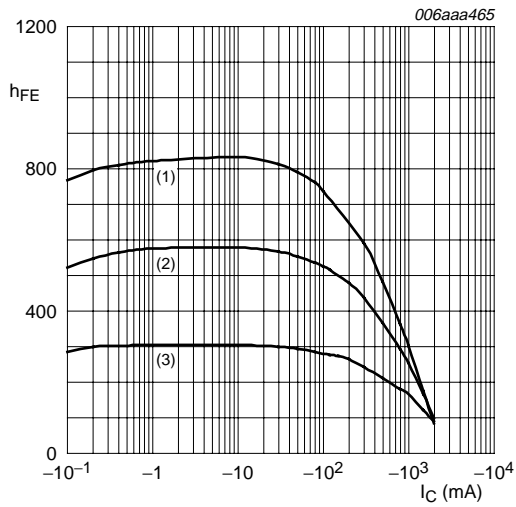
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = -40 V; I _E = 0 A	-	-	-0.1	μA
		V _{CB} = -40 V; I _E = 0 A; T _j = 150 °C	-	-	-50	μA
I _{CES}	collector-emitter cut-off current	V _{CE} = -30 V; V _{BE} = 0 V	-	-	-0.1	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	-	-	-0.1	μA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -1 mA	300	-	-	
		V _{CE} = -5 V; I _C = -100 mA	[1] 300	-	800	
		V _{CE} = -5 V; I _C = -500 mA	[1] 215	-	-	
		V _{CE} = -5 V; I _C = -1 A	[1] 150	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -100 mA; I _B = -1 mA	-	-80	-140	mV
		I _C = -500 mA; I _B = -50 mA	[1] -	-120	-170	mV
		I _C = -1 A; I _B = -100 mA	[1] -	-220	-310	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -500 mA; I _B = -50 mA	[1] -	240	340	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -1 A; I _B = -50 mA	[1] -	-	-1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = -5 V; I _C = -1 A	[1] -	-	-1	V

Table 7. Characteristics ...continued

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

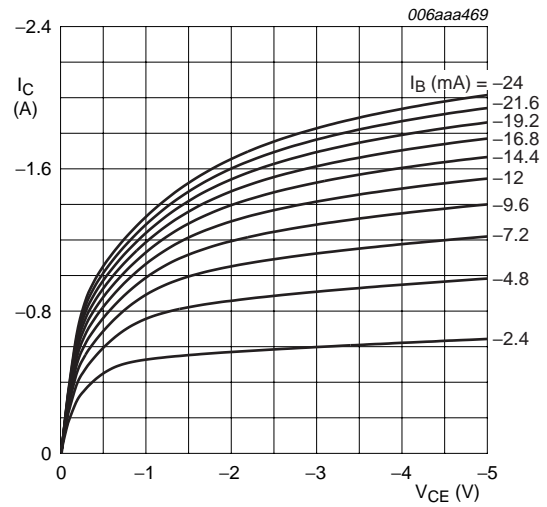
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_T	transition frequency	$I_C = -50\text{ mA}$; $V_{CE} = -10\text{ V}$; $f = 100\text{ MHz}$	150	-	-	MHz
C_C	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = i_e = 0\text{ A}$; $f = 1\text{ MHz}$	-	-	12	pF
TR2; NPN resistor-equipped transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$	-	-	90	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ }\mu\text{A}$	-	1.2	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 2\text{ mA}$	3	1.6	-	V
R1	bias resistor 1 (input)		33	47	61	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	
C_C	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = i_e = 0\text{ A}$; $f = 1\text{ MHz}$	-	-	2.5	pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.



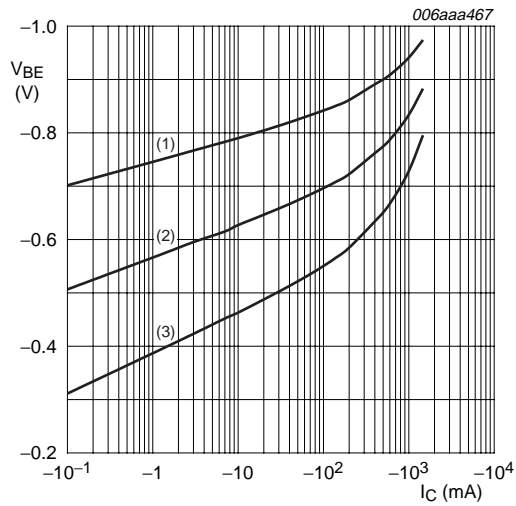
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -55\text{ }^\circ\text{C}$

Fig 5. TR1 (PNP): DC current gain as a function of collector current; typical values



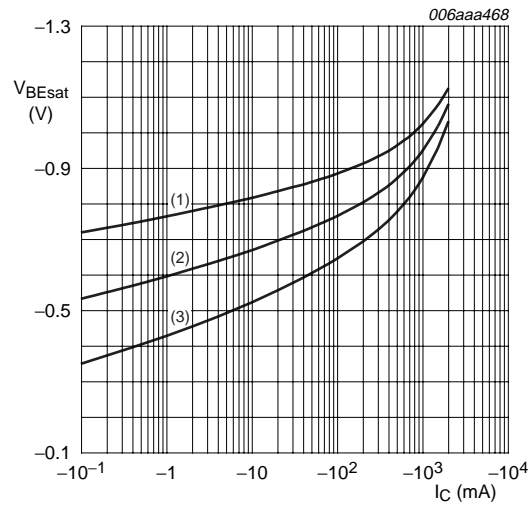
$T_{amb} = 25\text{ }^\circ\text{C}$

Fig 6. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



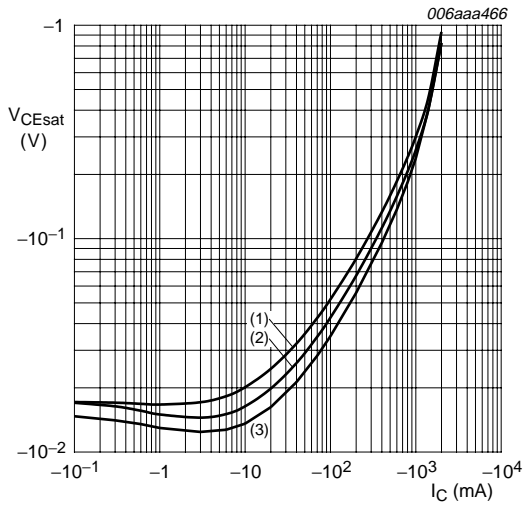
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = -55\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

Fig 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



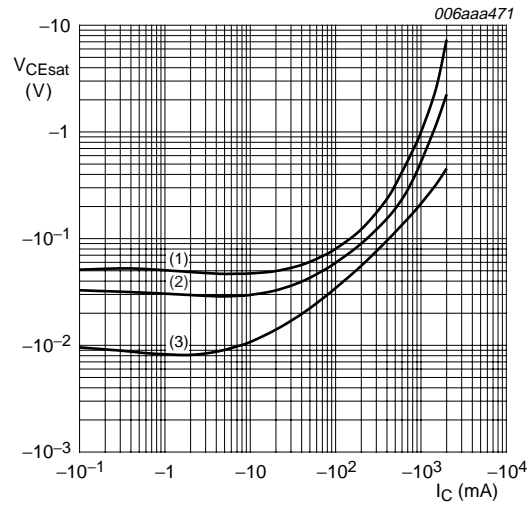
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

Fig 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



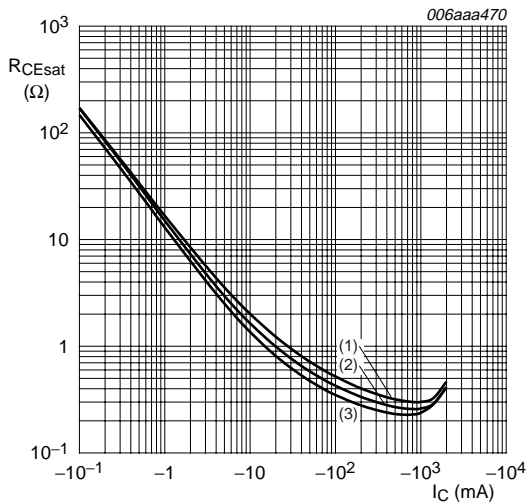
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 9. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



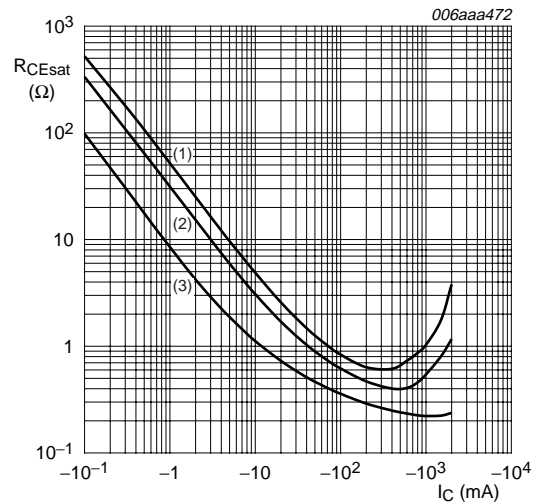
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 10. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



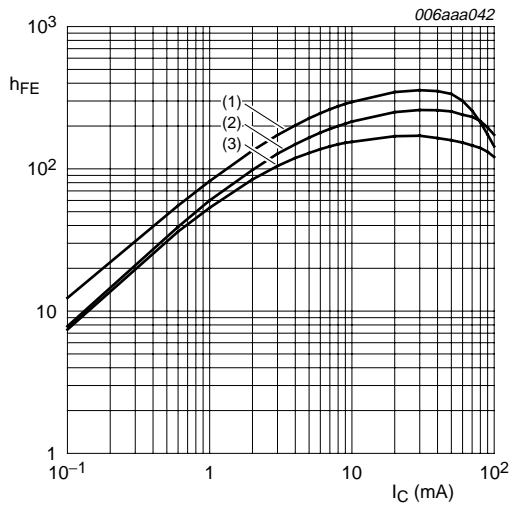
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 11. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



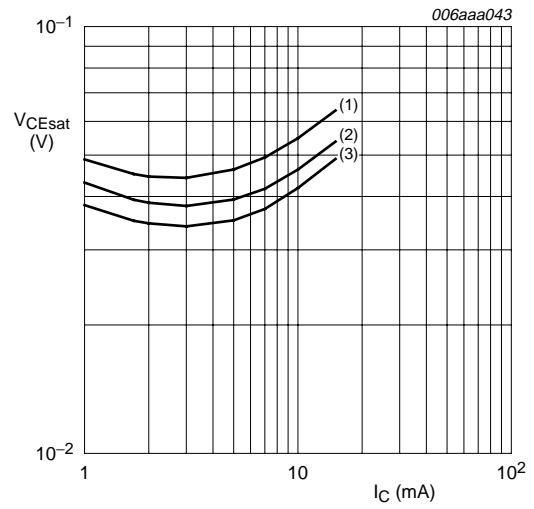
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



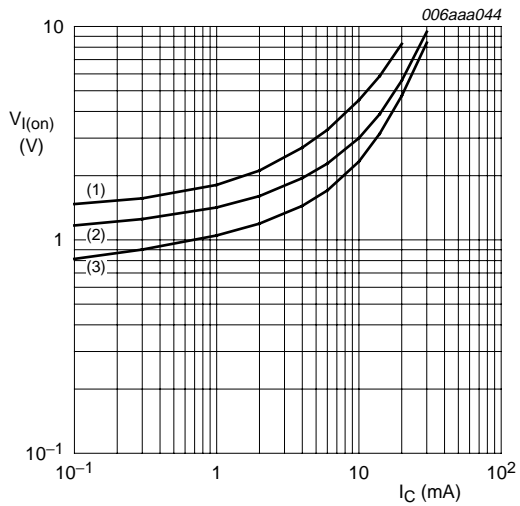
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 150 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 13. TR2 (NPN): DC current gain as a function of collector current; typical values



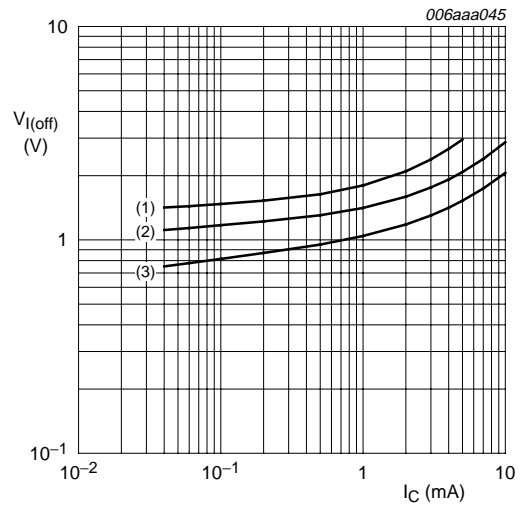
$I_C/I_B = 20$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

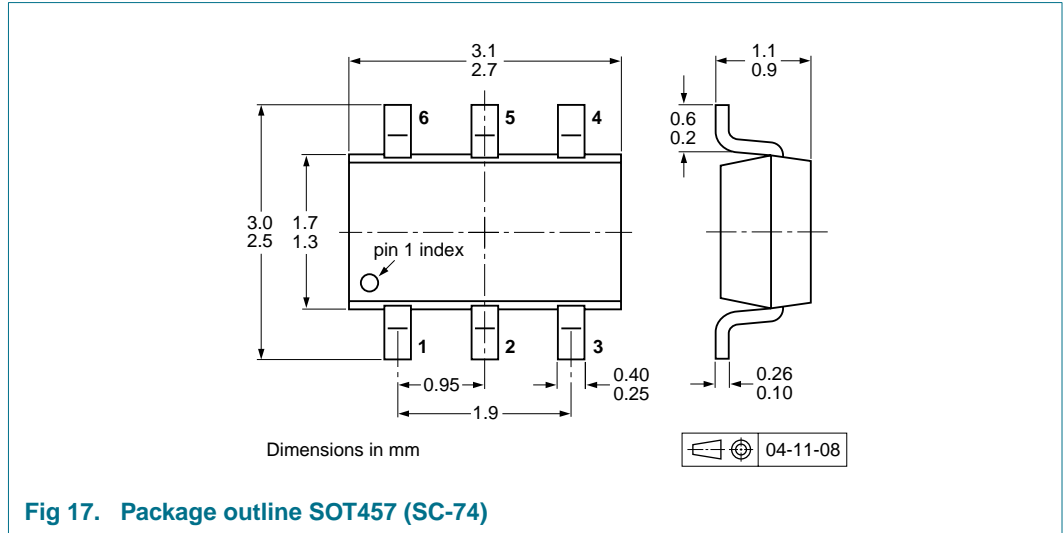
Fig 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values



$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

8. Package outline



9. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PBLS4005D	SOT457	4 mm pitch, 8 mm tape and reel; T1	^[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	^[3] -125	-165

[1] For further information and the availability of packing methods, see [Section 13](#).

[2] T1: normal taping

[3] T2: reverse taping

10. Soldering

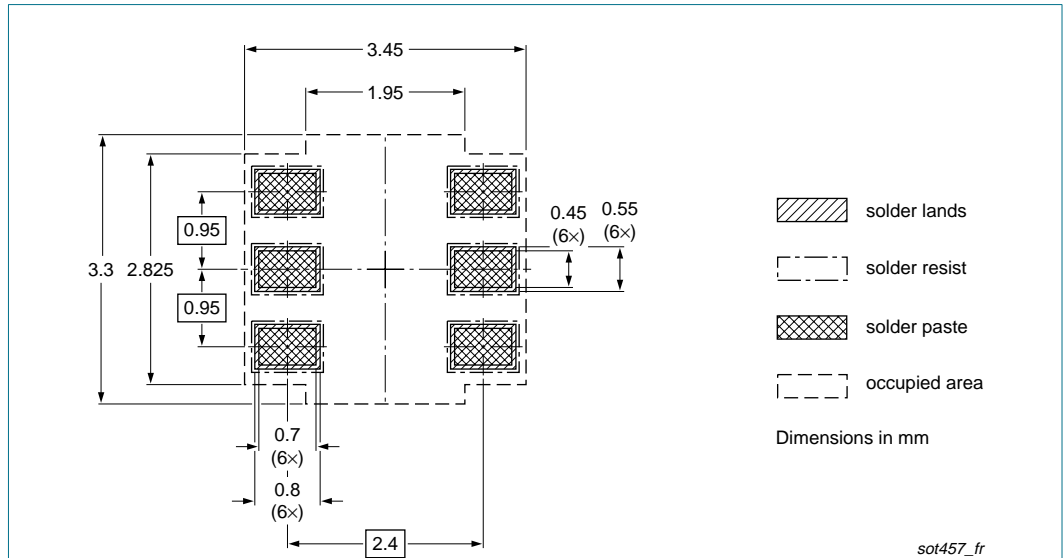


Fig 18. Reflow soldering footprint SOT457 (SC-74)

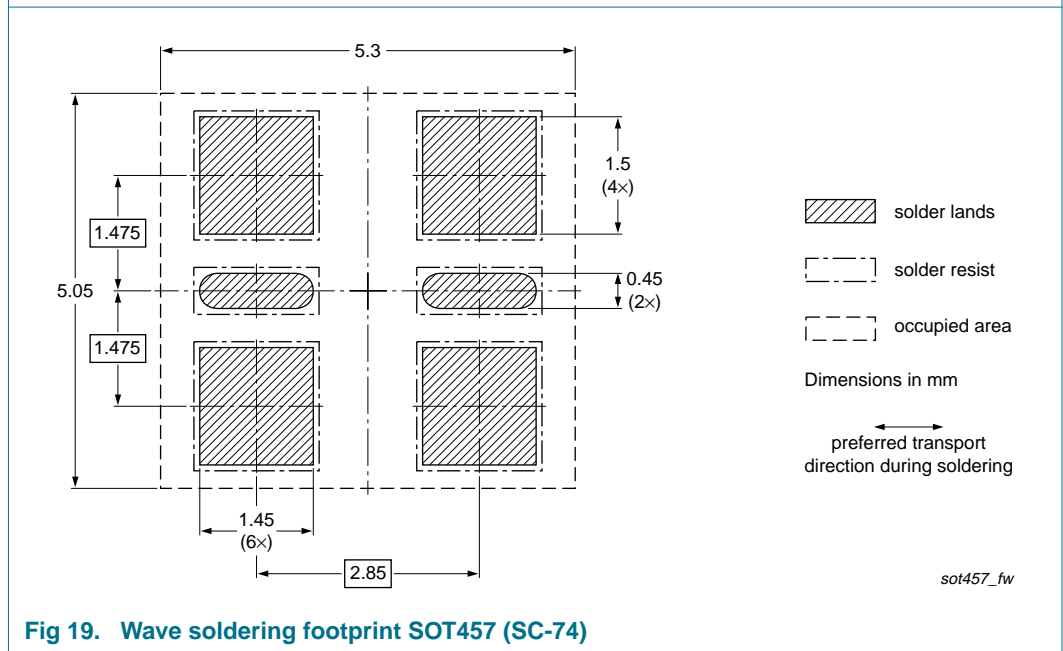


Fig 19. Wave soldering footprint SOT457 (SC-74)

11. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBL54005D_3	20090106	Product data sheet	-	PBL54005D_2
Modifications:		<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Figure 5, 9 and 10: amended• Section 12 "Legal information": updated		
PBL54005D_2	20050719	Product data sheet	-	PBL54005D_1
PBL54005D_1	20041201	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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