



PSMN022-30BL

N-channel 30 V 22.6 mΩ logic level MOSFET in D2PAK

Rev. 1 — 21 March 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

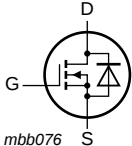
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	30	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	41	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _j = 100 °C; see Figure 13	-	26.84	31.6	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _j = 25 °C; see Figure 12	-	19.17	22.6	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 5 A; V _{DS} = 15 V; see Figure 14 ; see Figure 15	-	1.4	-	nC
Q _{G(tot)}	total gate charge		-	4.4	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 30 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	-	7	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN022-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN022-30BL	PSMN022-30BL

5. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	22	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	-	30	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	125	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	41	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	30	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	125	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 30 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	7	mJ

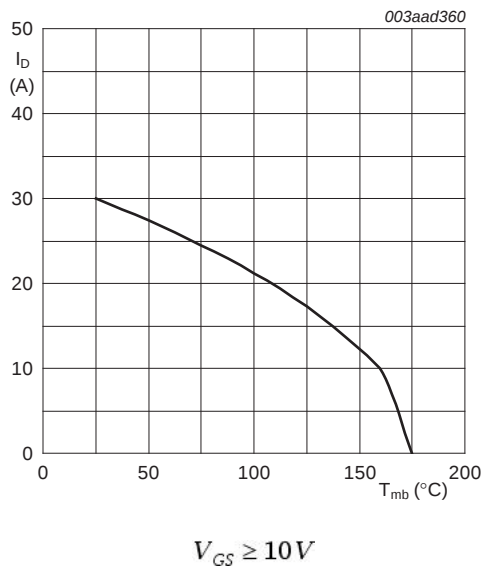


Fig 1. Continuous drain current as a function of mounting base temperature

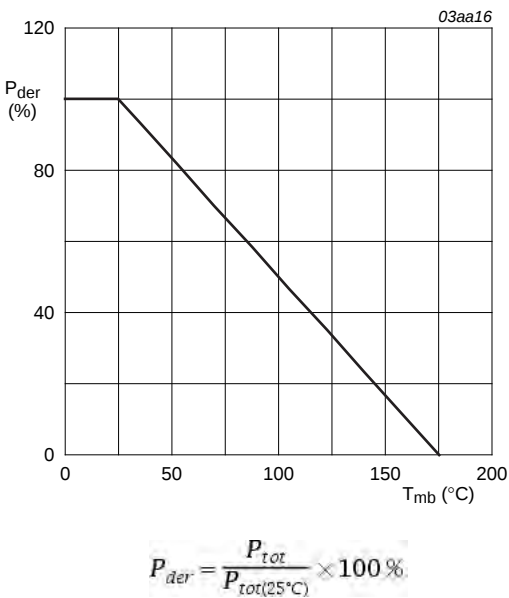


Fig 2. Normalized total power dissipation as a function of mounting base temperature

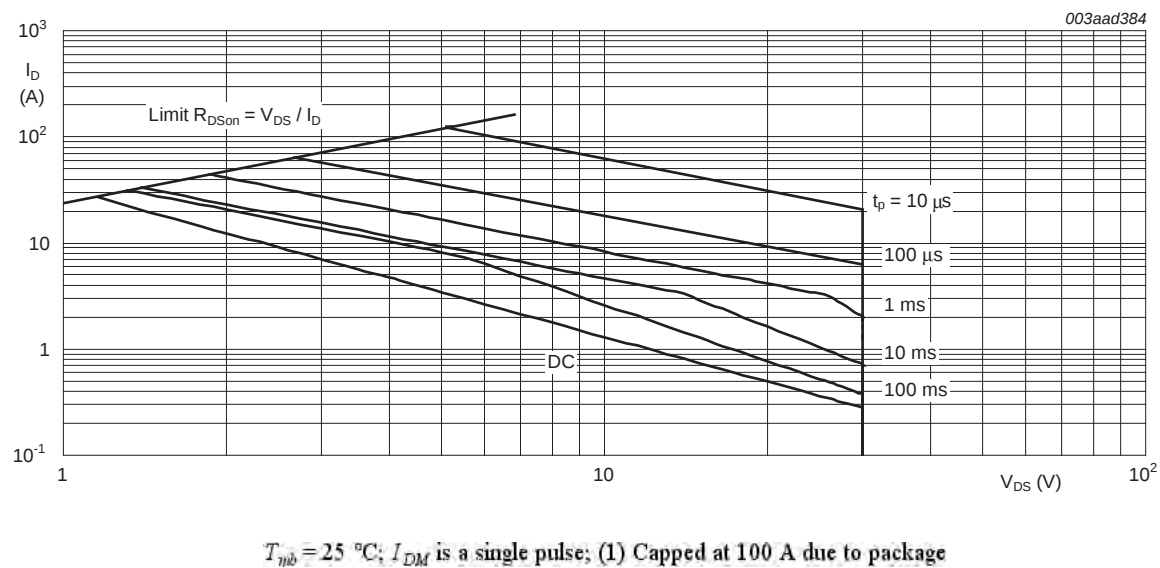


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	3.1	3.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed circuit board	-	50	-	K/W

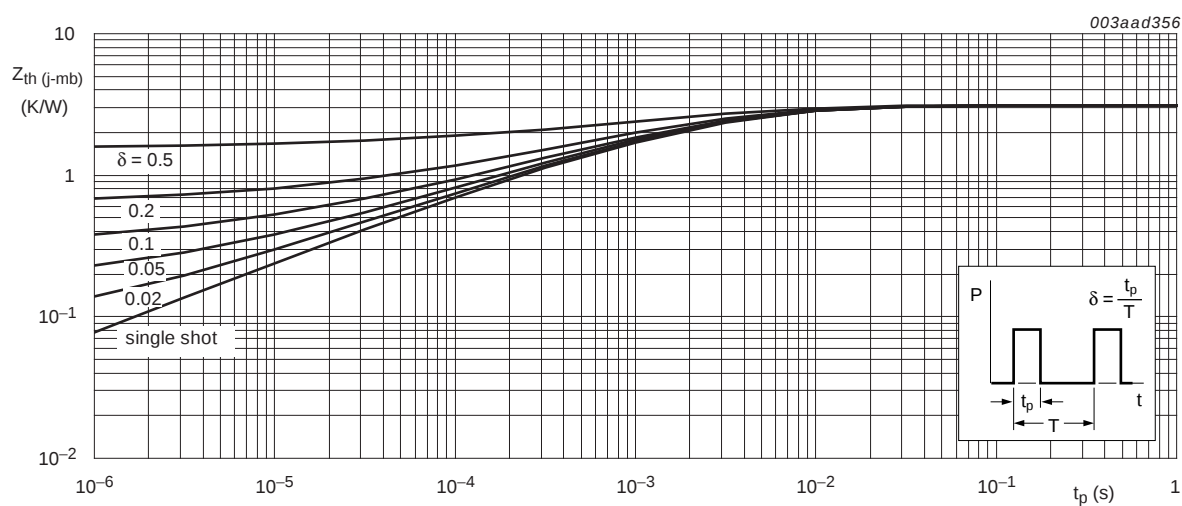


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$; see Figure 10 ; see Figure 11	1.3	1.7	2.15	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 175\ ^\circ C$; see Figure 11	0.5	-	-	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ C$; see Figure 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	0.3	1	μA
		$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_j = 125\ ^\circ C$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 5\ A$; $T_j = 25\ ^\circ C$; see Figure 12	-	25.17	29.6	mΩ
		$V_{GS} = 10\ V$; $I_D = 5\ A$; $T_j = 175\ ^\circ C$; see Figure 13 ; see Figure 12	-	50.99	60	mΩ
		$V_{GS} = 10\ V$; $I_D = 5\ A$; $T_j = 100\ ^\circ C$; see Figure 13	-	26.84	31.6	mΩ
		$V_{GS} = 10\ V$; $I_D = 5\ A$; $T_j = 25\ ^\circ C$; see Figure 12	-	19.17	22.6	mΩ
R_G	gate resistance	$f = 1\ MHz$	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5\ A$; $V_{DS} = 15\ V$; $V_{GS} = 10\ V$; see Figure 14 ; see Figure 15	-	9	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	8	-	nC
		$I_D = 5\ A$; $V_{DS} = 15\ V$; $V_{GS} = 4.5\ V$; see Figure 14 ; see Figure 15	-	4.4	-	nC
Q_{GS}	gate-source charge		-	1.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	0.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.8	-	nC
Q_{GD}	gate-drain charge		-	1.4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5\ A$; $V_{DS} = 15\ V$; see Figure 14 ; see Figure 15	-	3	-	V
C_{iss}	input capacitance	$V_{DS} = 15\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_j = 25\ ^\circ C$; see Figure 16	-	447	-	pF
C_{oss}	output capacitance		-	96	-	pF
C_{rss}	reverse transfer capacitance		-	61	-	pF

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 1.5 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 4.7 Ω	-	12	-	ns
t _r	rise time		-	29	-	ns
t _{d(off)}	turn-off delay time		-	17	-	ns
t _f	fall time		-	7	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 17	-	0.7	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	-	22	-	ns
Q _r	recovered charge	V _{DS} = 15 V	-	10	-	nC

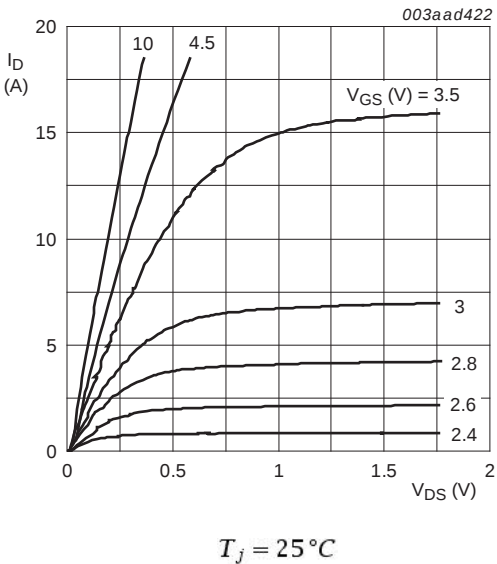


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

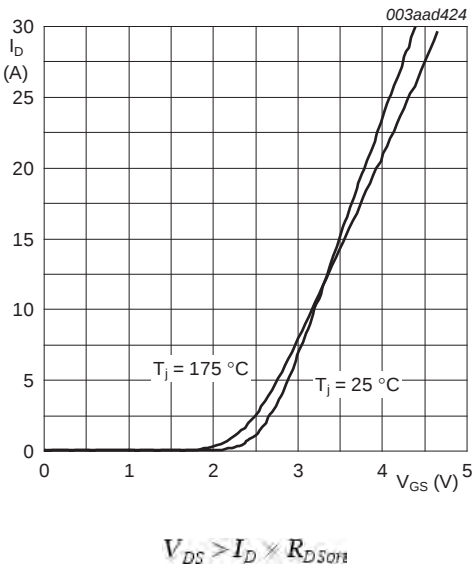
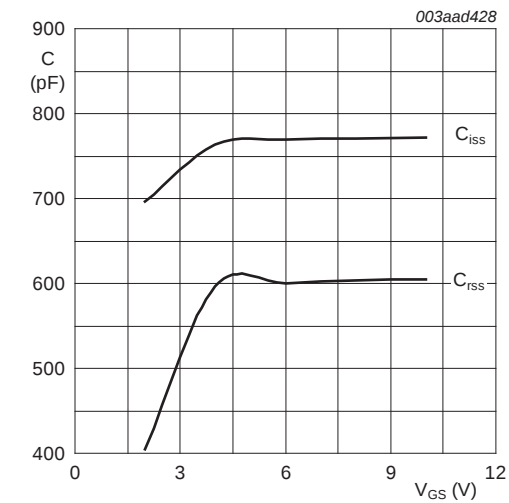
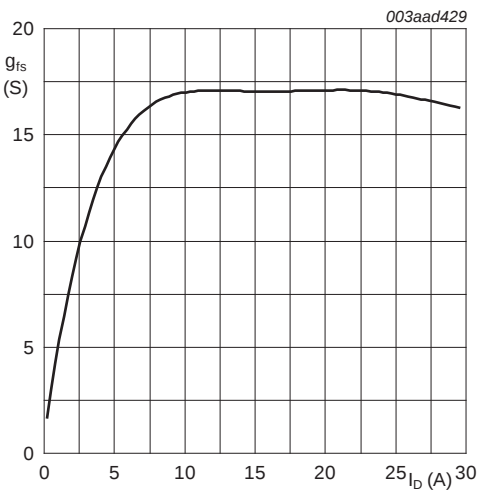


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



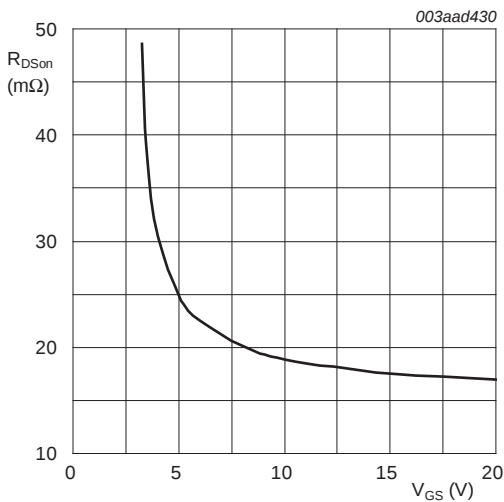
$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



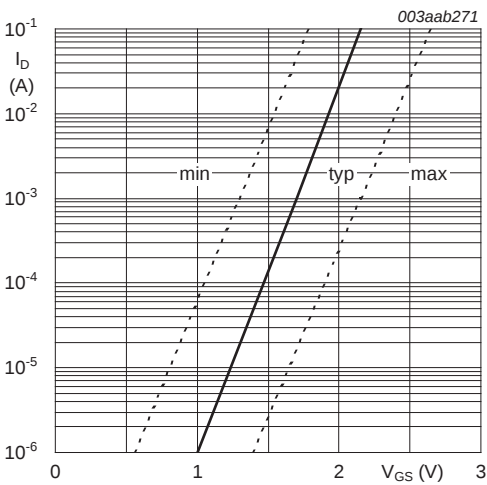
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{ V}$

Fig 8. Forward transconductance as a function of drain current; typical values



$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

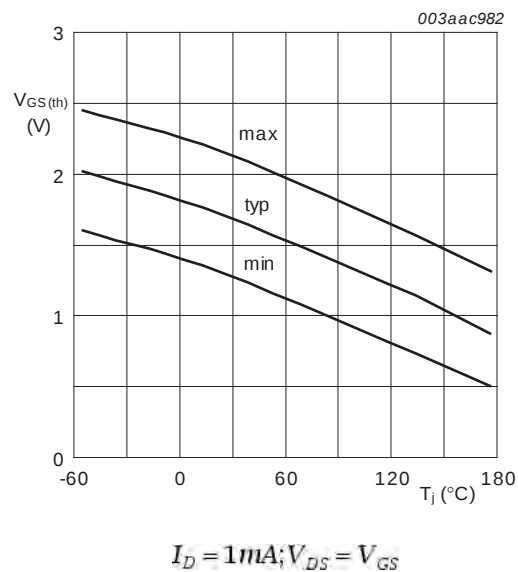


Fig 11. Gate-source threshold voltage as a function of junction temperature

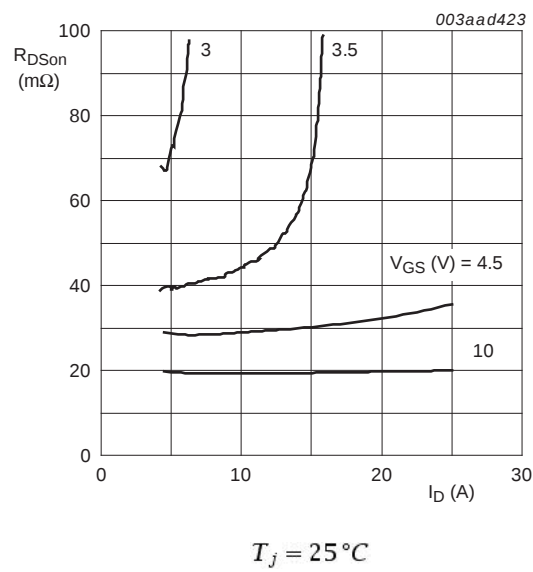


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

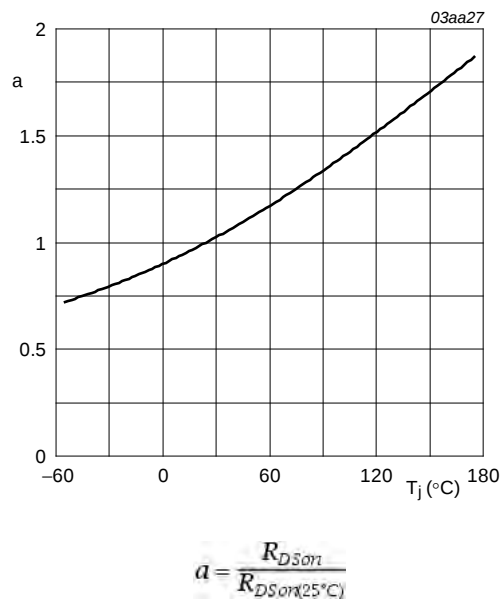


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

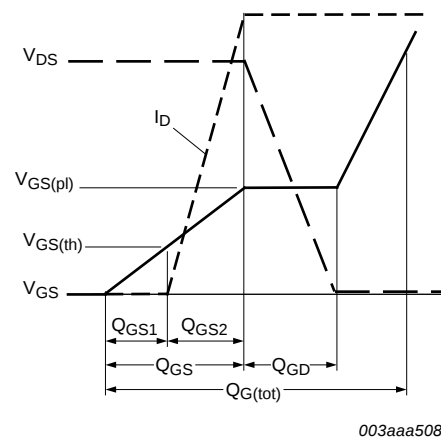


Fig 14. Gate charge waveform definitions

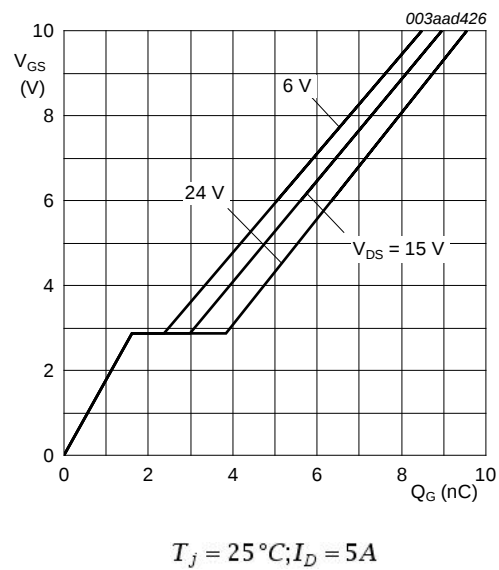


Fig 15. Gate-source voltage as a function of gate charge; typical values

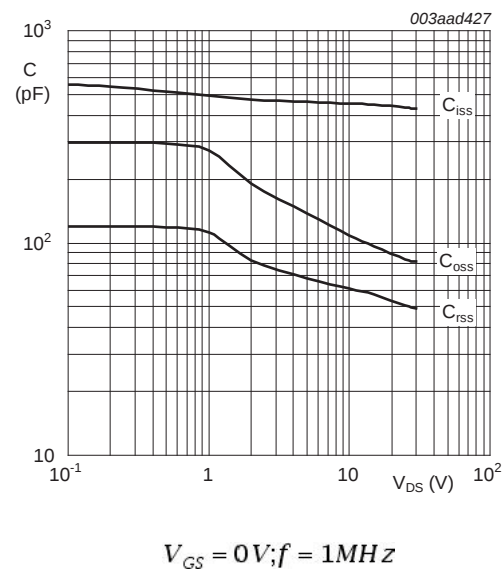


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

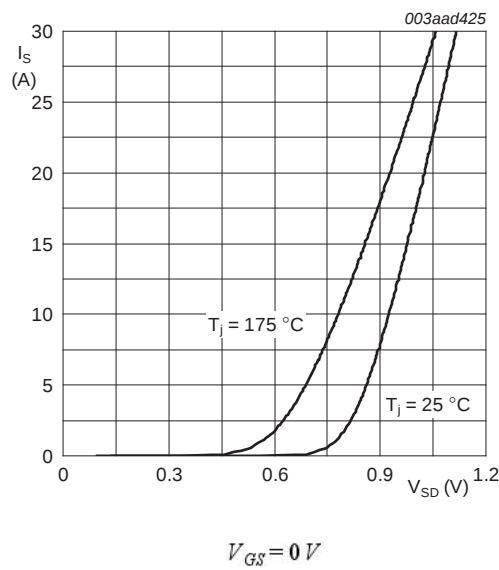
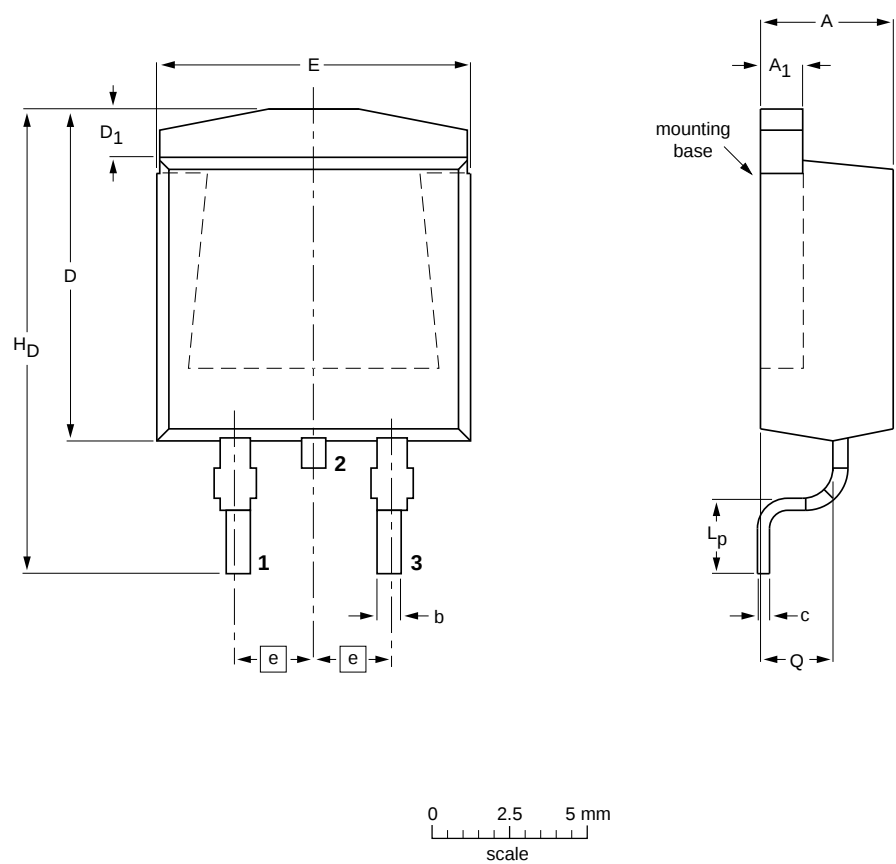


Fig 17. Source current as a function of source-drain voltage;

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN022-30BL v.1	20120321	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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