



PMPB14R0EP

30 V, P-channel Trench MOSFET

13 October 2020

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020M-6 (SOT1220-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portable devices
- Computing power management

4. Quick reference data

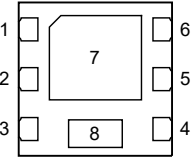
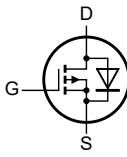
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}$; $T_{amb} = 25\text{ °C}$; $t \leq 5\text{ s}$	[1]	-	-	-12	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -8.5\text{ A}$; $T_j = 25\text{ °C}$		-	14	16	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view DFN2020M-6 (SOT1220-2)	 017aaa094
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB14R0EP	DFN2020M-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB14R0EP	ZG

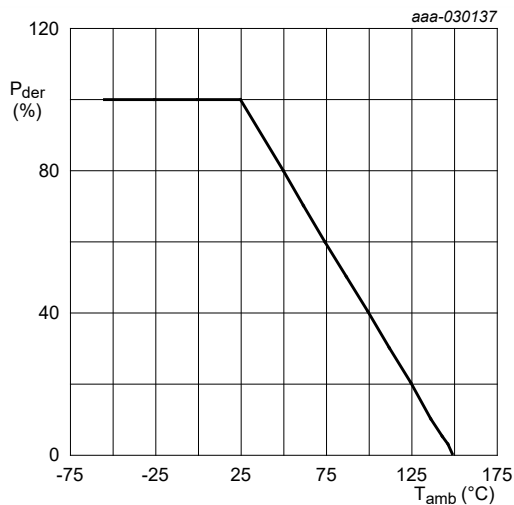
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

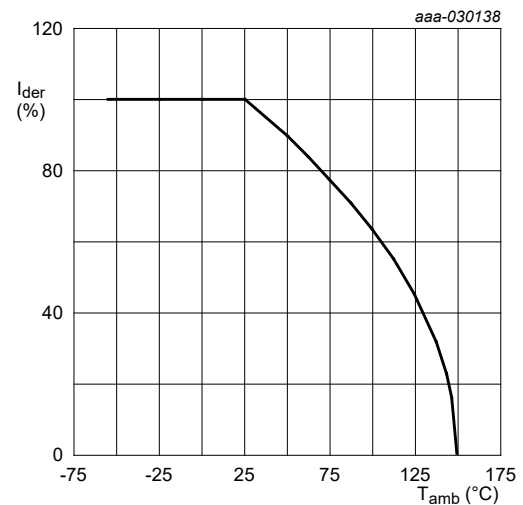
Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-12	A
		V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-9	A
		V _{GS} = -10 V; T _{amb} = 100 °C	[1]	-	-5.4	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-34	A
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	3.8	W
		T _{amb} = 25 °C	[1]	-	1.9	W
		T _{sp} = 25 °C		-	12.5	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.6	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



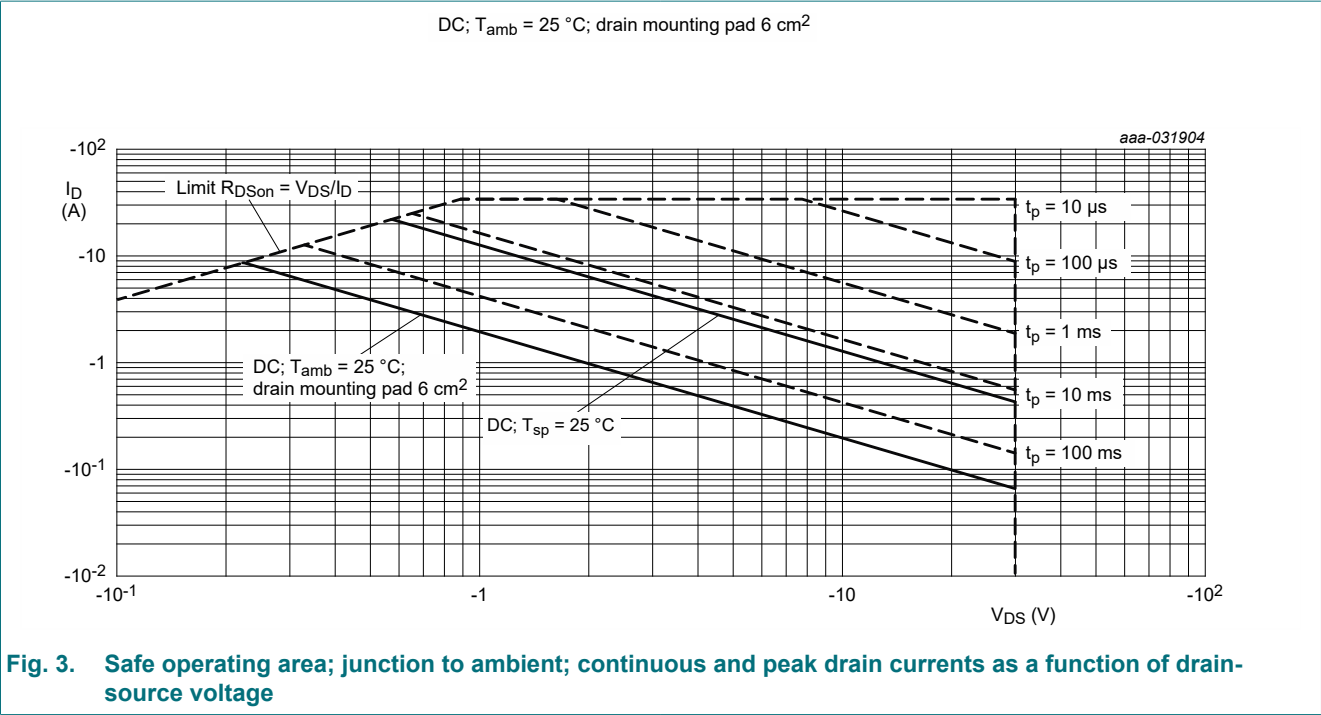
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}\text{C})} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	57	66	K/W
		in free air; $t \leq 5$ s	[2]	-	29	33	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	6	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

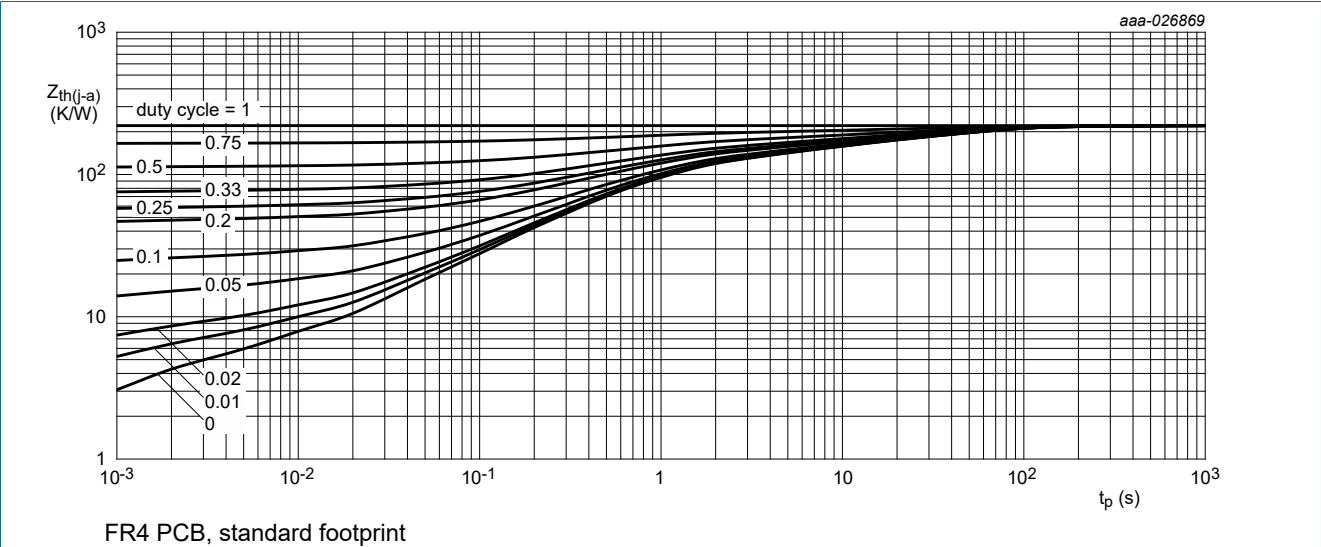


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

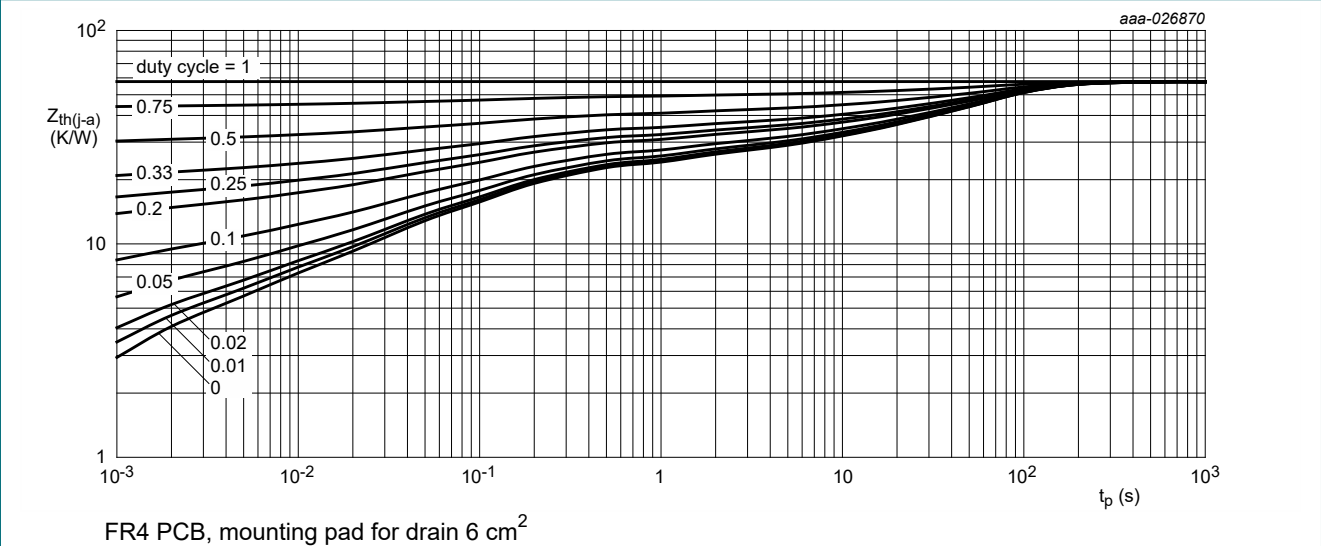


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-1	-1.6	-2	V
I _{DSS}	drain leakage current	V _{DS} = -30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -8.5 A; T _j = 25 °C		-	14	16	mΩ
		V _{GS} = -10 V; I _D = -8.5 A; T _j = 150 °C		-	23	26	mΩ
		V _{GS} = -4.5 V; I _D = -6.9 A; T _j = 25 °C		-	18	24	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -8 A; T _j = 25 °C		-	18.2	-	S
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -15 V; I _D = -8 A; V _{GS} = -10 V; T _j = 25 °C		-	26.6	40	nC
Q _{GS}	gate-source charge			-	3	-	nC
Q _{GD}	gate-drain charge			-	5.2	-	nC
C _{iss}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	227	-	pF
C _{oss}	output capacitance			-	138	-	pF
C _{rss}	reverse transfer capacitance			-	17	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -15 V; I _D = -8 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	2	-	ns
t _r	rise time			-	4	-	ns
t _{d(off)}	turn-off delay time			-	145	-	ns
t _f	fall time			-	83	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -1.6 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V

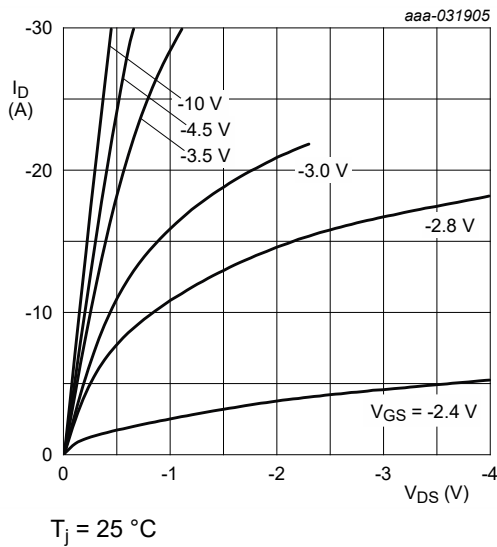


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

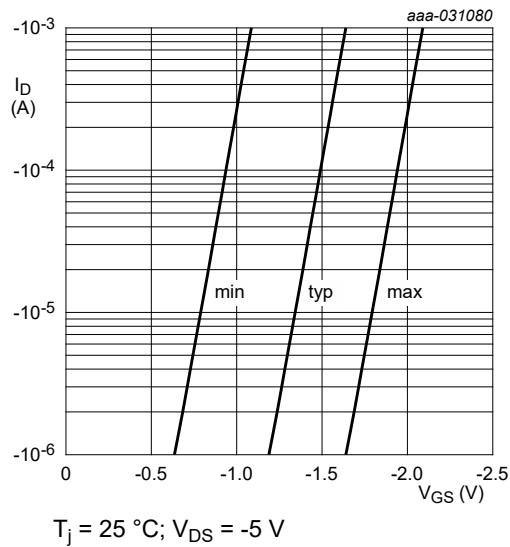


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

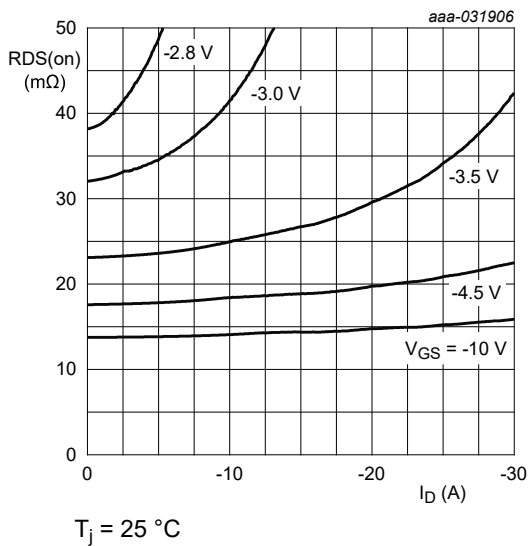


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

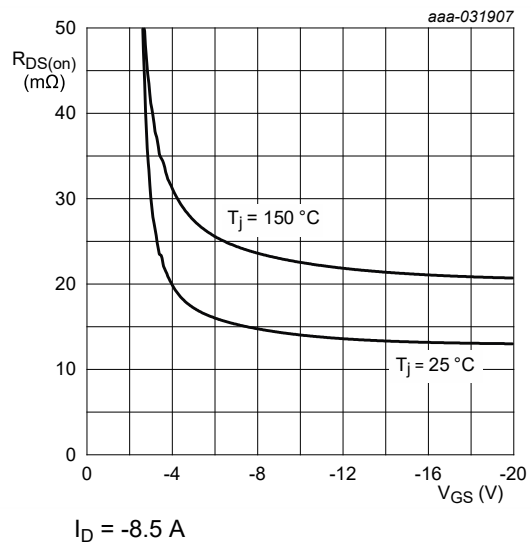


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

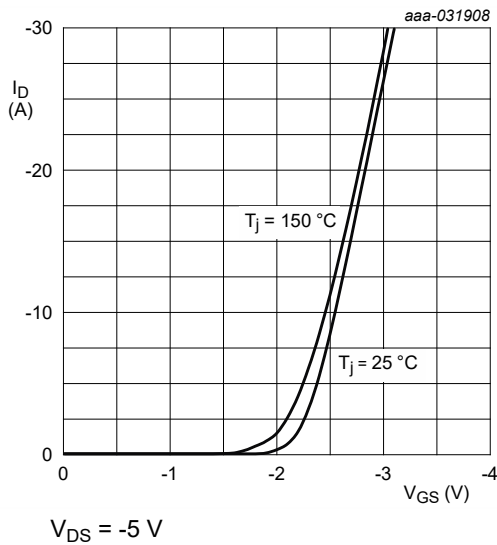


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

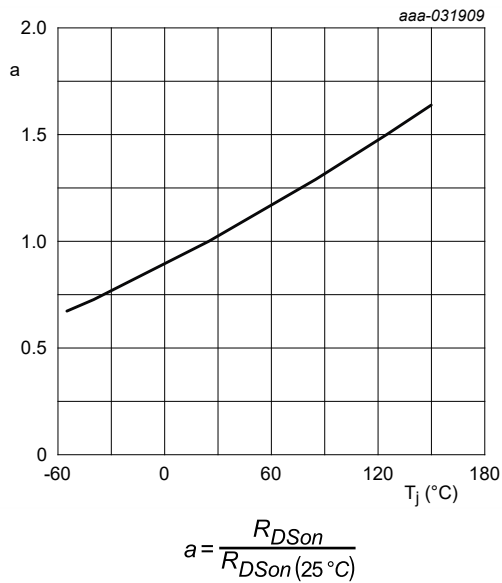


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

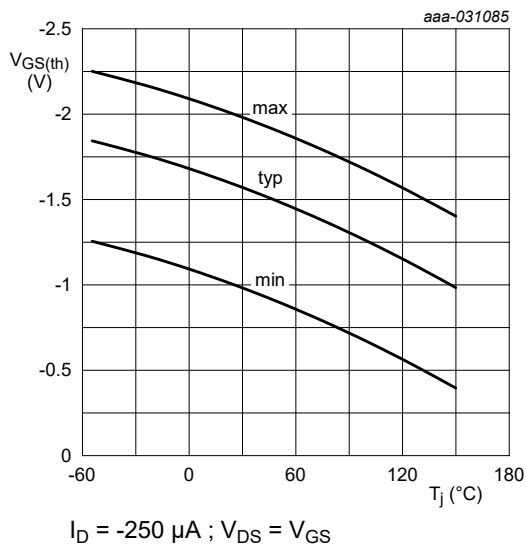


Fig. 12. Gate-source threshold voltage as a function of junction temperature

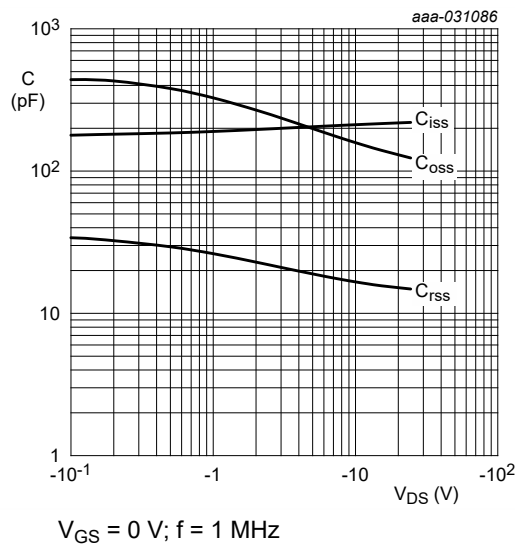


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

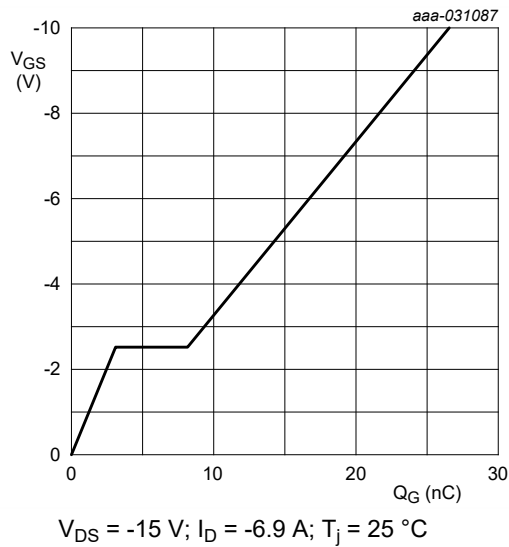


Fig. 14. Gate-source voltage as a function of gate charge; typical values

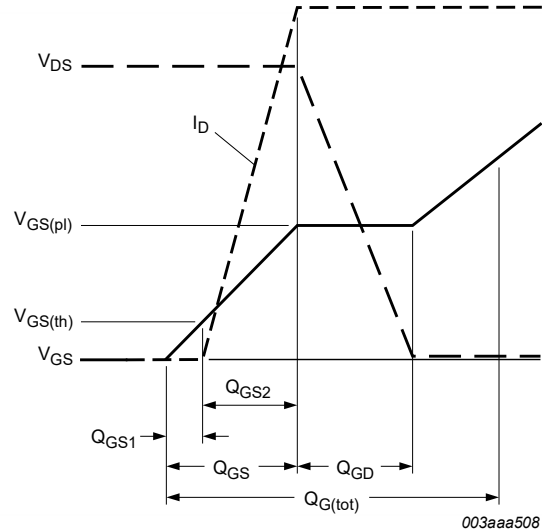


Fig. 15. Gate charge waveform definitions

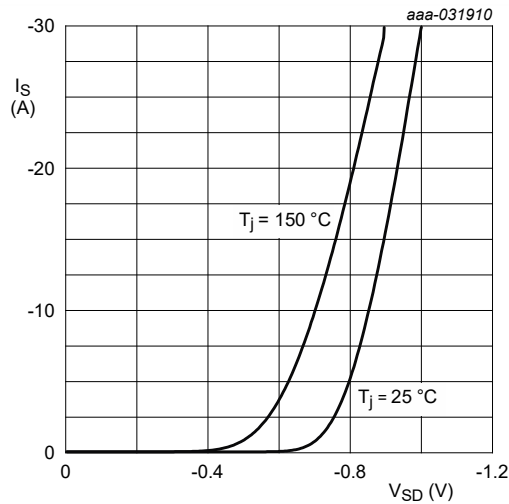


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

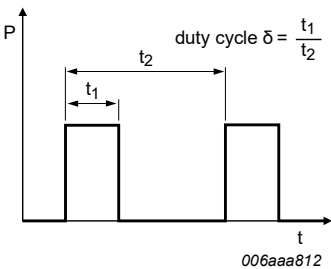


Fig. 17. Duty cycle definition

12. Package outline

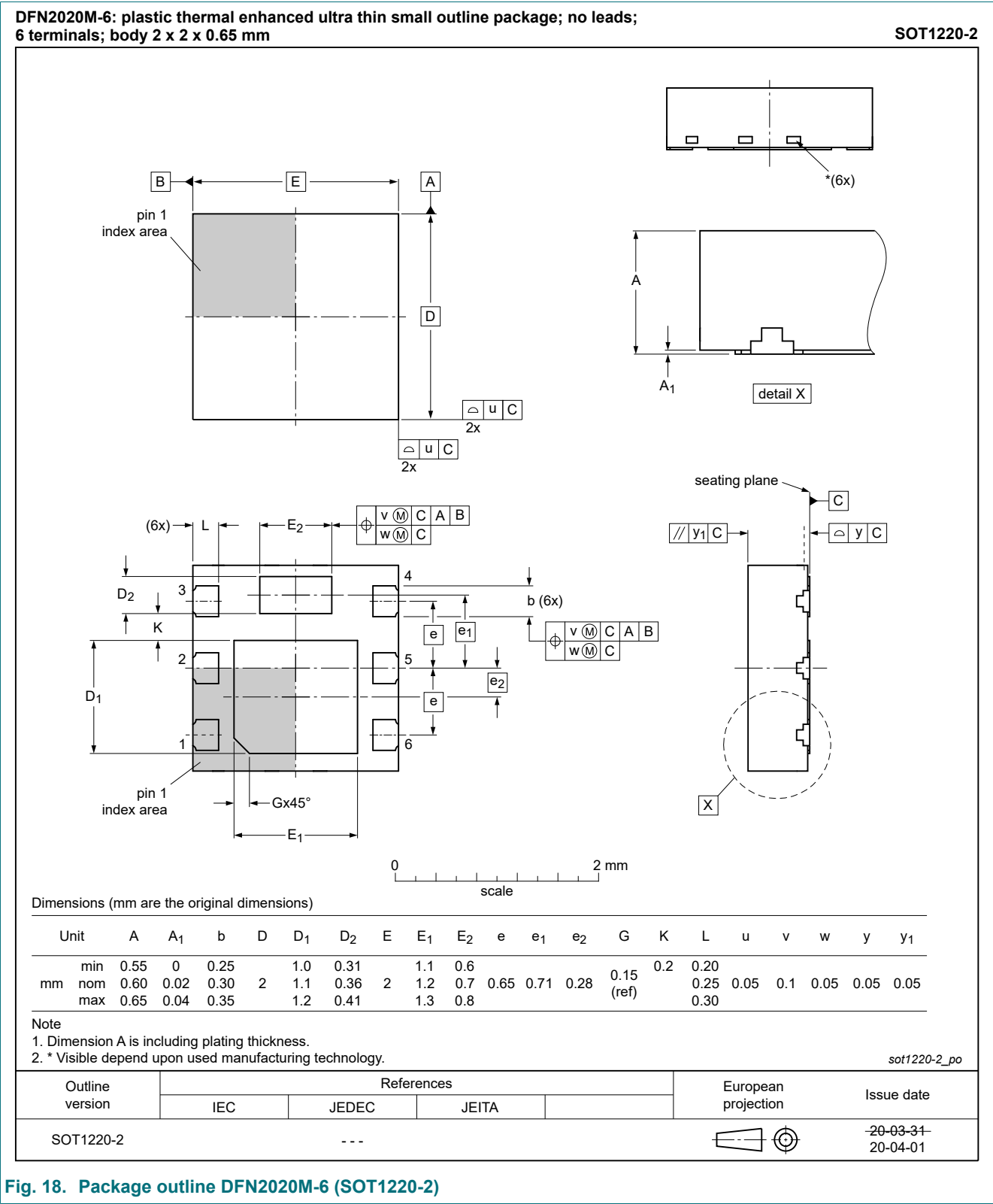


Fig. 18. Package outline DFN2020M-6 (SOT1220-2)

13. Soldering

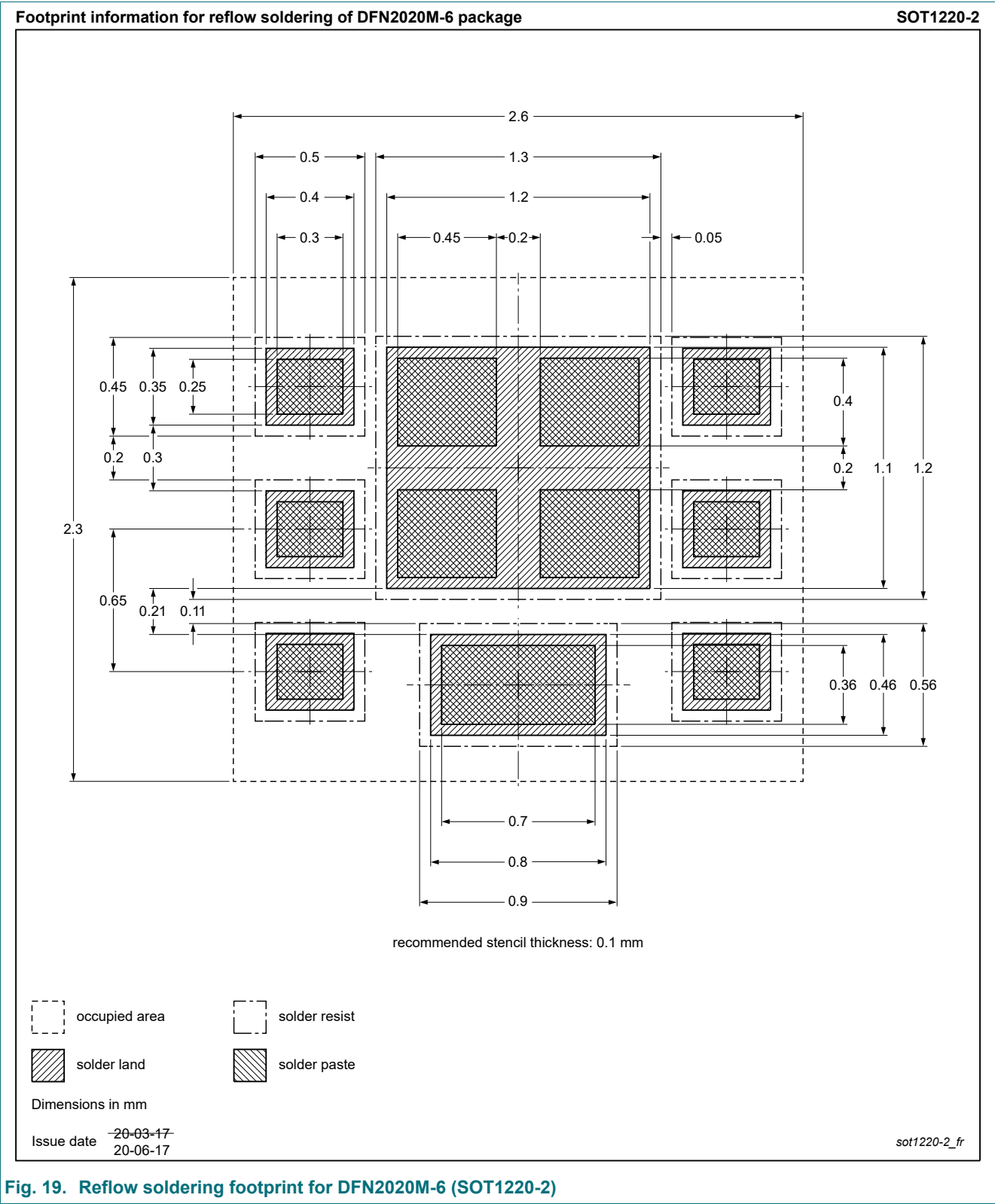


Fig. 19. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB14R0EP v.1	20201013	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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