



PMN42XPEA

20 V, P-channel Trench MOSFET

21 March 2014

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Fast switching
- Trench MOSFET technology
- 2 kV ESD protection
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

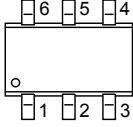
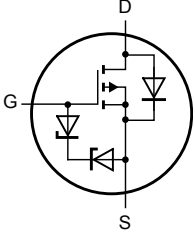
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	-20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t \leq 5\text{ s}$	[1]	-	-	-5.7	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -3\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	41	46	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 TSOP6 (SOT457)	 017aaa259
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN42XPEA	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN42XPEA	B9

8. Limiting values

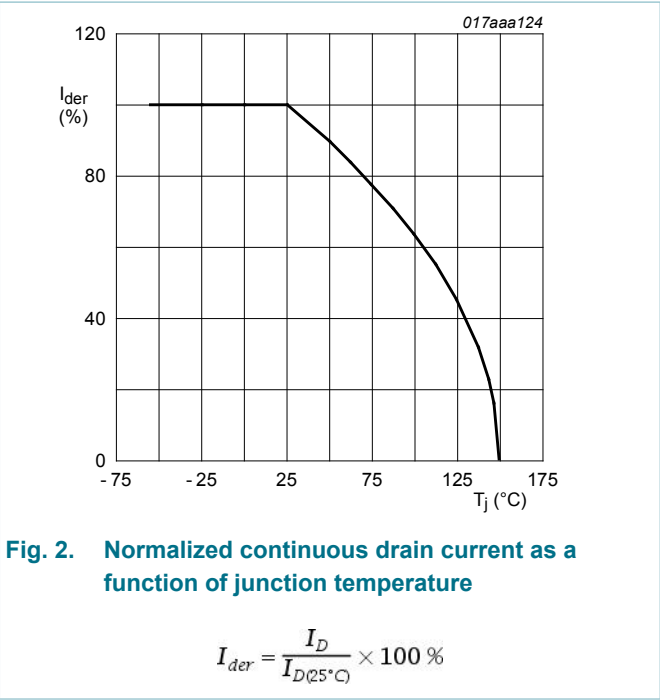
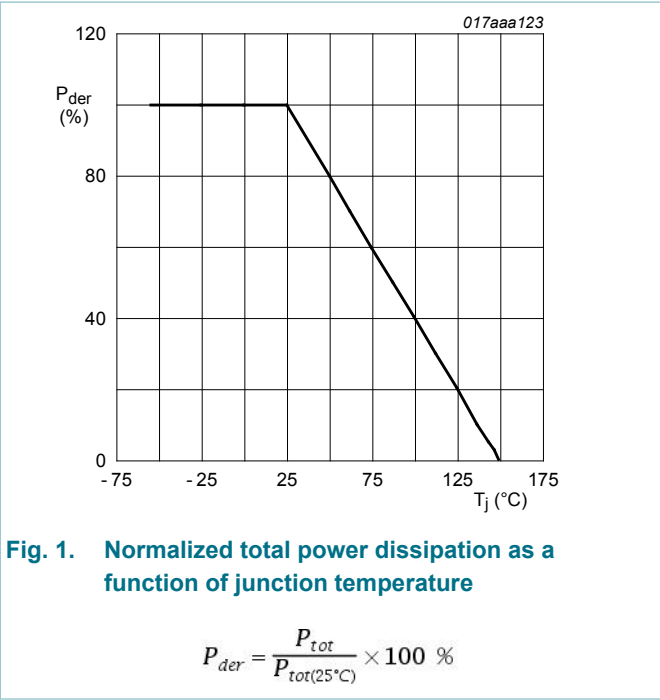
Table 5. Limiting values

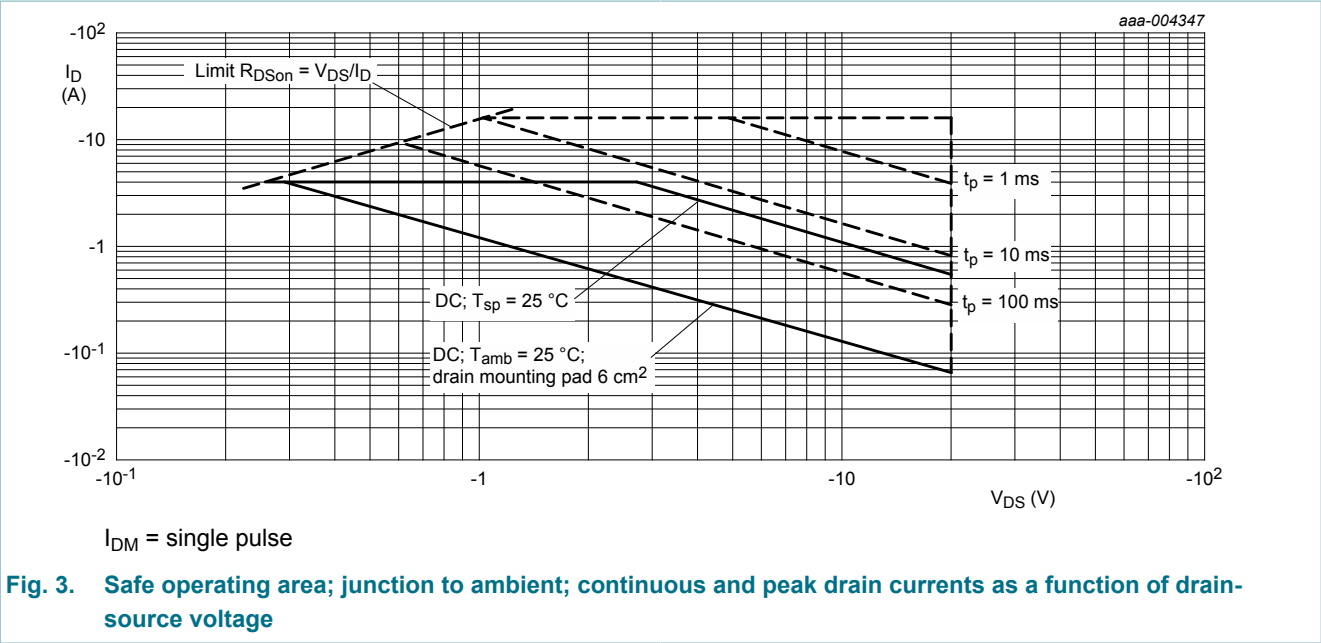
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-20	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-5.7	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-4	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-2.9	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-16	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	500	mW
			[1]	-	1310	mW
		$T_{sp} = 25\text{ °C}$		-	8330	mW

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.4	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	216	250	K/W
			[2]	-	83	95	K/W
		in free air; $t \leq 5\text{ s}$	[2]	-	51	60	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

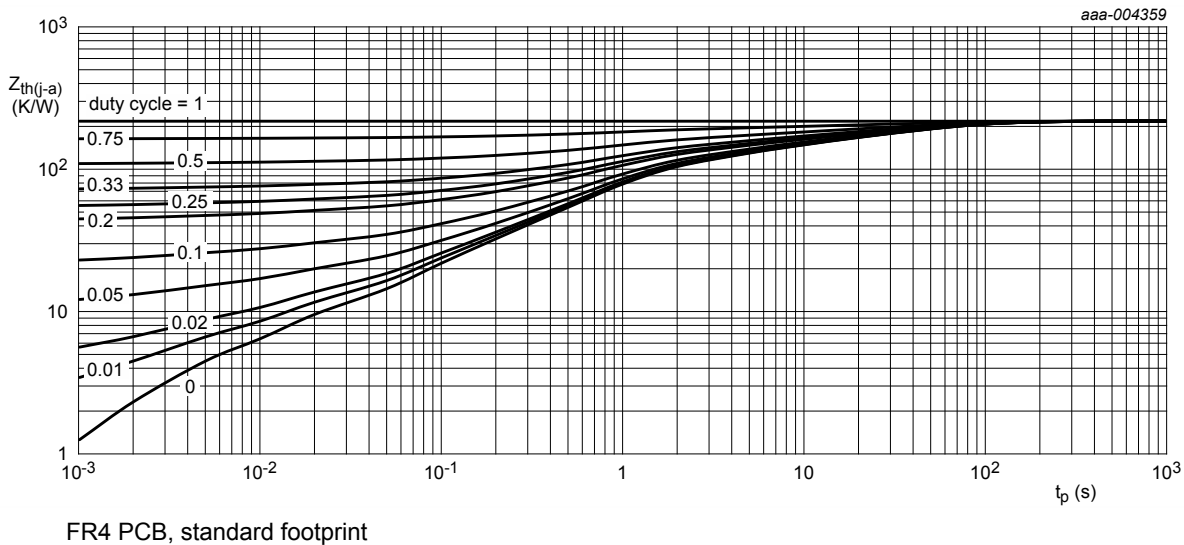


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

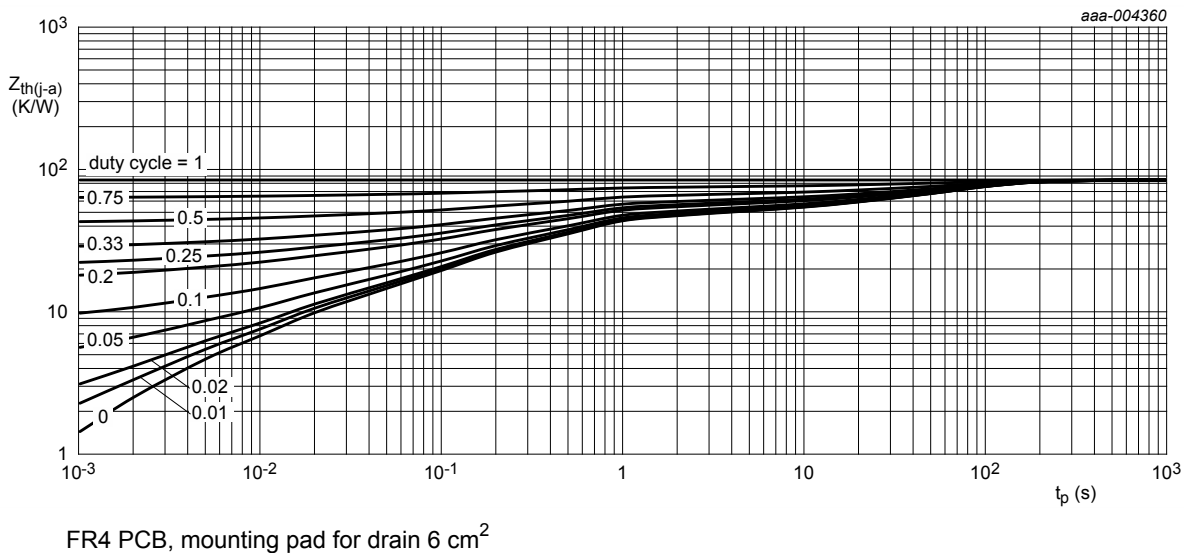


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-0.75	-1	-1.25	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{DS} = -20 V; V _{GS} = 0 V; T _{amb} = 150 °C		-	-	-10	μA
I _{GSS}	gate leakage current	V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -3 A; T _j = 25 °C		-	41	46	mΩ
		V _{GS} = -4.5 V; I _D = -3 A; T _j = 150 °C		-	56	64	mΩ
		V _{GS} = -2.5 V; I _D = -3 A; T _j = 25 °C		-	56	64	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -4 A; T _j = 25 °C		-	12.5	-	S
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -4 A; V _{GS} = -4.5 V; T _j = 25 °C		-	11.5	17.3	nC
Q _{GS}	gate-source charge			-	2.7	-	nC
Q _{GD}	gate-drain charge			-	2.4	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	1410	-	pF
C _{oss}	output capacitance			-	207	-	pF
C _{rss}	reverse transfer capacitance			-	148	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -4 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	17	-	ns
t _r	rise time			-	27	-	ns
t _{d(off)}	turn-off delay time			-	33	-	ns
t _f	fall time			-	27	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -1.2 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V

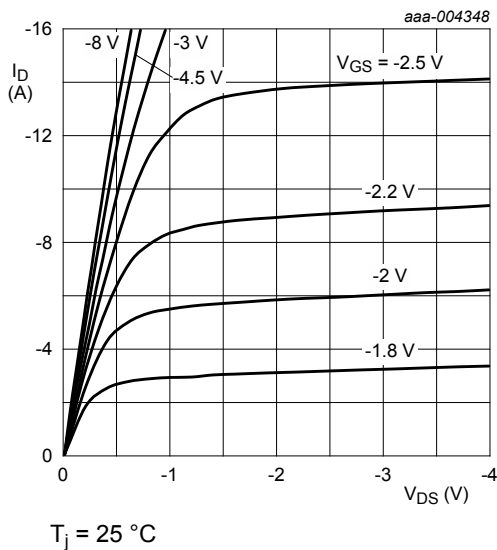


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

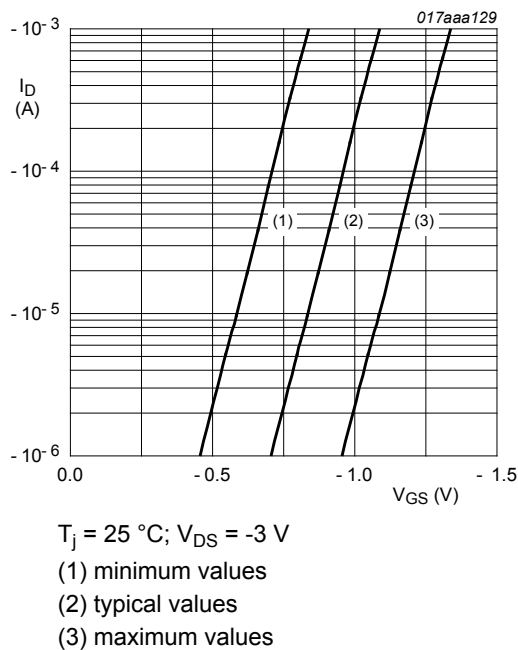


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

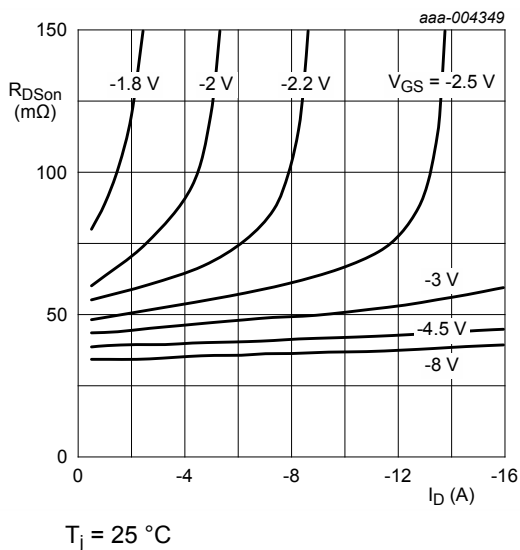


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

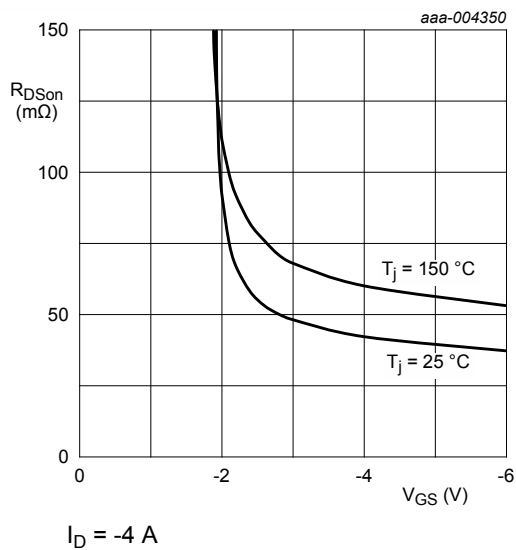


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

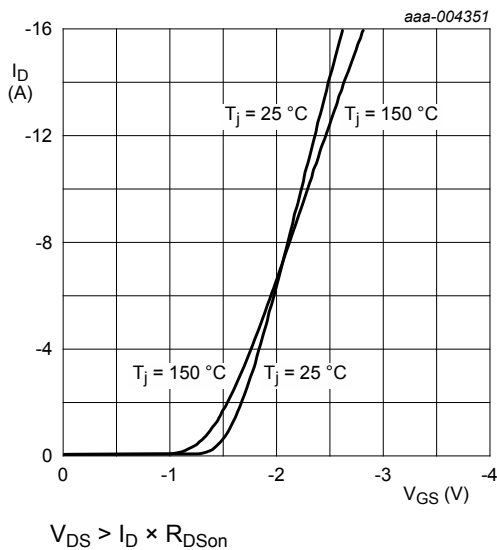


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

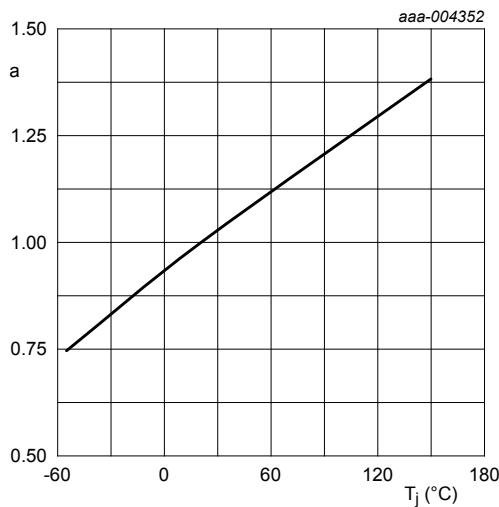


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

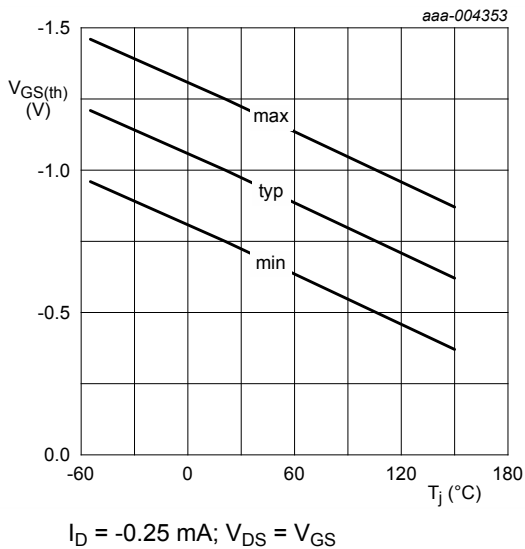


Fig. 12. Gate-source threshold voltage as a function of junction temperature

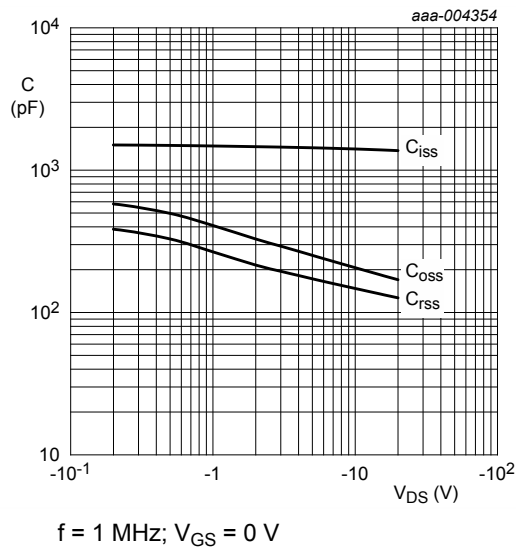


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

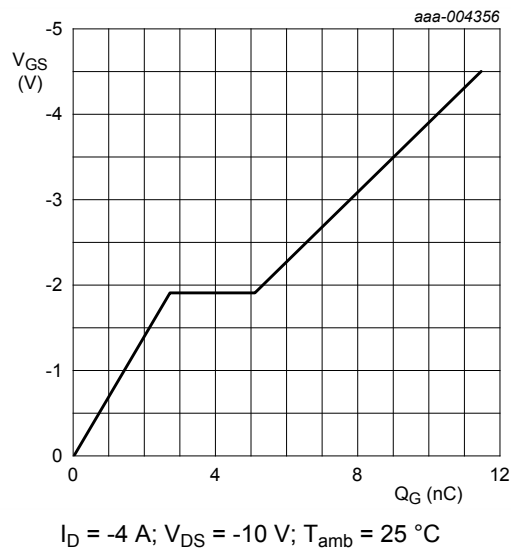


Fig. 14. Gate-source voltage as a function of gate charge; typical values

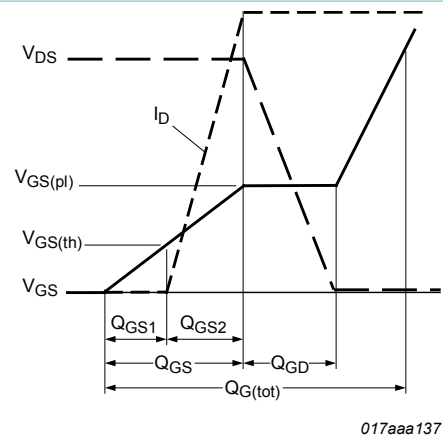
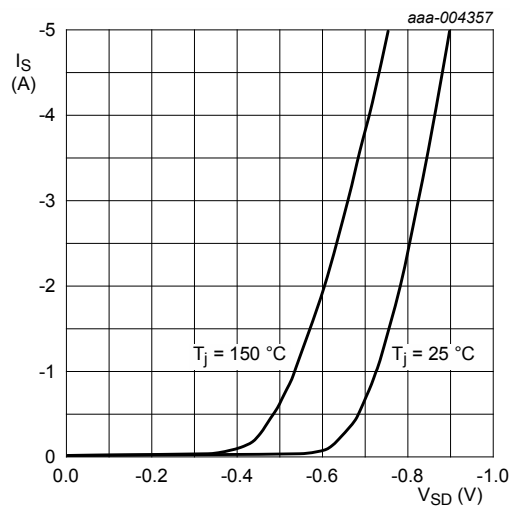


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

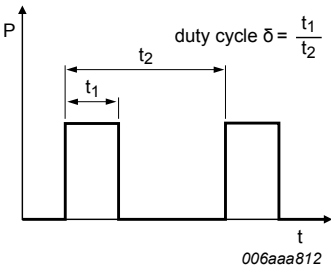


Fig. 17. Duty cycle definition

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

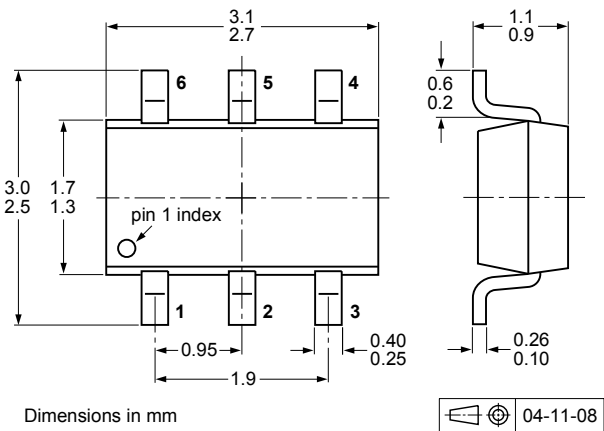


Fig. 18. Package outline TSOP6 (SOT457)

13. Soldering

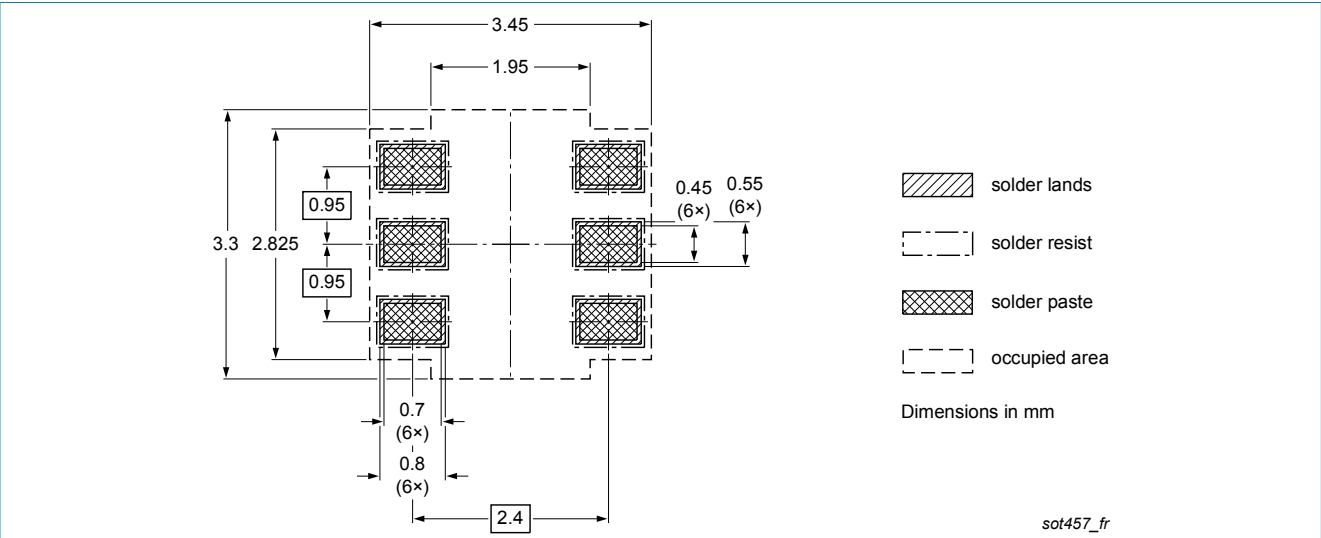


Fig. 19. Reflow soldering footprint for TSOP6 (SOT457)

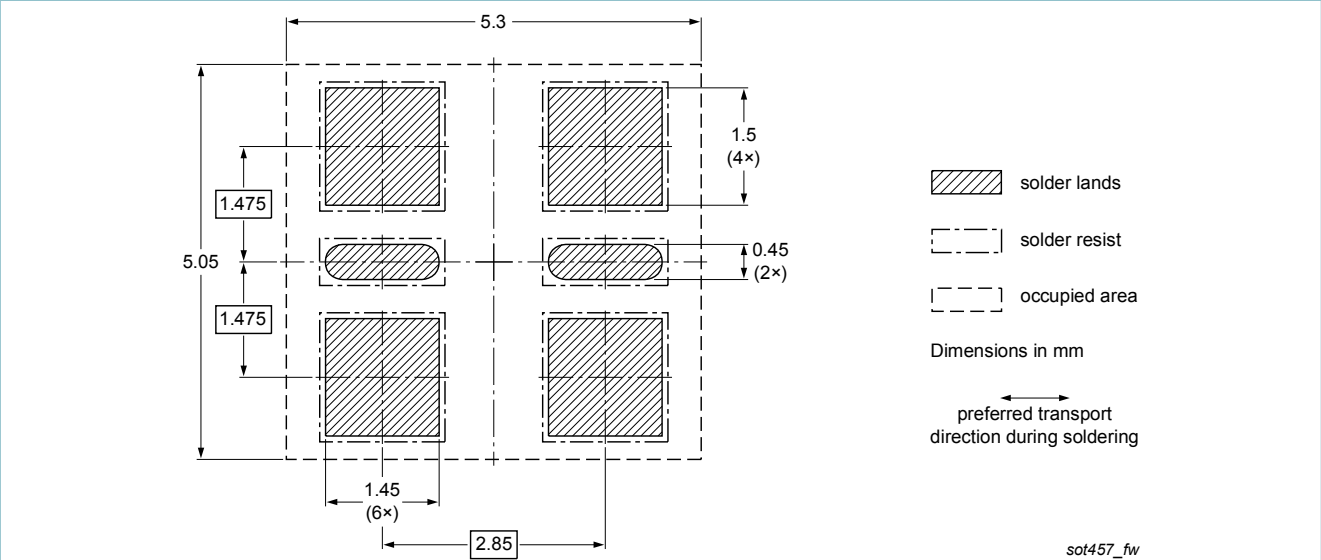


Fig. 20. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN42XPEA v.1	20140321	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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