

Dual General Purpose Transistor

NST3904DXV6T1G, NSVT3904DXV6T1G, NST3904DXV6T5G

The NST/NSV3904DXV6 device is a spin-off of our popular SOT-23/SOT-323 three-lead device. It is designed for general purpose amplifier applications and is housed in the SOT-563 six-lead surface mount package. By putting two discrete devices in one package, this device is ideal for low-power surface mount applications where board space is at a premium.

Features

- h_{FE} , 100–300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- AEC-Q101 Qualified and PPAP Capable – NSVT3904DXV6T1G
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements

MAXIMUM RATINGS

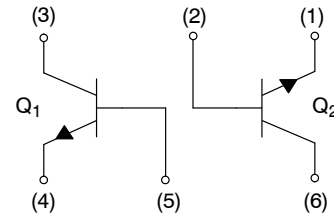
| Rating | Symbol | Value | Unit |
|--------------------------------|-----------|------------------------|------|
| Collector–Emitter Voltage | V_{CEO} | 40 | Vdc |
| Collector–Base Voltage | V_{CBO} | 60 | Vdc |
| Emitter–Base Voltage | V_{EBO} | 6.0 | Vdc |
| Collector Current – Continuous | I_C | 200 | mAdc |
| Electrostatic Discharge | HBM MM | ESD >16000 >2000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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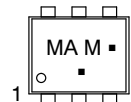


NST/NSV3904DXV6



SOT-563
CASE 463A
STYLE 1

MARKING DIAGRAM



MA = Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|----------------------|------------------|
| NST3904DXV6T1G | SOT-563 (Pb-Free) | 4000/Tape & Reel |
| NSVT3904DXV6T1G | SOT-563 (Pb-Free) | 4000/Tape & Reel |
| NST3904DXV6T5G | SOT-563 (Pb-Free) | 8000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NST3904DXV6T1G, NSVT3904DXV6T1G, NST3904DXV6T5G

THERMAL CHARACTERISTICS

| Characteristic (One Junction Heated) | Symbol | Max | Unit |
|---|-----------------|-------------|----------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 1) | P_D | 357 2.9 | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 350 | $^\circ\text{C}/\text{W}$ |
| Characteristic (Both Junctions Heated) | Symbol | Max | Unit |
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 1) | P_D | 500 4.0 | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 250 | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

1. FR-4 @ Minimum Pad

NST3904DXV6T1G, NSVT3904DXV6T1G, NST3904DXV6T5G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|--|---------------|-----|-----|------|
| OFF CHARACTERISTICS | | | | |
| Collector – Emitter Breakdown Voltage (Note 2) ($I_C = 1.0\text{ mAdc}$, $I_B = 0$) | $V_{(BR)CEO}$ | 40 | – | Vdc |
| Collector – Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{Adc}$, $I_E = 0$) | $V_{(BR)CBO}$ | 60 | – | Vdc |
| Emitter – Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{Adc}$, $I_C = 0$) | $V_{(BR)EBO}$ | 6.0 | – | Vdc |
| Base Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $V_{EB} = 3.0\text{ Vdc}$) | I_{BL} | – | 50 | nAdc |
| Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $V_{EB} = 3.0\text{ Vdc}$) | I_{CEX} | – | 50 | nAdc |

ON CHARACTERISTICS (Note 2)

| | | | | |
|--|---------------|-----------------------------|-------------------------|-----|
| DC Current Gain ($I_C = 0.1\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 10\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 50\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 100\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) | h_{FE} | 40 70 100 60 30 | – – 300 – – | – |
| Collector – Emitter Saturation Voltage ($I_C = 10\text{ mAdc}$, $I_B = 1.0\text{ mAdc}$) ($I_C = 50\text{ mAdc}$, $I_B = 5.0\text{ mAdc}$) | $V_{CE(sat)}$ | – – | 0.2 0.3 | Vdc |
| Base – Emitter Saturation Voltage ($I_C = 10\text{ mAdc}$, $I_B = 1.0\text{ mAdc}$) ($I_C = 50\text{ mAdc}$, $I_B = 5.0\text{ mAdc}$) | $V_{BE(sat)}$ | 0.65 – | 0.85 0.95 | Vdc |

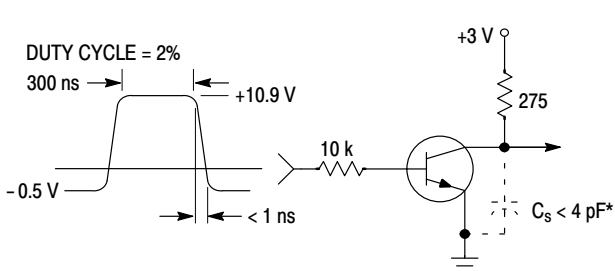
SMALL – SIGNAL CHARACTERISTICS

| | | | | |
|---|-----------|------------|------------|------------------|
| Current – Gain – Bandwidth Product ($I_C = 10\text{ mAdc}$, $V_{CE} = 20\text{ Vdc}$, $f = 100\text{ MHz}$) | f_T | 300 | – | MHz |
| Output Capacitance ($V_{CB} = 5.0\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$) | C_{obo} | – | 4.0 | pF |
| Input Capacitance ($V_{EB} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 1.0\text{ MHz}$) | C_{ibo} | – | 8.0 | pF |
| Input Impedance ($V_{CE} = 10\text{ Vdc}$, $I_C = 1.0\text{ mAdc}$, $f = 1.0\text{ kHz}$) | h_{ie} | 1.0 2.0 | 10 12 | k Ω |
| Voltage Feedback Ratio ($V_{CE} = 10\text{ Vdc}$, $I_C = 1.0\text{ mAdc}$, $f = 1.0\text{ kHz}$) | h_{re} | 0.5 0.1 | 8.0 10 | $\times 10^{-4}$ |
| Small – Signal Current Gain ($V_{CE} = 10\text{ Vdc}$, $I_C = 1.0\text{ mAdc}$, $f = 1.0\text{ kHz}$) | h_{fe} | 100 100 | 400 400 | – |
| Output Admittance ($V_{CE} = 10\text{ Vdc}$, $I_C = 1.0\text{ mAdc}$, $f = 1.0\text{ kHz}$) | h_{oe} | 1.0 3.0 | 40 60 | μmhos |
| Noise Figure ($V_{CE} = 5.0\text{ Vdc}$, $I_C = 100\text{ }\mu\text{Adc}$, $R_S = 1.0\text{ k}\Omega$, $f = 1.0\text{ kHz}$) | NF | – – | 5.0 4.0 | dB |

SWITCHING CHARACTERISTICS

| | | | | | |
|--------------|--|-------|---|-----|----|
| Delay Time | ($V_{CC} = 3.0\text{ Vdc}$, $V_{BE} = -0.5\text{ Vdc}$) | t_d | – | 35 | ns |
| Rise Time | ($I_C = 10\text{ mAdc}$, $I_{B1} = 1.0\text{ mAdc}$) | t_r | – | 35 | |
| Storage Time | ($V_{CC} = 3.0\text{ Vdc}$, $I_C = 10\text{ mAdc}$) | t_s | – | 200 | ns |
| Fall Time | ($I_{B1} = I_{B2} = 1.0\text{ mAdc}$) | t_f | – | 50 | |

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2.0\%$.



* Total shunt capacitance of test jig and connectors

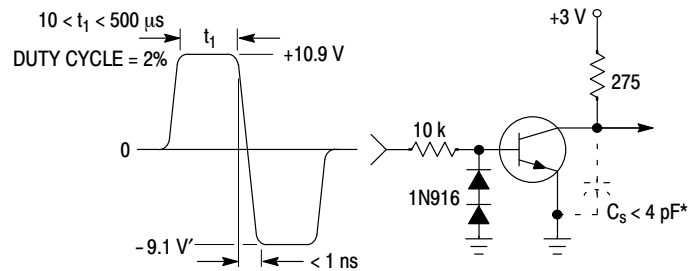


Figure 1. Delay and Rise Time Equivalent Test Circuit

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

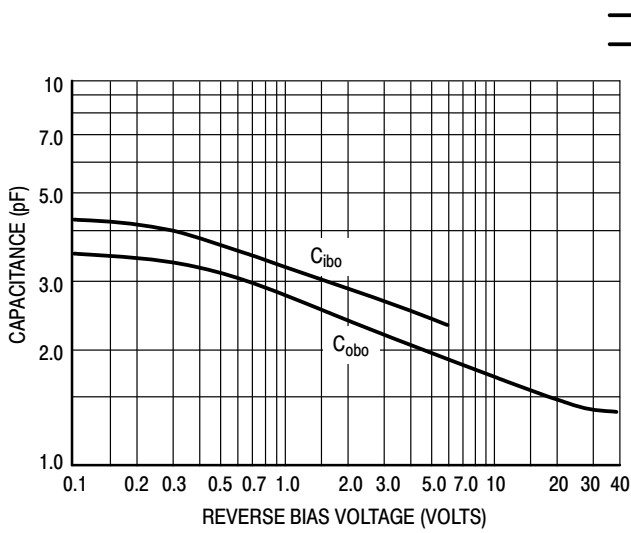


Figure 3. Capacitance

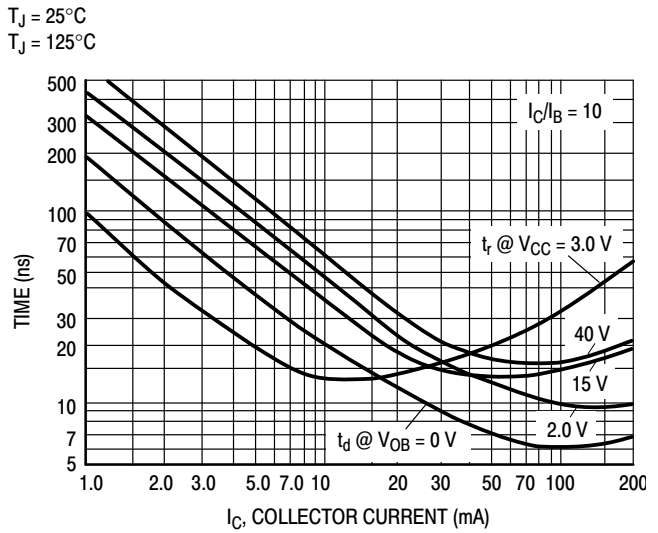


Figure 4. Turn-On Time

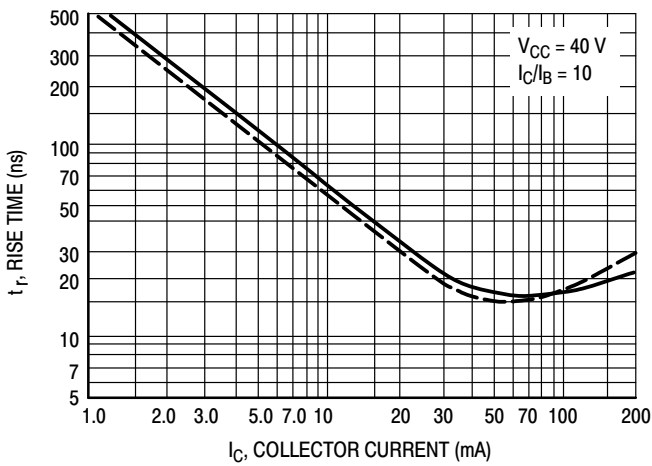


Figure 5. Rise Time

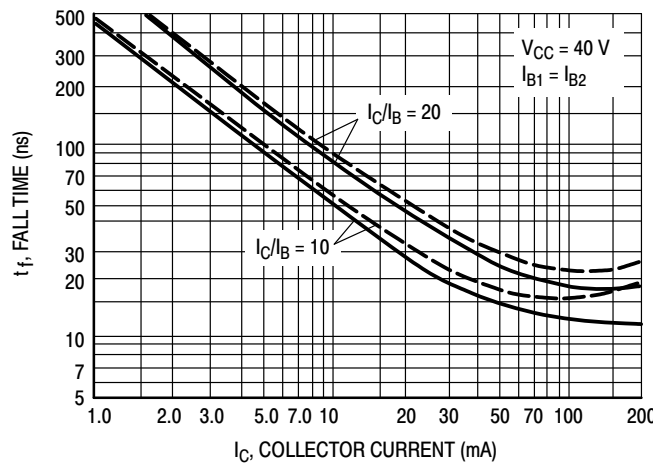


Figure 6. Fall Time

TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS

($V_{CE} = 5.0$ Vdc, $T_A = 25^\circ\text{C}$, Bandwidth = 1.0 Hz)

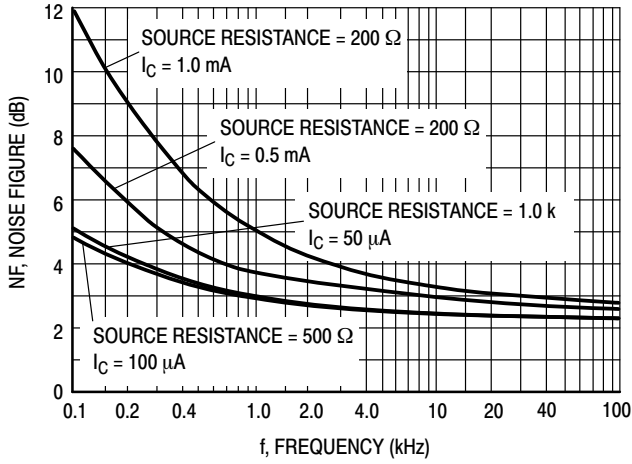


Figure 7. Noise Figure

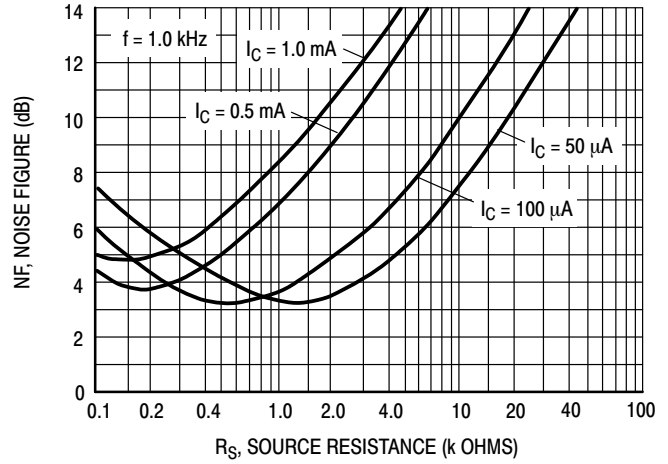


Figure 8. Noise Figure

h PARAMETERS

($V_{CE} = 10$ Vdc, $f = 1.0$ kHz, $T_A = 25^\circ\text{C}$)

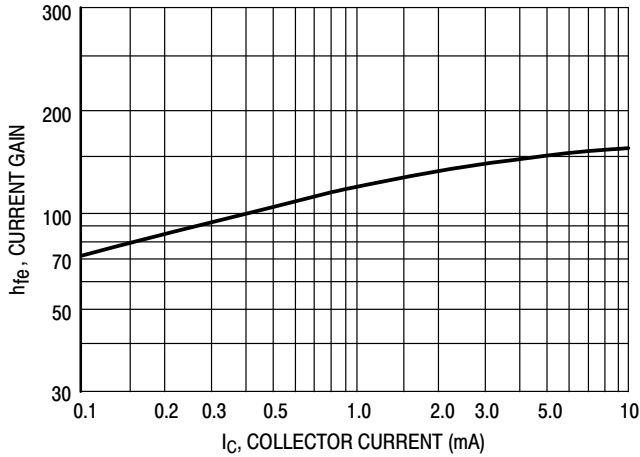


Figure 9. Current Gain

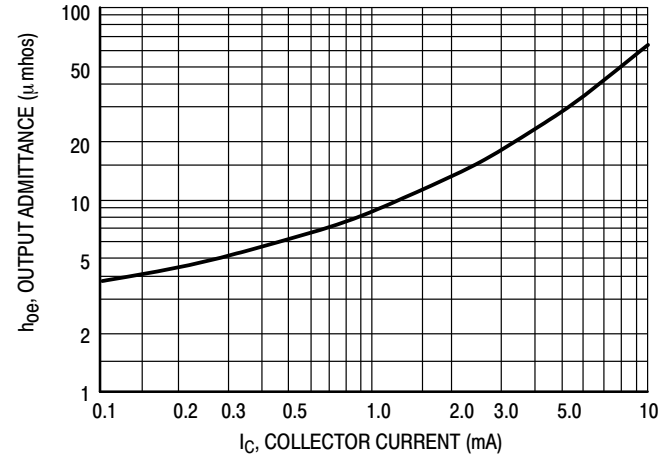


Figure 10. Output Admittance

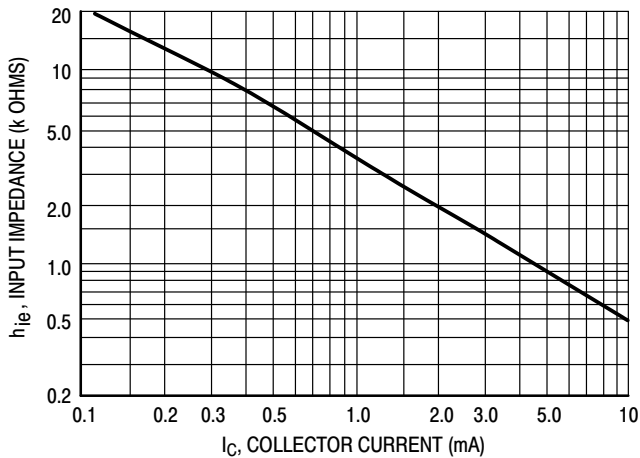


Figure 11. Input Impedance

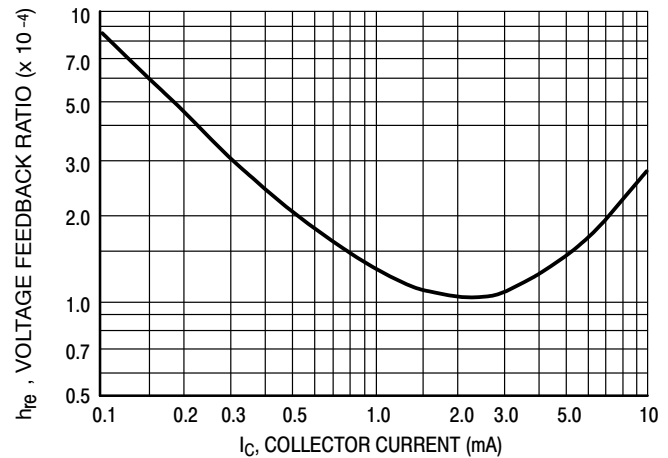


Figure 12. Voltage Feedback Ratio

TYPICAL STATIC CHARACTERISTICS

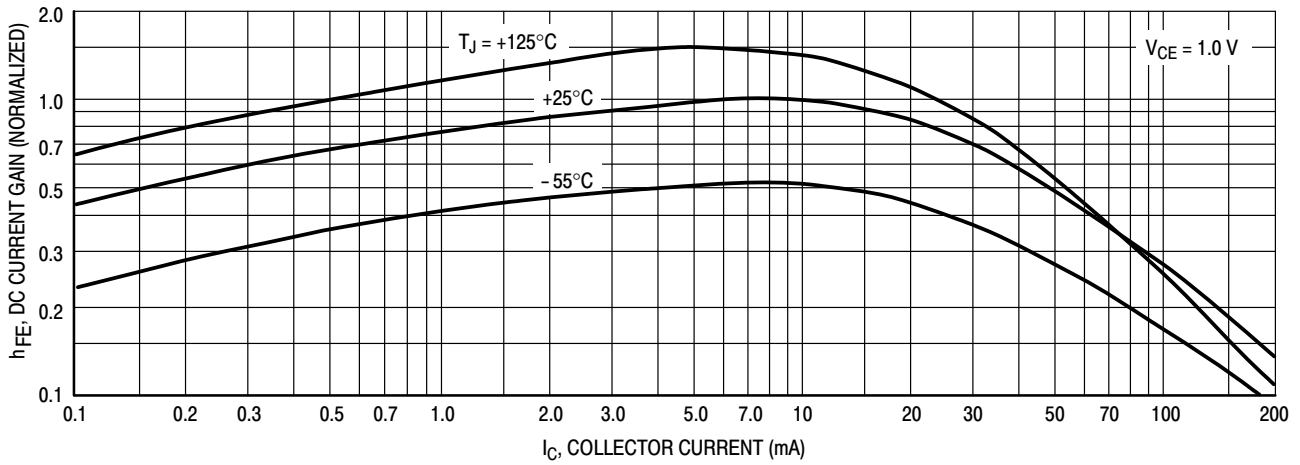


Figure 13. DC Current Gain

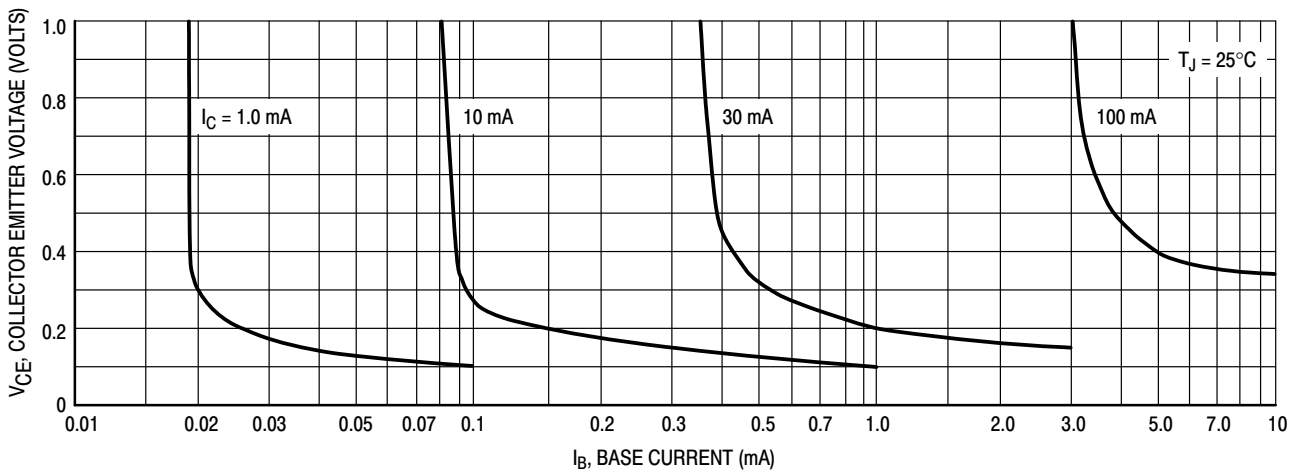


Figure 14. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

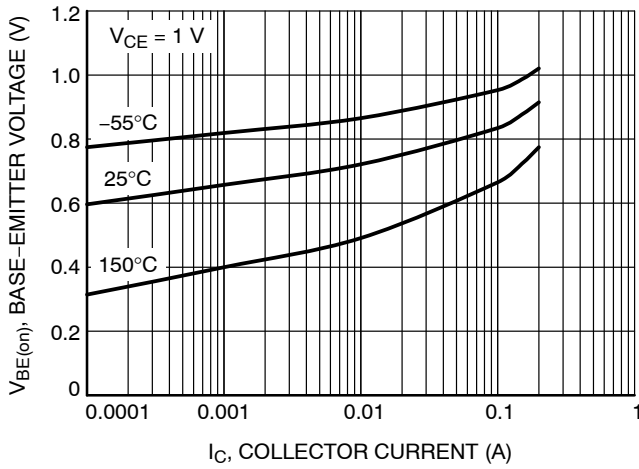


Figure 15. Base Emitter Voltage vs. Collector Current

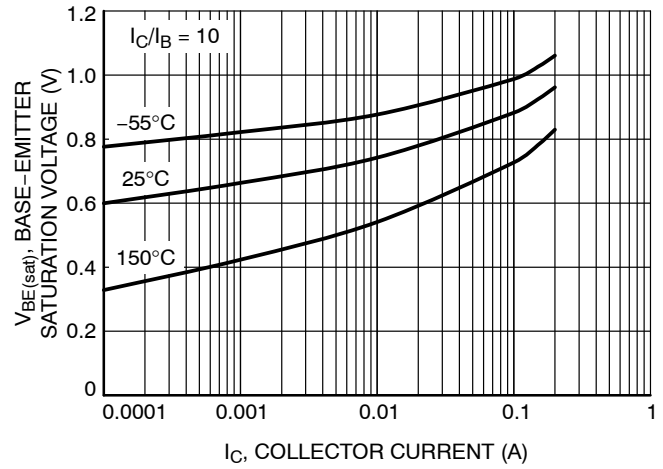


Figure 16. Base Emitter Saturation Voltage vs. Collector Current

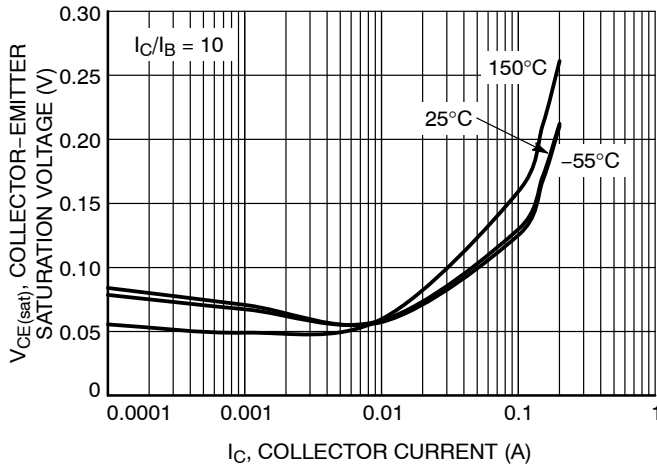


Figure 17. Collector Emitter Saturation Voltage vs. Collector Current

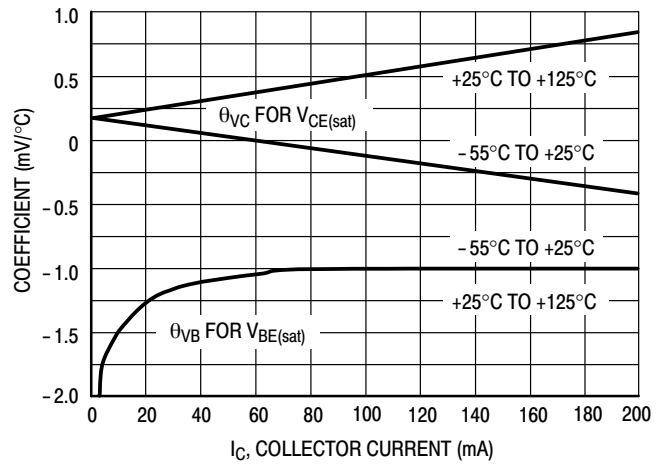


Figure 18. Temperature Coefficients

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 4:1

SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



| DIM | MILLIMETERS | | |
|----------------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.50 | 1.60 | 1.70 |
| E | 1.10 | 1.20 | 1.30 |
| e | 0.50 BSC | | |
| L | 0.10 | 0.20 | 0.30 |
| H _E | 1.50 | 1.60 | 1.70 |

RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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SOT-563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Month Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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