

# NTD12N10

## Power MOSFET 12 Amps, 100 Volts

### N-Channel Enhancement-Mode DPAK



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#### Features

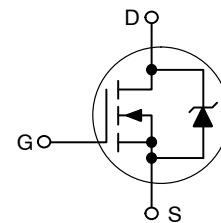
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Avalanche Energy Specified
- $I_{DSS}$  and  $R_{DS(on)}$  Specified at Elevated Temperature
- Mounting Information Provided for the DPAK Package
- These are Pb-Free Devices

#### Typical Applications

- PWM Motor Controls
- Power Supplies
- Converters

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
100 V	165 mΩ @ 10 V	12 A

#### N-Channel



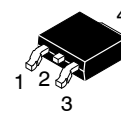
#### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	100	Vdc
Drain-to-Source Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	100	Vdc
Gate-to-Source Voltage – Continuous – Non-Repetitive ( $t_p \leq 10 \text{ ms}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 30$	Vdc Vpk
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Continuous @ $T_A = 100^\circ\text{C}$ – Pulsed (Note 3)	$I_D$ $I_{D1}$ $I_{DM}$	12 7.0 36	Adc A Apk
Total Power Dissipation Derate above $25^\circ\text{C}$ Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)	$P_D$	56.6 0.38 1.76 1.28	W W/ $^\circ\text{C}$ W W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 12 \text{ Apk}$ , $L = 1.0 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	75	mJ
Thermal Resistance – Junction to Case – Junction to Ambient (Note 1) – Junction to Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.65 85 117	$^\circ\text{C/W}$
Maximum Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

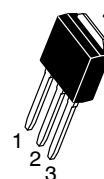
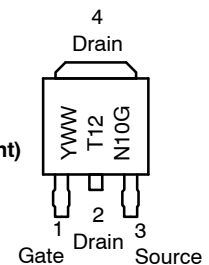
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.
3. Pulse Test: Pulse Width = 10  $\mu\text{s}$ , Duty Cycle = 2%.

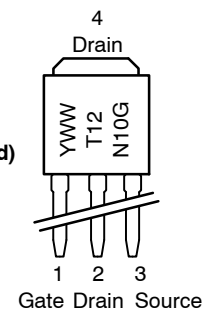
#### MARKING DIAGRAMS & PIN ASSIGNMENTS



DPAK  
CASE 369C  
(Surface Mount)  
STYLE 2



DPAK  
CASE 369D  
(Straight Lead)  
STYLE 2



Y = Year  
WW = Work Week  
T12N10 = Device Code  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# NTD12N10

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	100 -	- 135	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 100 Vdc, T <sub>J</sub> = 25°C) (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 100 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	- -	- -	5.0 50	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	-	-	±100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 -	3.1 -7.5	4.0 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 6.0 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 6.0 Adc, T <sub>J</sub> = 125°C)	R <sub>DS(on)</sub>	- -	0.130 0.250	0.165 0.400	Ω
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 12 Adc)	V <sub>DS(on)</sub>	-	1.62	2.16	Vdc
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 6.0 Adc)	g <sub>FS</sub>	-	7.0	-	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ISS</sub>	-	390	550	pF
Output Capacitance		C <sub>OSS</sub>	-	115	160	
Reverse Transfer Capacitance		C <sub>RSS</sub>	-	35	70	

### SWITCHING CHARACTERISTICS (Notes 4 & 5)

Turn-On Delay Time	(V <sub>DD</sub> = 80 Vdc, I <sub>D</sub> = 12 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	-	11	20	ns
Rise Time		t <sub>r</sub>	-	30	60	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	22	40	
Fall Time		t <sub>f</sub>	-	32	60	
Total Gate Charge	(V <sub>DS</sub> = 80 Vdc, I <sub>D</sub> = 12 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>tot</sub>	-	14	20	nC
Gate-to-Source Charge		Q <sub>gs</sub>	-	3.0	-	
Gate-to-Drain Charge		Q <sub>gd</sub>	-	7.0	-	

### BODY-DRAIN DIODE RATINGS (Note 4)

Diode Forward On-Voltage	(I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	0.95 0.80	1.0 -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	85	-	ns
		t <sub>a</sub>	-	60	-	
		t <sub>b</sub>	-	28	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.3	-	μC

4. Indicates Pulse Test: P.W. = 300 μs max, Duty Cycle = 2%.

5. Switching characteristics are independent of operating junction temperature.

### ORDERING INFORMATION

Device	Package	Shipping†
NTD12N10G	DPAK (Pb-Free)	75 Units/Rail
NTD12N10-1G	DPAK-3 (Pb-Free)	75 Units/Rail
NTD12N10T4G	DPAK (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD12N10

## TYPICAL ELECTRICAL CHARACTERISTICS

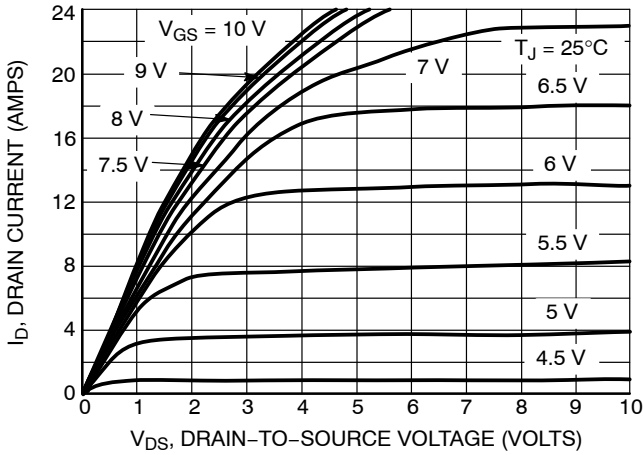


Figure 1. On-Region Characteristics

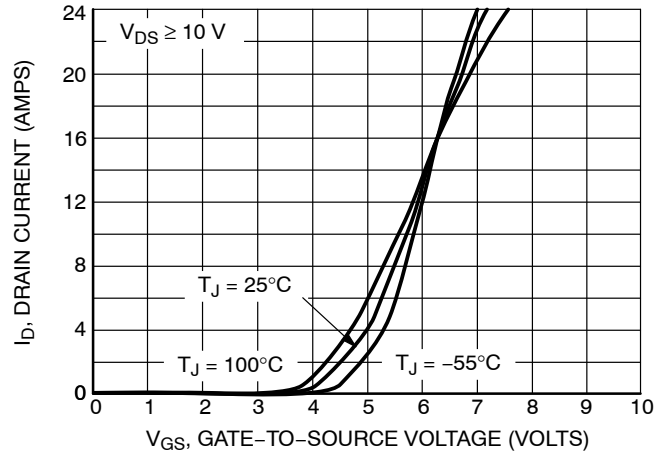


Figure 2. Transfer Characteristics

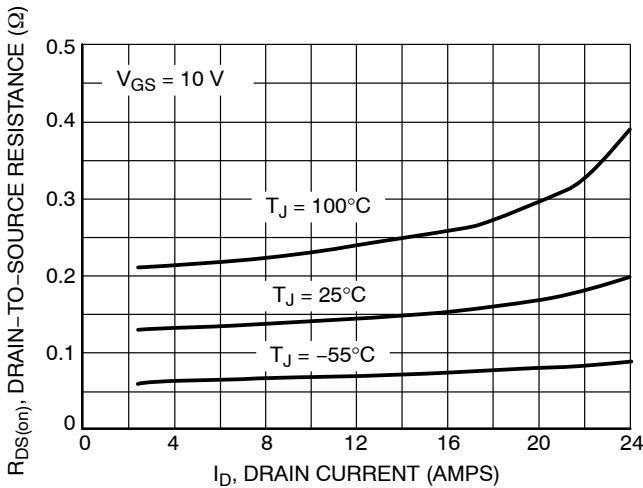


Figure 3. On-Resistance versus Drain Current and Temperature

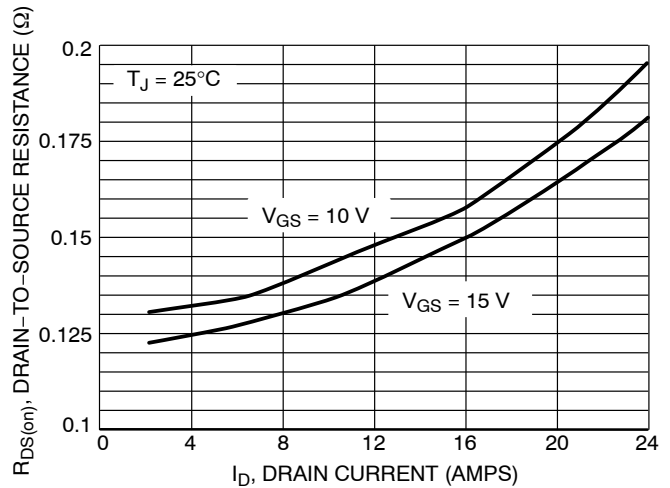


Figure 4. On-Resistance versus Drain Current and Gate Voltage

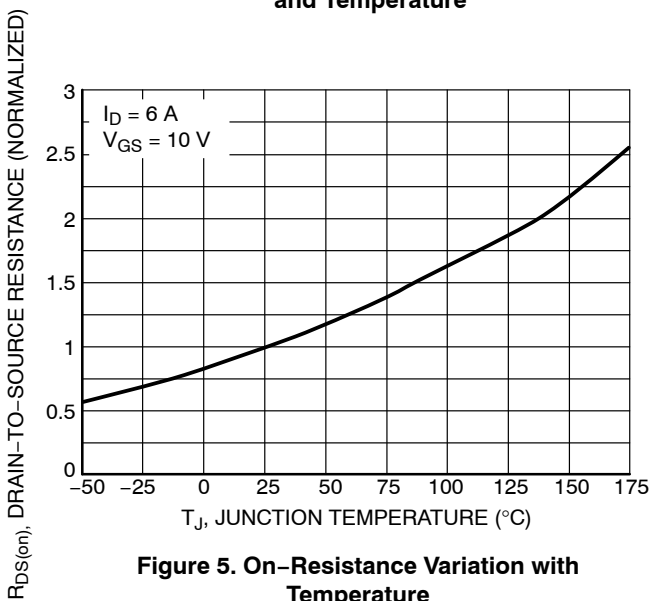


Figure 5. On-Resistance Variation with Temperature

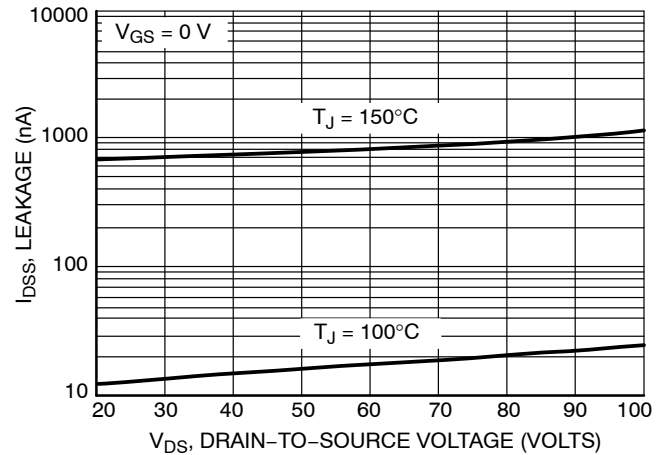


Figure 6. Drain-to-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{SGP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{SGP})$$

$$t_f = Q_2 \times R_G / V_{SGP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{SGP}$  are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{SGP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{SGP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on-state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

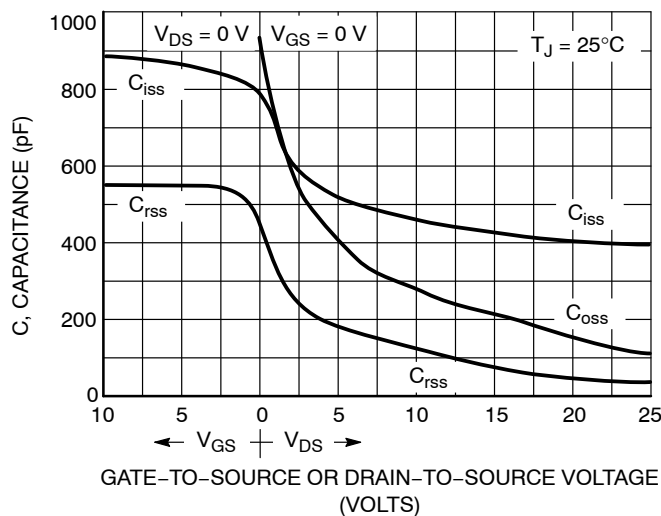
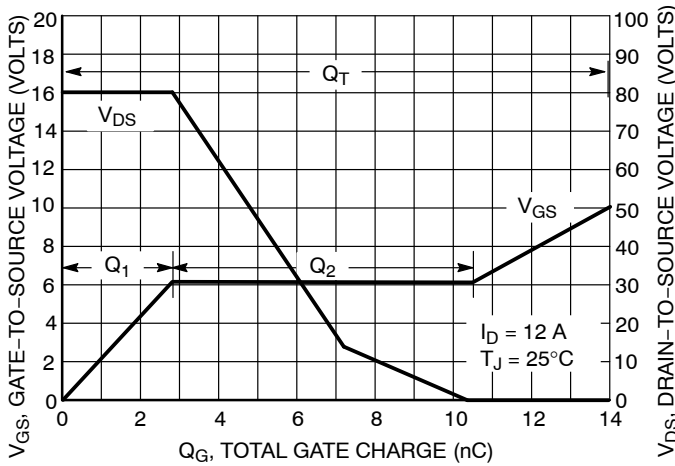
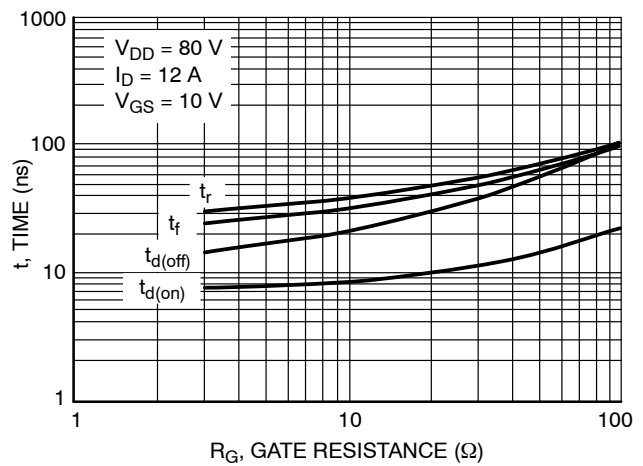


Figure 7. Capacitance Variation

# NTD12N10

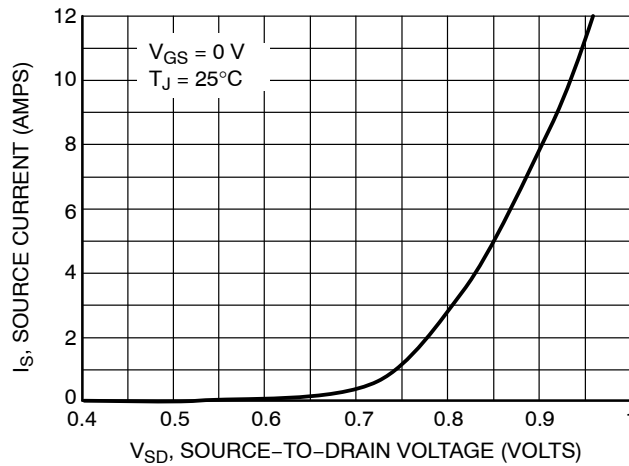


**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance—General Data and Its Use.”

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded and the transition time ( $t_r, t_f$ ) do not exceed 10  $\mu s$ . In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

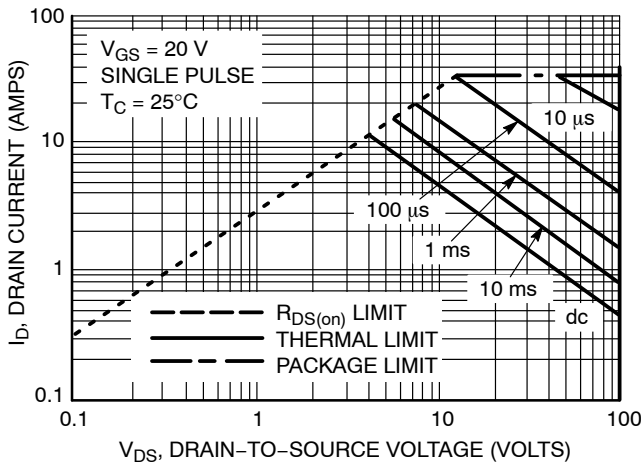
A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

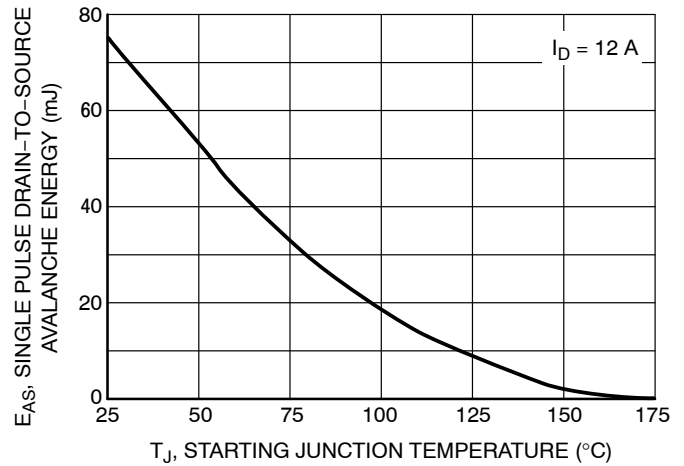
Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

# NTD12N10

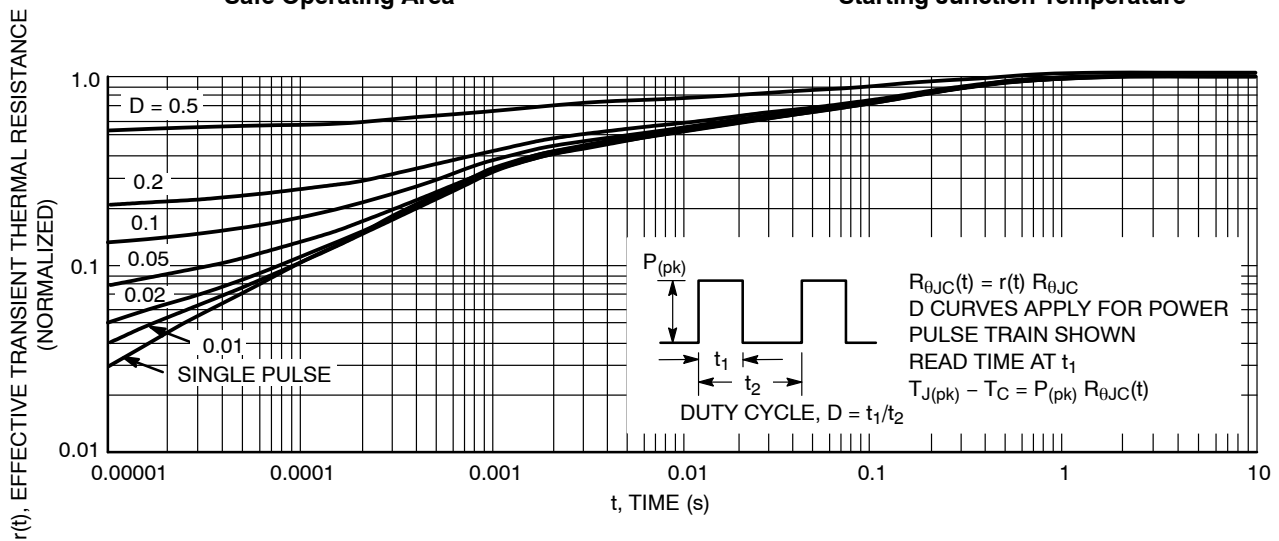
## SAFE OPERATING AREA



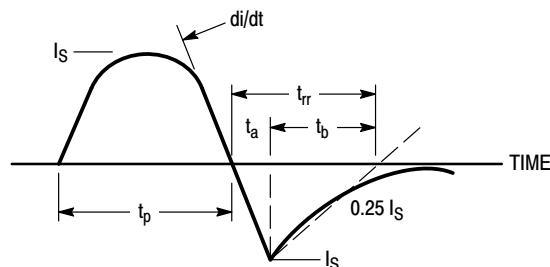
**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**



**Figure 13. Thermal Response**

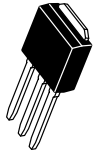


**Figure 14. Diode Reverse Recovery Waveform**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

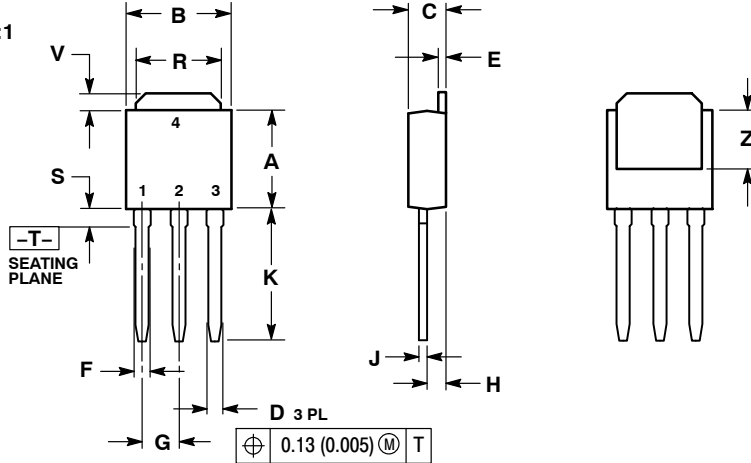
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### MARKING DIAGRAMS



- xxxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

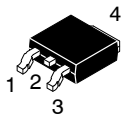
DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

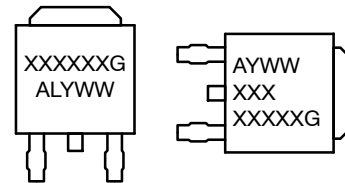


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*



IC

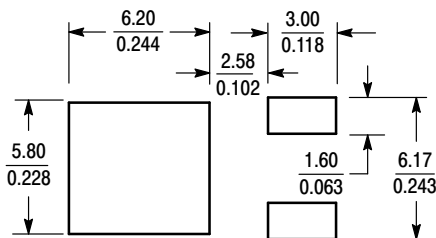
Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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