MOSFET – Power, Single N-Channel
40 V, 0.72 mΩ, 368 A

NTMJS0D8N04CL

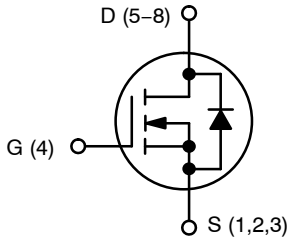
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Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK8 Package, Industry Standard
- These Devices are Pb−Free and are RoHS Compliant

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.72 mΩ @ 10 V	368 A
	1.15 mΩ @ 4.5 V	



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	368	A
		T_C = 100°C		260	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	180	W
		T_C = 100°C		90	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	56	A
		T_A = 100°C		40	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	4.2	W
		T_A = 100°C		2.1	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	150	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 32.8 A)			E_{AS}	1286	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

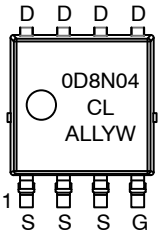
Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	0.83	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	35.9	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



LFPAK8
CASE 760AA

MARKING DIAGRAM



0D8N04CL = Specific Device Code
A = Assembly Location
LL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				18		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		0.60	0.72	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		0.91	1.15	
Forward Transconductance	g_{FS}	V_{DS} =15 V, I_D = 50 A			500		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			9600		pF
Output Capacitance	C_{OSS}				4690		
Reverse Transfer Capacitance	C_{RSS}				119		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 32 V; I_D = 50 A			78		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V; I_D = 50 A			162		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 32 V; I_D = 50 A			14		
Gate−to−Source Charge	Q_{GS}				25		
Gate−to−Drain Charge	Q_{GD}				29		
Plateau Voltage	V_{GP}				2.7		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 32 V, I_D = 50 A, R_G = 2.5 Ω			36		ns
Rise Time	t_r				50		
Turn−Off Delay Time	$t_{d(OFF)}$				81		
Fall Time	t_f				37		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.73	1.2	V
			T_J = 125°C		0.6		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 50 A			83		ns
Charge Time	t_a				53		
Discharge Time	t_b				30		
Reverse Recovery Charge	Q_{RR}				163		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

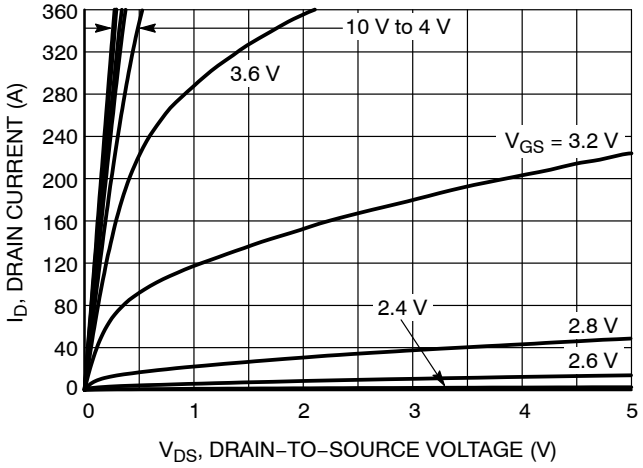


Figure 1. On−Region Characteristics

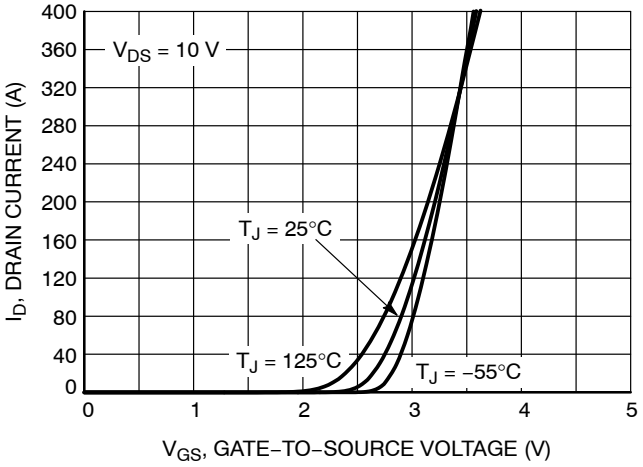


Figure 2. Transfer Characteristics

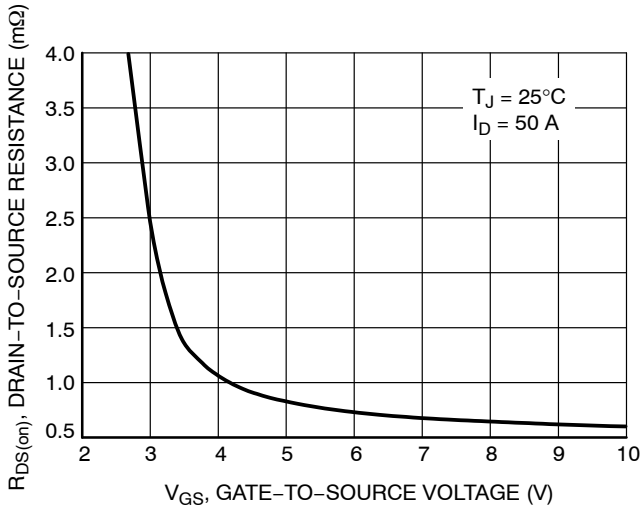


Figure 3. On−Resistance vs. Gate−to−Source Voltage

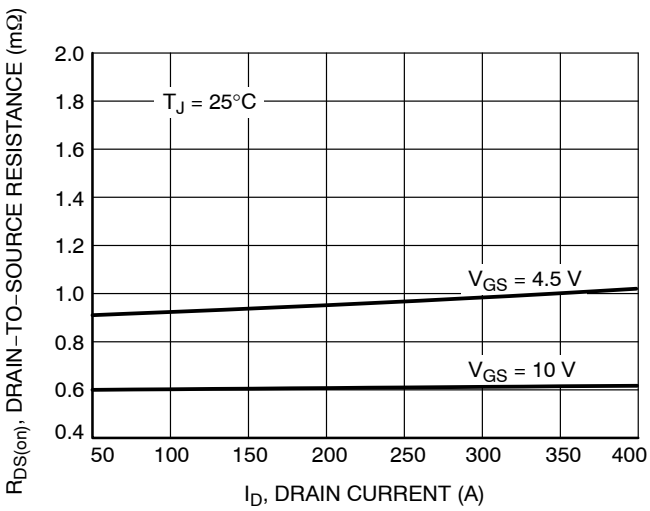


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

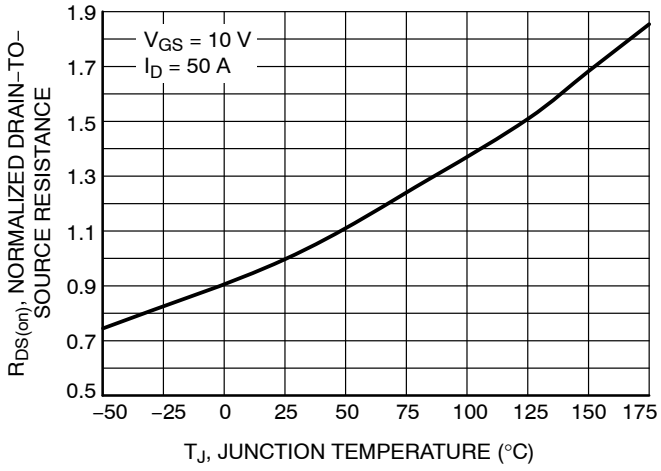


Figure 5. On−Resistance Variation with Temperature

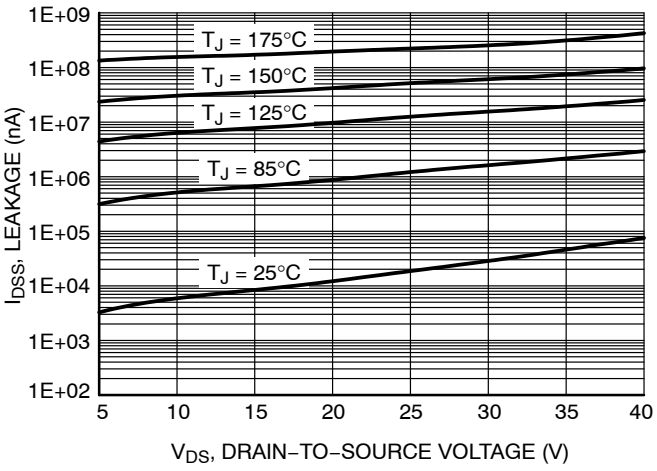


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

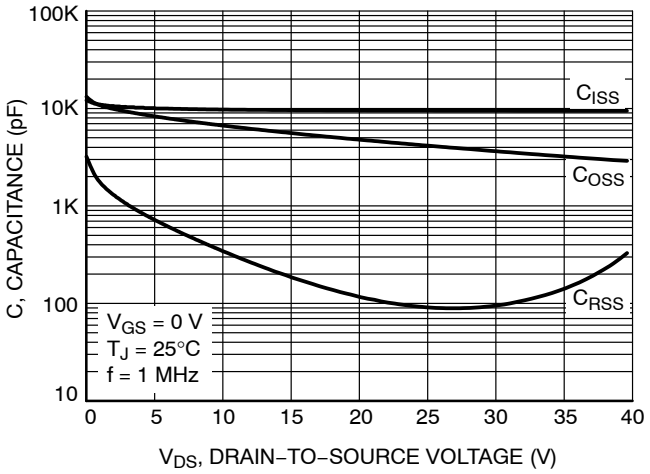


Figure 7. Capacitance Variation

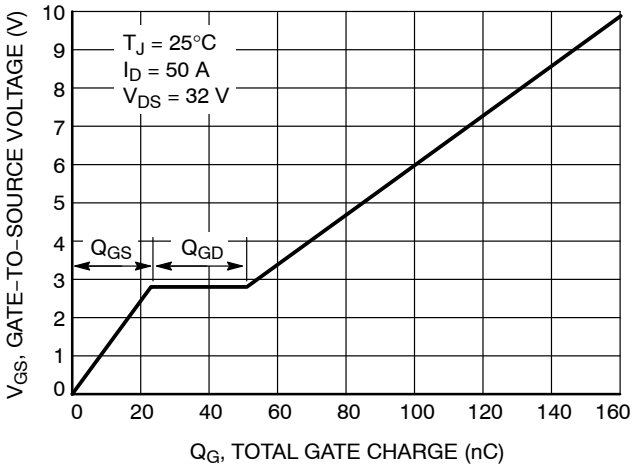


Figure 8. Gate−to−Source Voltage vs. Total Charge

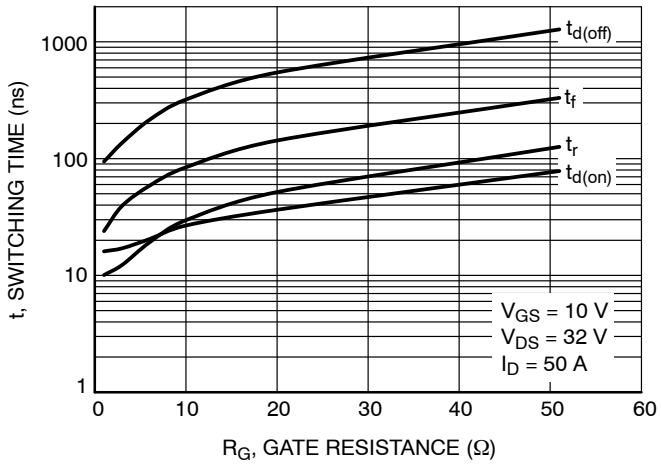


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

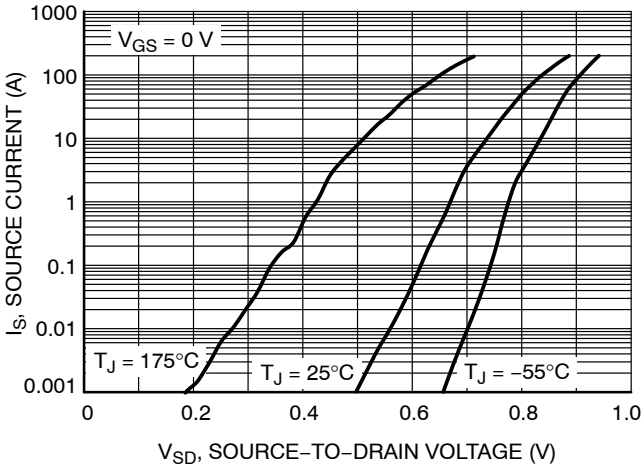


Figure 10. Diode Forward Voltage vs. Current

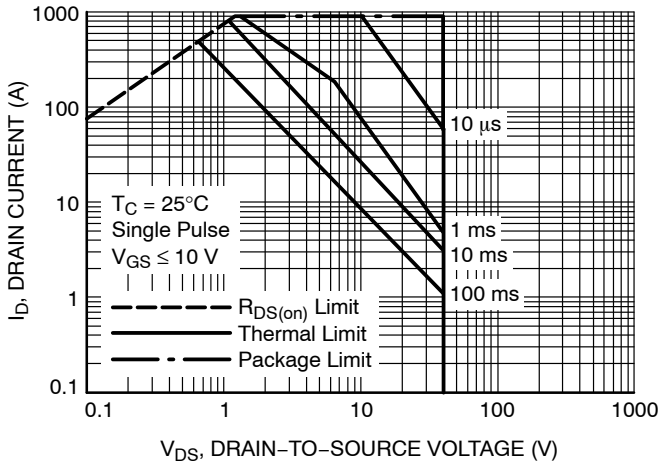


Figure 11. Maximum Rated Forward Biased Safe Operating Area

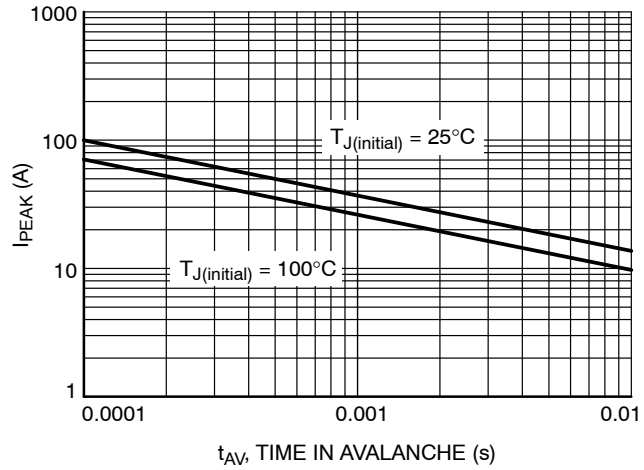


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

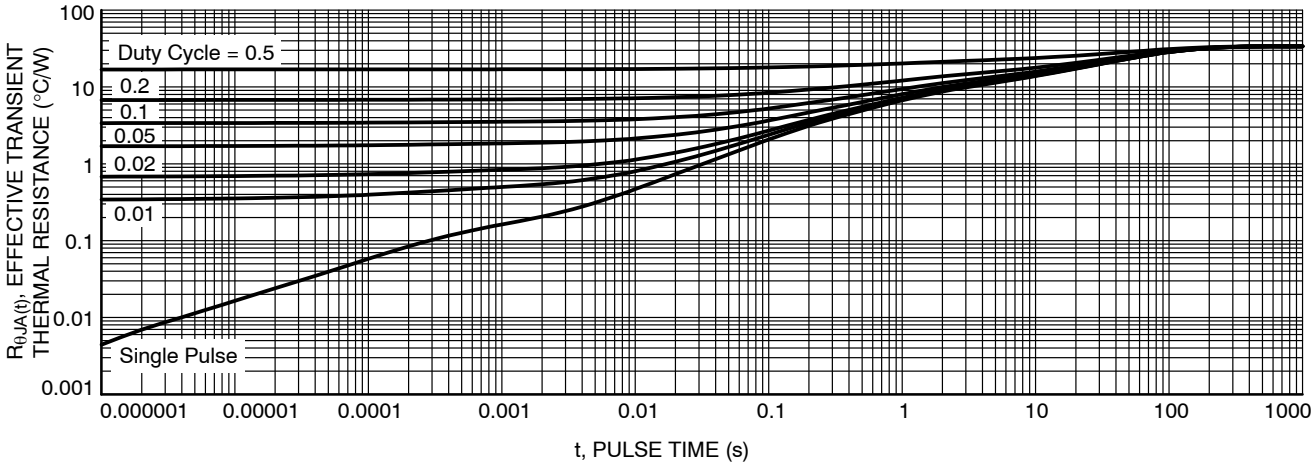


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMJS0D8N04CLTWG	0D8N04CL	LFPAK8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

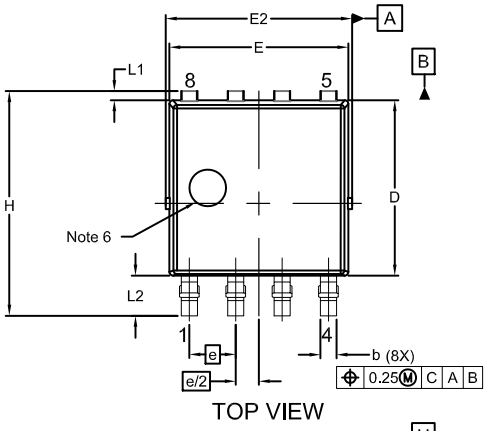
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

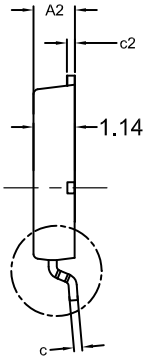


LFPAK8 5x6
CASE 760AA
ISSUE C

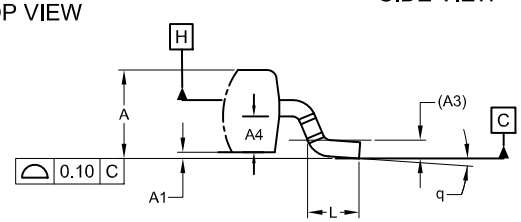
DATE 13 AUG 2019



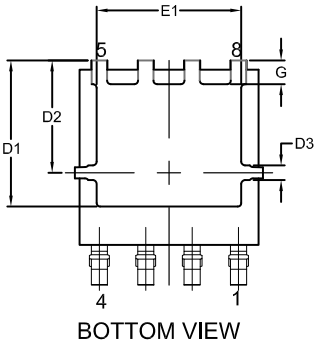
TOP VIEW



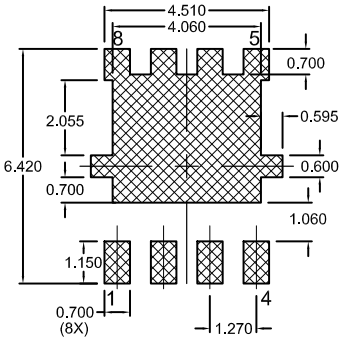
SIDE VIEW



DETAIL 'A'



BOTTOM VIEW



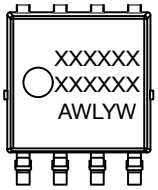
RECOMMENDED LAND PAD

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3		0.25 REF	
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
E	4.80	4.90	5.00
E1	3.90	4.00	4.10
E2	5.00	5.15	5.30
e		1.27 BSC	
G	0.55	0.65	0.75
H	6.00	6.15	6.30
L	0.45	0.65	0.85
L1	0.15	0.25	0.35
L2	0.90	1.10	1.30
q	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

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DESCRIPTION:	**LFPAK8 5x6**	**PAGE 1 OF 1**

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