

NTTFS4C02N

MOSFET – Power, Single, N-Channel, μ 8FL 30 V, 170 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	29	A
		$T_A = 85^\circ\text{C}$	21	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	2.7	W	
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	I_D	$T_A = 25^\circ\text{C}$	36	A
		$T_A = 85^\circ\text{C}$	26	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	P_D	4.2	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	16	A
		$T_A = 85^\circ\text{C}$	12	
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	0.83	W	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	170	A
		$T_C = 85^\circ\text{C}$	120	
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	91	W	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	500	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	100	A	
Drain to Source dV/dt	dV/dt	6.0	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 37 A_{pk}$) (Note 3)	E_{AS}	162	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

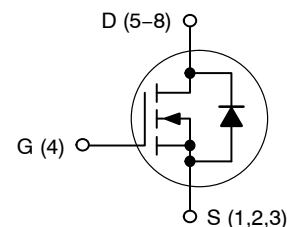


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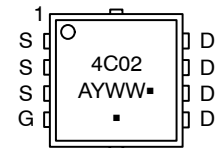
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	2.25 m Ω @ 10 V	170 A
	3.1 m Ω @ 4.5 V	

N-Channel MOSFET



MARKING DIAGRAM



4C02 = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS4C02NTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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- Surface-mounted on FR4 board using the minimum recommended pad size.
- This is the absolute maximum ratings. Parts are 100% tested at $T_J = 25^\circ\text{C}$, $V_{GS} = 10\text{ V}$, $I_L = 36\text{ A}$, $E_{AS} = 65\text{ mJ}$.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.4	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	46	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	150	
Junction-to-Ambient – ($t \leq 10\text{ s}$) (Note 4)	$R_{\theta JA}$	30	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			13.8		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1.3	1.6	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	1.9	2.25	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$	2.7	3.1	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}$, $I_D = 50\text{ A}$		140		S
Gate Resistance	R_G			0.9		Ω

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$, $V_{DS} = 15\text{ V}$		2980		pF
Output Capacitance	C_{OSS}			1200		
Reverse Transfer Capacitance	C_{RSS}			55		
Output Charge	Q_{OSS}	$V_{GS} = 0\text{ V}$, $V_{DD} = 15\text{ V}$		25		nC
Capacitance Ratio	C_{RSS}/C_{ISS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 15\text{ V}$, $f = 1\text{ MHz}$		0.018		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}$, $V_{DS} = 15\text{ V}$; $I_D = 50\text{ A}$		20		nC
Threshold Gate Charge	$Q_{G(TH)}$			4.7		
Gate-to-Source Charge	Q_{GS}			8.5		
Gate-to-Drain Charge	Q_{GD}			4		
Gate Plateau Voltage	V_{GP}			2.8		V
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 15\text{ V}$; $I_D = 50\text{ A}$		45		nC

SWITCHING CHARACTERISTICS (Note 7)

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 7)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 50\text{ A}, R_G = 3.0\ \Omega$		12		ns
Rise Time	t_r			116		
Turn-Off Delay Time	$t_{d(OFF)}$			25		
Fall Time	t_f			10		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 50\text{ A}, R_G = 3.0\ \Omega$		9		ns
Rise Time	t_r			102		
Turn-Off Delay Time	$t_{d(OFF)}$			33		
Fall Time	t_f			6		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 20\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.1	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 50\text{ A}$		42		ns	
Charge Time	t_a			21			
Discharge Time	t_b			21			
Reverse Recovery Charge	Q_{RR}			28		nC	

6. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

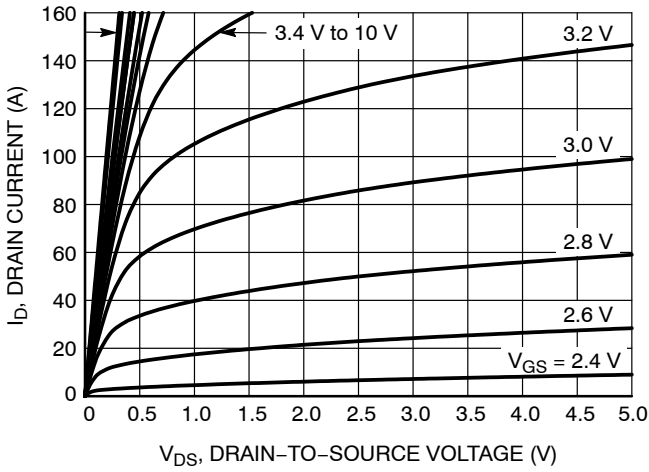


Figure 1. On-Region Characteristics

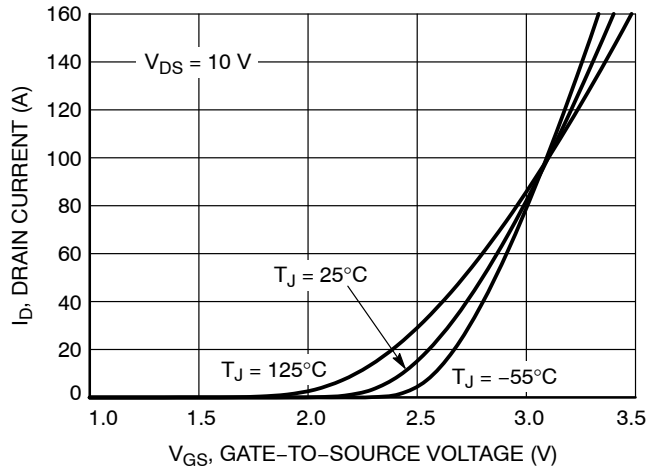


Figure 2. Transfer Characteristics

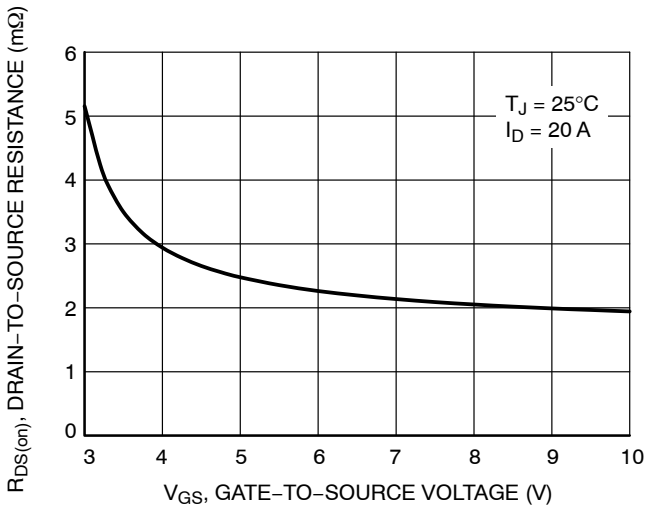


Figure 3. On-Resistance vs. Gate-to-Source Voltage

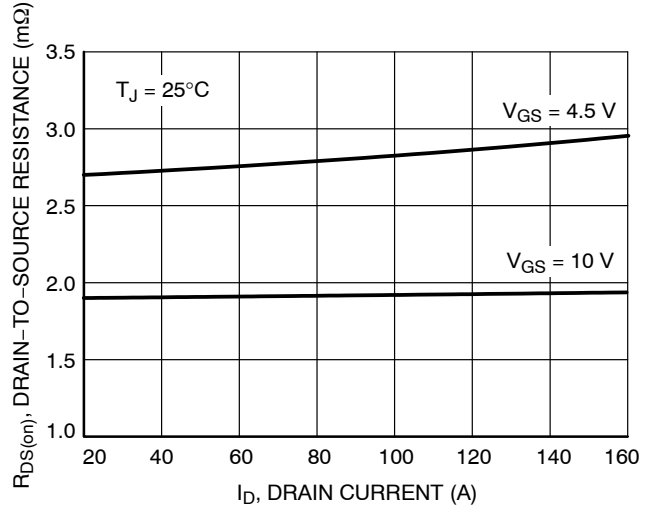


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

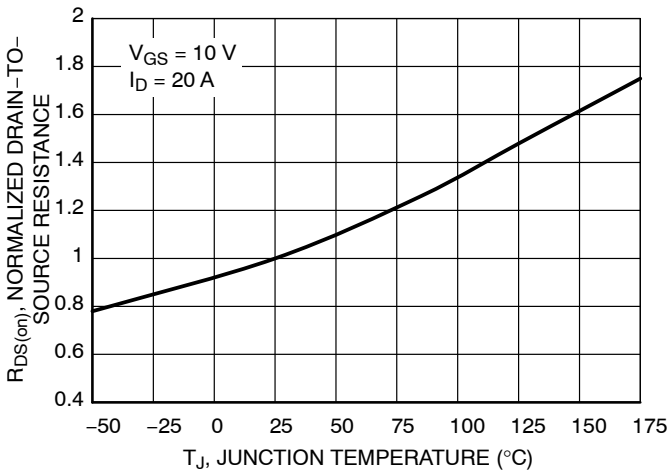


Figure 5. On-Resistance Variation with Temperature

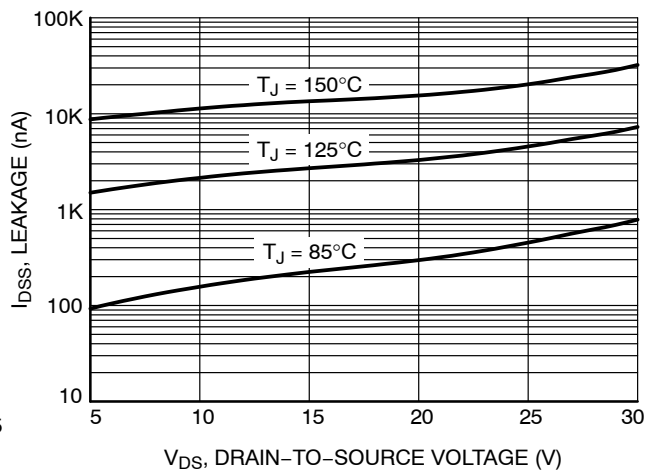


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

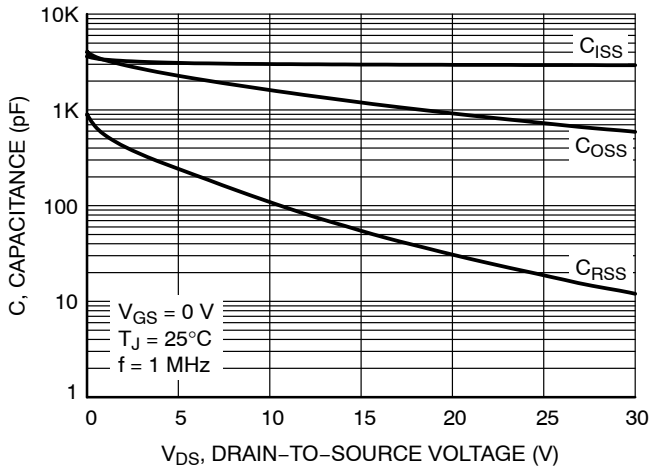


Figure 7. Capacitance Variation

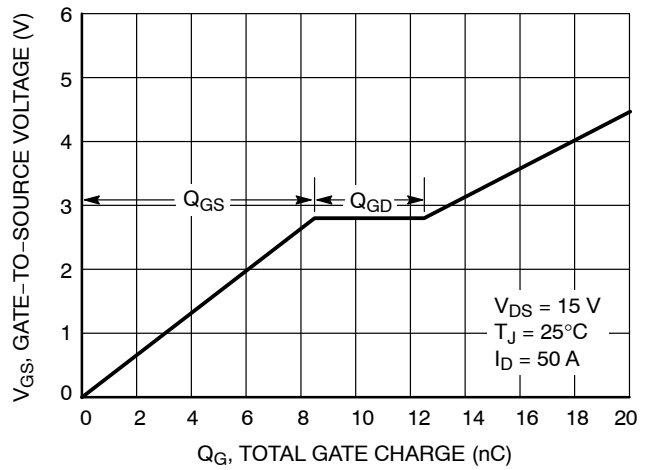


Figure 8. Gate-to-Source vs. Total Charge

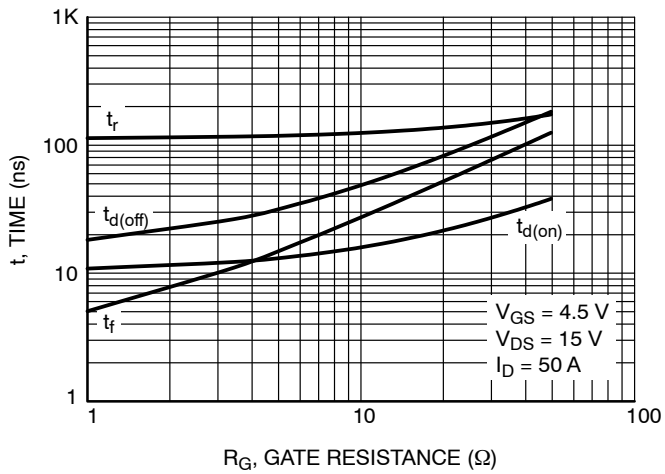


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

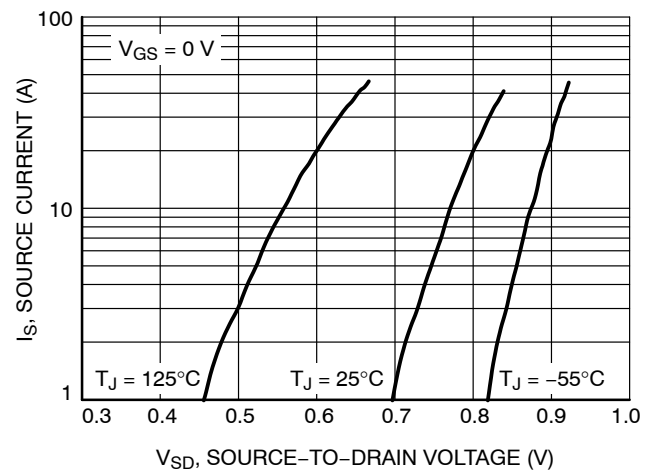


Figure 10. Diode Forward Voltage vs. Current

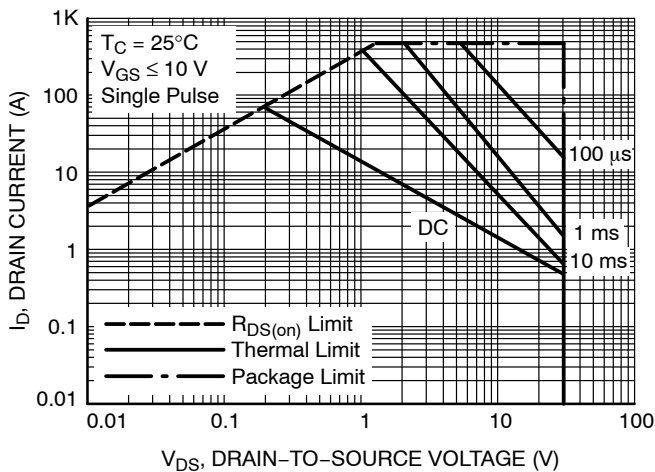


Figure 11. Maximum Rated Forward Biased Safe Operating Area

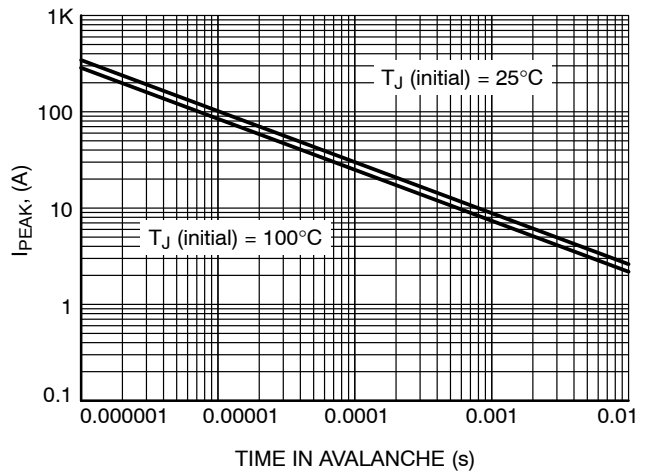


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

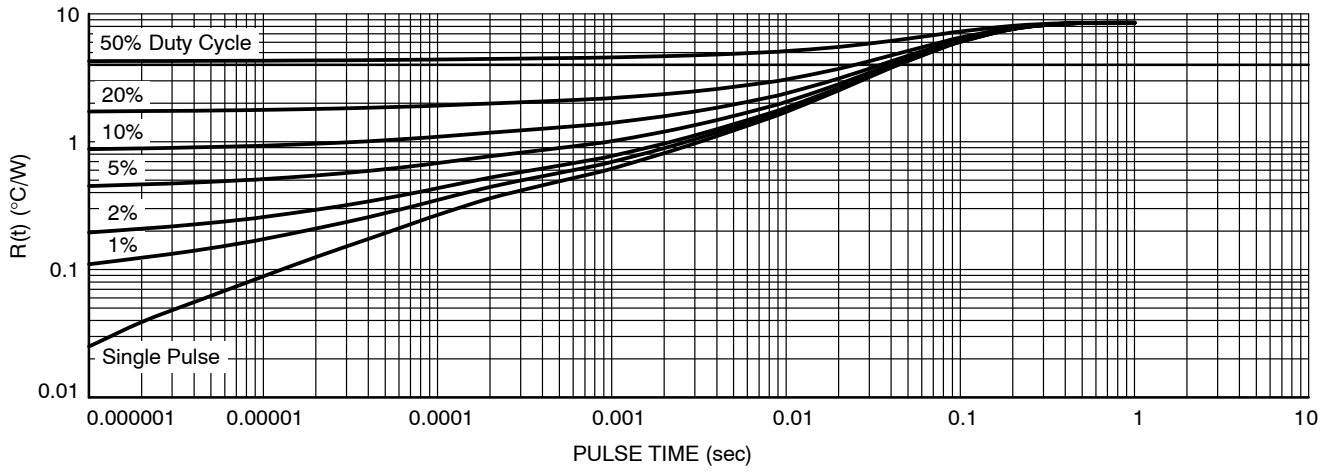


Figure 13. Thermal Characteristics

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

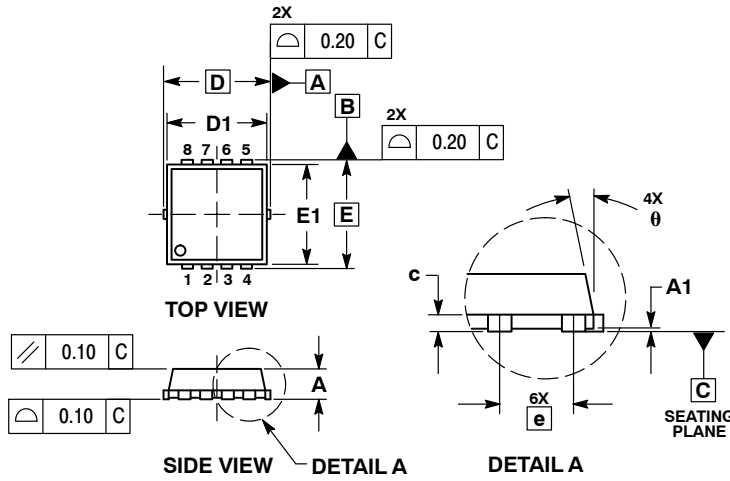
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SCALE 2:1

WDFN8 3.3x3.3, 0.65P CASE 511AB ISSUE D

DATE 23 APR 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°



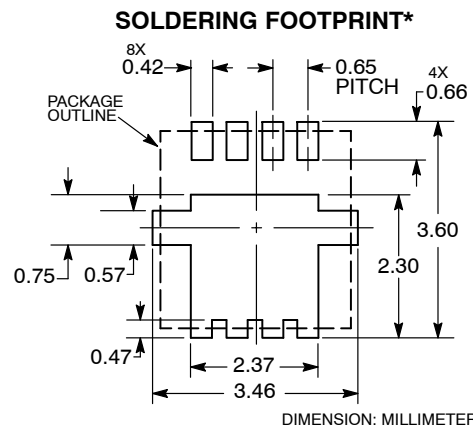
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "▪", may or may not be present.



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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