# CSPEMI204

# EMI Filter with ESD Protection

### Product Description

The CSPEMI204 is an L−R−C EMI filter array with ESD protection that integrates two Pi−filters (C−L−R−C) to suppress EMI/RFI Noise. CSPEMI204 includes ESD protection diodes on all input/output pins, and provides a very high level of protection for sensitive electronic components against possible electrostatic discharge (ESD). The ESD diodes connected to the filter ports safely dissipate ESD strikes of ±30 kV, which is beyond the maximum requirement of the IEC61000−4−2 international standard.

### Features

- Two Channels of EMI Filtering
- ±30 kV ESD Protection (IEC 61000−4−2, Contact Discharge)
- ±30 kV ESD Protection (IEC 61000−4−2, Air Discharge)
- Greater than 45 dB of Attenuation at 900 MHz
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Mobile Phones

**MAXIMUM RATINGS** ($T_A$ = 25°C)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| ESD Discharge IEC61000−4−2<br>Contact Discharge<br>Air Discharge | $V_{pp}$ | <br>30<br>30 | kV |
| RMS Current per Line | $I_{Line}$ | 350 | mA |
| Operating Temperature Range | $T_J$ | −40 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Lead Solder Temperature (10 second duration) | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

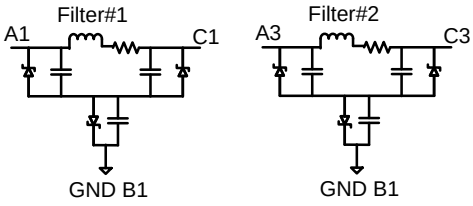
**ON Semiconductor®**

www.onsemi.com



**WLCSP5**
**FC SUFFIX**
**CASE 567MA**

### BLOCK DIAGRAM




### MARKING DIAGRAM




AT = Specific Device Code
M = Date Code

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| CSPEMI204FCTAG | WLCSP5 (Pb−Free) | 5000 / Tape & Reel |

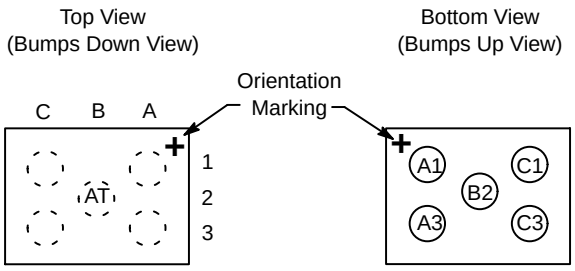
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**Table 1. PIN DESCRIPTIONS**

| Pin | Name | Description |
|---|---|---|
| A1 | Filter #1 | Filter #1 Input/Output |
| C1 | Filter #1 | Filter #1 Input/Output |
| A3 | Filter #2 | Filter #2 Input/Output |
| C3 | Filter #2 | Filter #2 Input/Output |
| B2 | GND | Device Ground |

**PACKAGE/PINOUT DIAGRAMS**




WLCSP5 Package

**Table 2. ELECTRICAL OPERATING CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Working Voltage | | | 3.0 | | V |
| $V_{BR}$ | Breakdown Voltage | $I_T$ = 1 mA; (Note 4) | 6.0 | | | V |
| $I_{LEAK}$ | Channel Leakage Current | $V_{IN}$ = 3.0 V, GND = 0 V | | | 400 | nA |
| $R_{CH}$ | Channel Resistance<br>(Pins A1 – A3, C1 – C3) | | | | 3.0 | Ω |
| $C_t$ | Line Capacitance | $V_R$ = 0 V, f = 1 MHz | 185 | 250 | 315 | pF |
| $f_{3dB}$ | Cut-off Frequency | 450 Ω Source and<br>10 kΩ Load Termination | | 2.0 | | MHz |
| $f_{3dB}$ | Cut-off Frequency | 50 Ω Termination | | 25 | | MHz |
| $F_{atten}$ | Stop Band Attenuation | @ 700 MHz<br>@ 900 MHz | | 40<br>47 | | dB |
| $V_{ESD}$ | In-system ESD Withstand Voltage<br>a) Contact discharge per IEC 61000-4-2 standard, Level 4 **(External Pins)**<br>b) Contact discharge per IEC 61000-4-2 standard, Level 1 **(Internal Pins)** | (Notes 1 and 2) | <br>±30<br><br>±30 | | | kV |
| $V_{CL}$ | TLP Clamping Voltage | Forward $I_{PP}$ = 8 A<br>Forward $I_{PP}$ = 16 A<br>Forward $I_{PP}$ = ±8 A<br>Forward $I_{PP}$ = ±16 A | | 9.8<br>11.5<br>−9.7<br>−11.7 | | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Standard IEC61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330, GND grounded.
2. These measurements performed with no external capacitor.
3. TVS devices are normally selected according to the working peak reverse voltage ($V_{RWM}$), which should be equal to or greater than the DC or continuous peak operating voltage level.
4. $V_{BR}$ is measured at pulse test current $I_T$.

## PERFORMANCE INFORMATION

### Typical Filter Performance

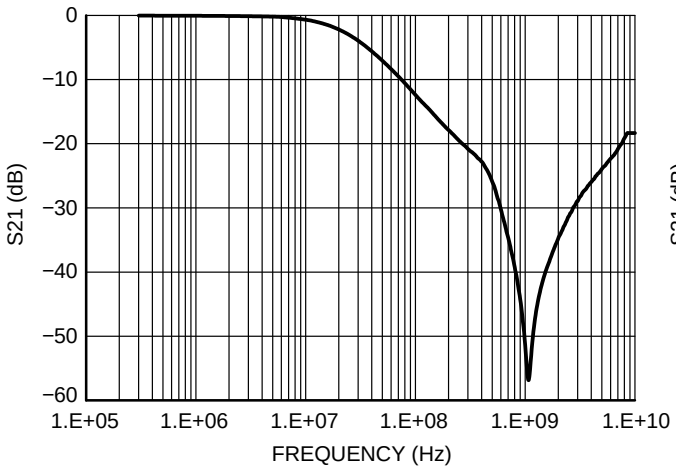



**Figure 1. Typical Insertion Loss (50 Ω Termination)**

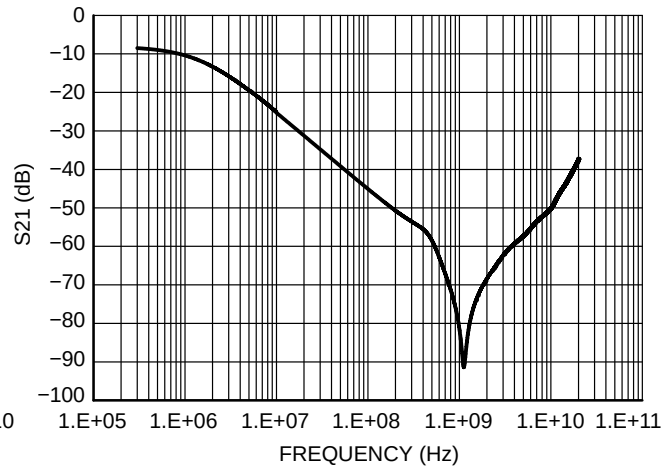



**Figure 3. Typical Insertion Loss (450 Ω Source and 10 kΩ Load Termination)**

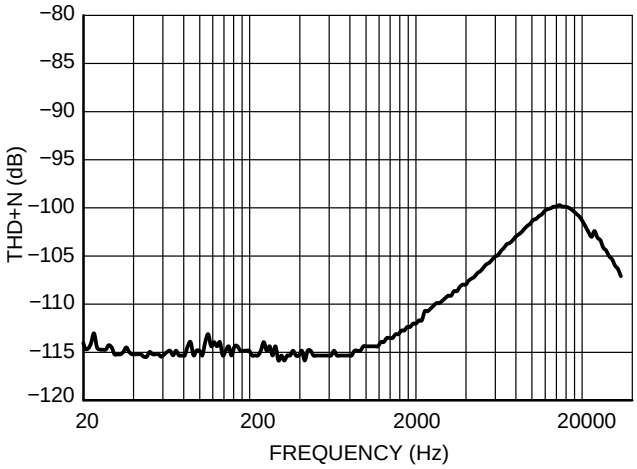



**Figure 2. Typical THD+N at 1.8 $V_{pp}$**

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

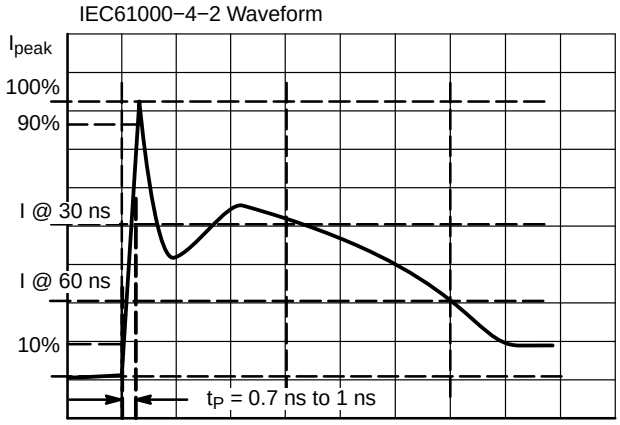



**Figure 4. IEC61000−4−2 Spec**

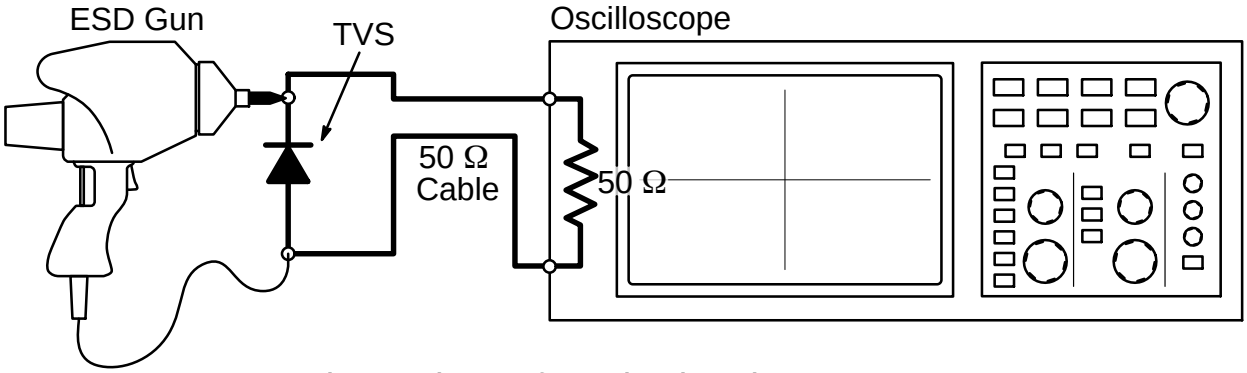



**Figure 5. Diagram of ESD Clamping Voltage Test Setup**

**The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.**

**ESD Voltage Clamping**

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

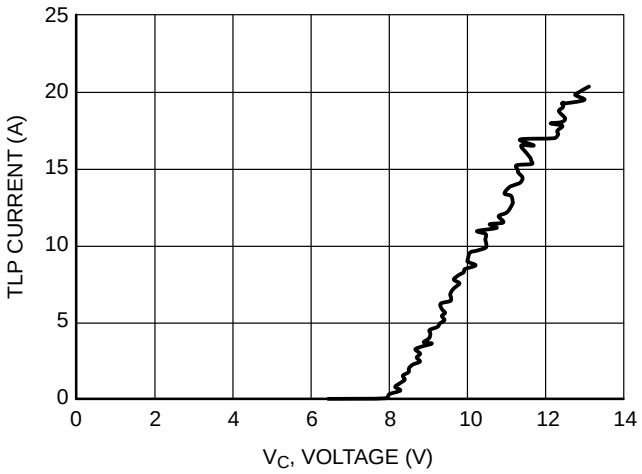



**Figure 6. Positive TLP I−V Curve (Preliminary)**

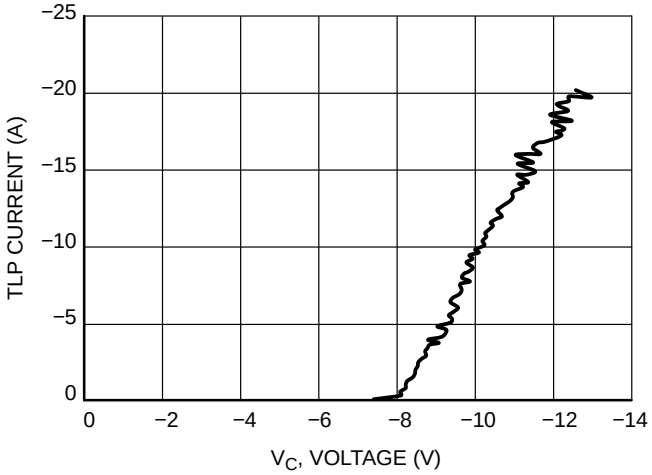



**Figure 7. Negative TLP I−V Curve (Preliminary)**

NOTE: TLP parameter: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 300 ps, averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns. $V_{IEC}$ is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

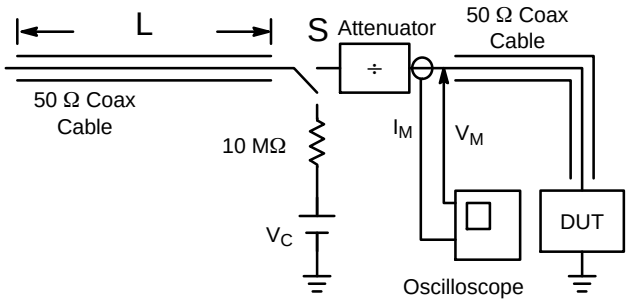



**Figure 8. Simplified Schematic of a Typical TLP System**

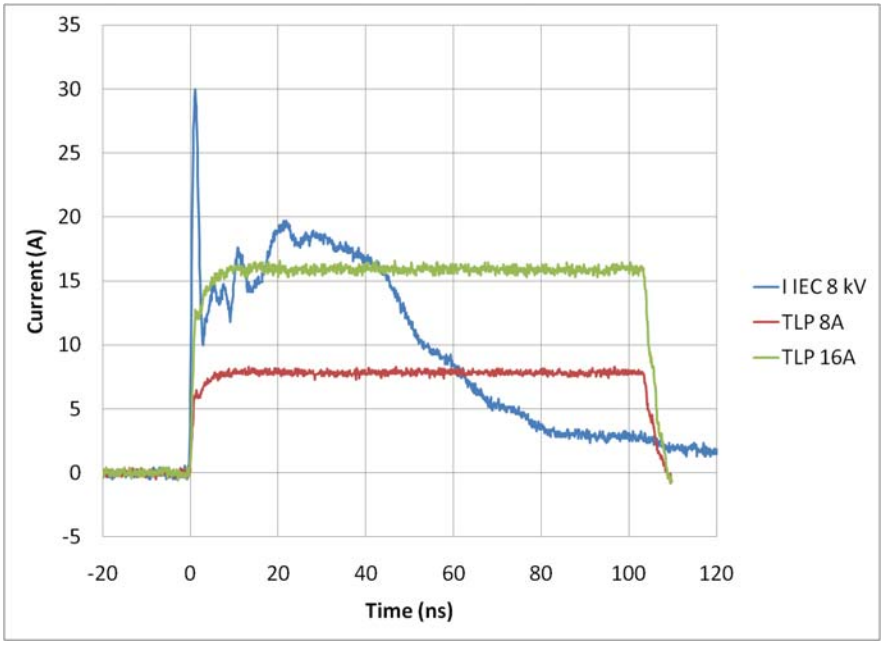



**Figure 9. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

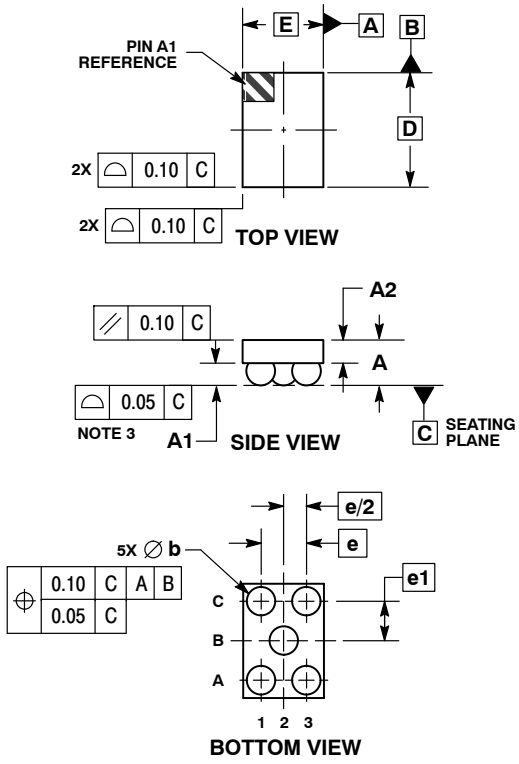
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 4:1

**WLCSP5, 1.26x0.89**
CASE 567MA
ISSUE O

DATE 07 JUL 2015




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 0.50 |
| A1 | 0.18 | 0.22 |
| A2 | 0.255 REF | |
| b | 0.235 | 0.295 |
| D | 1.26 BSC | |
| E | 0.89 BSC | |
| e | 0.50 BSC | |
| e1 | 0.435 BSC | |

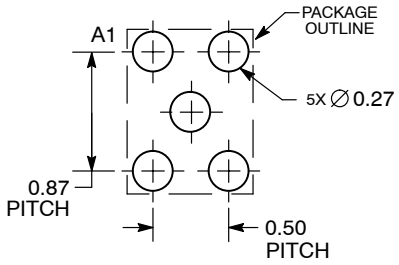
### GENERIC MARKING DIAGRAM*




XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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