CAT5132

16 Volt Digital Potentiometer (POT) with 128 Taps and I²C Interface

Description

The CAT5132 is a high voltage digital POT with non-volatile wiper setting memory, operating like a mechanical potentiometer. The tap points between the 127 equal resistive elements are connected to the wiper output via CMOS switches. The switches are controlled by a 7-bit Wiper Control Register (WCR). The wiper setting can be stored in a 7-bit non-volatile Data Register (DR). The WCR is accessed via the I^2C serial bus.

Upon power-up, the WCR is set to mid-scale (1000000). After the power supply is stable, the contents of the DR are transferred to the WCR and the wiper is returned to the memorized setting.

The CAT5132 has two voltage supplies: V_{CC}, the digital supply and V+, the analog supply. V+ can be much higher than V_{CC}, allowing for 16 V analog operations.

The CAT5132 can be used as a potentiometer or as a two-terminal variable resistor.

Features

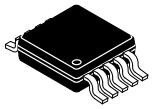
- Single Linear Digital Potentiometer with 128 Taps
- End-to-end Resistance of 10 kΩ, 50 kΩ or 100 kΩ
- I^2C Interface
- Fast Up/Down Wiper Control Mode
- Non-volatile Wiper Setting Storage
- Automatic Wiper Setting Recall at Power−up
- Digital Supply Range (V_{CC}): 2.7 V to 5.5 V
- Analog Supply Range (V+): +8 V to +16 V
- Low Standby Current: 15 μA
- 100 Year Wiper Setting Memory
- Industrial Temperature Range: −40°C to +85°C
- 10-pin MSOP Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- LCD Screen Adjustment
- Volume Control
- Mechanical Potentiometer Replacement
- Gain Adjustment
- Line Impedance Matching
- VCOM Setting Adjustments

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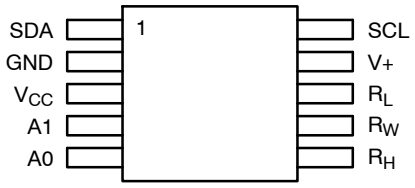
MSOP−10
Z SUFFIX
CASE 846AE

MARKING DIAGRAM



ANBU = CAT5132ZI-10-GT3
ANBK = CAT5132ZI-50-GT3
ANBP = CAT5132ZI-00-GT3
Y = Production Year (Last Digit)
M = Production Month (1-9, A, B, C)
R = Production Revision

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
CAT5132ZI−10−GT3	MSOP (Pb−Free)	3,000 / Tape & Reel
CAT5132ZI−50−GT3		
CAT5132ZI−00−GT3		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

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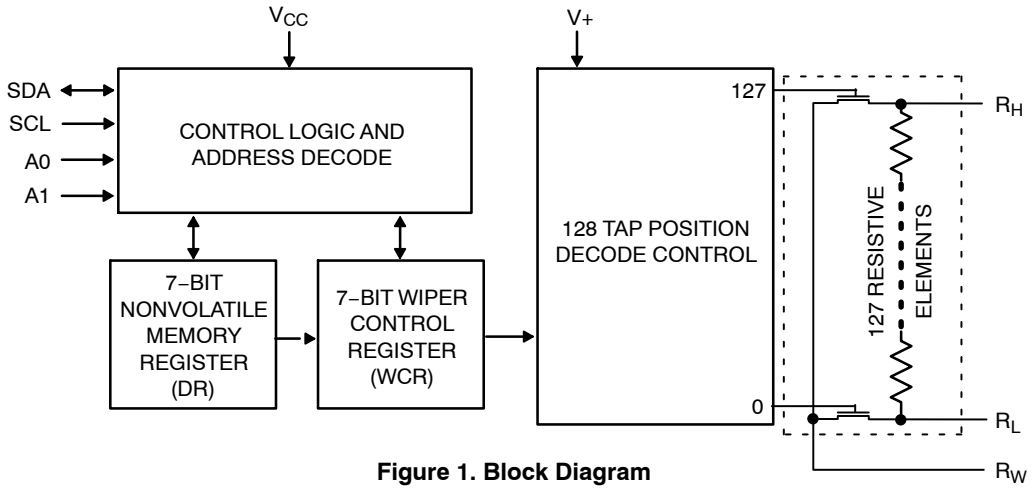


Figure 1. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	SDA	Serial Data Input/Output − Bidirectional Serial Data pin used to transfer data into and out of the CAT5132. This is an Open-Drain I/O and can be wire OR'd with other Open-Drain (or Open Collector) I/Os.
2	GND	Ground
3	V_{CC}	Digital Supply Voltage (2.7 V to 5.5 V)
4	A1	Address Select Input to select slave address for I^2C bus.
5	A0	Address Select Input to select slave address for I^2C bus.
6	R_H	High Reference Terminal for the potentiometer
7	R_W	Wiper Terminal for the potentiometer
8	R_L	Low Reference Terminal for the potentiometer
9	V+	Analog Supply Voltage for the potentiometer (+8.0 V to 16.0 V)
10	SCL	Serial Bus Clock input for the I^2C Serial Bus. This clock is used to clock all data transfers into and out of the CAT5132

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on any SDA, SCL, A0 & A1 pins with respect to Ground (Note 4)	−0.3 to V_{CC} + 0.3	V
Voltage on R_H, R_L & R_W pins with respect to Ground	V+	
V_{CC} with respect to Ground	−0.3 to +6	V
V+ with respect to Ground	−0.3 to +16.5	V
Wiper Current (10 sec)	±6	mA
Lead Soldering temperature (10 sec)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −0.3 V to V_{CC} +0.3 V.

Table 3. RECOMMENDED OPERATING CONDITIONS

Rating	Value	Unit
V_{CC}	+2.7 to +5.5	V
V+	+8.0 to +16	V
Operating Temperature Range	−40 to +85	°C

Table 4. POTENTIOMETER CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
R_{POT}	Potentiometer Resistance (100 kΩ)			100		kΩ
R_{POT}	Potentiometer Resistance (50 kΩ)			50		kΩ
R_{POT}	Potentiometer Resistance (10 kΩ)			10		kΩ
R_{TOL}	Potentiometer Resistance Tolerance				±20	%
	Power Rating	25°C			50	mW
I_W	Wiper Current				±3	mA
R_W	Wiper Resistance	I_W = ±1 mA @ V+ = 12 V		70	150	Ω
		I_W = ±1 mA @ V+ = 8 V		110	200	Ω
V_{TERM}	Voltage on R_W, R_H or R_L	GND = 0 V; V+ = 8 V to 16 V	GND		V+	V
RES	Resolution			0.78		%
A_{LIN}	Absolute Linearity (Note 6)	$V_{W(n)(actual)} - V_{W(n)(expected)}$ (Notes 9, 10)			±1	LSB (Note 8)
R_{LIN}	Relative Linearity (Note 7)	$V_{W(n+1)} - [V_{W(n)} + LSB]$ (Notes 9, 10)			±0.5	LSB (Note 8)
TC_{RPOT}	Temperature Coefficient of R_{POT}	(Note 5)		±300		ppm/°C
TC_{Ratio}	Ratiometric Temperature Coefficient	(Note 5)			30	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	(Note 5)		10/10/25		pF
fc	Frequency Response	R_{POT} = 50 kΩ		0.4		MHz

5. This parameter is tested initially and after a design or process change that affects the parameter.
6. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
7. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer.
8. LSB = $(R_{HM} - R_{LM})/127$; where R_{HM} and R_{LM} are the highest and lowest measured values on the wiper terminal.
9. n = 1, 2, ..., 127
10. V^+ @ R_H; 0 V @ R_L; V_W measured @ R_W with no load.

Table 5. D.C. ELECTRICAL CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Volatile Write/Read)	F_{SCL} = 400 kHz, SDA Open, V_{CC} = 5.5 V, Input = GND		1	mA
I_{CC2}	Power Supply Current (Nonvolatile WRITE)	F_{SCL} = 400 kHz, SDA Open, V_{CC} = 5.5 V, Input = GND		3.0	mA
$I_{SB(VCC)}$	Standby Current (V_{CC} = 5 V)	V_{IN} = GND or V_{CC}, SDA = V_{CC}		5	μA
$I_{SB(V+)}$	V+ Standby Current	V_{CC} = 5 V, V+ = 16 V		10	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	μA
V_{IL}	Input Low Voltage		−1	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 3.0)	I_{OL} = 3 mA		0.4	V

Table 6. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V (Note 11)		8	pF
C_{IN}	Input Capacitance (A0, A1, SCL)	V_{IN} = 0 V (Note 11)		6	pF

Table 7. A.C. CHARACTERISTICS

Symbol	Parameter (see Figure 6)	V_{CC} = 2.7 – 5.5 V		Units
		Min	Max	
F_{SCL}	Clock Frequency		400	kHz
T_I (Note 11)	Noise Suppression Time Constant at SCL & SDA Inputs		50	ns
t_{AA}	SLC Low to SDA Data Out and ACK Out		1	μs
t_{BUF} (Note 11)	Time the bus must be free before a new transmission can start	1.2		μs
$t_{HD:STA}$	Start Condition Hold Time	0.6		μs
t_{LOW}	Clock Low Period	1.2		μs
t_{HIGH}	Clock High Period	0.6		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6		μs
$t_{HD:DAT}$	Data in Hold Time	0		ns
t_R (Note 11)	SDA and SCL Rise Time		0.3	μs
t_F (Note 11)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Conditions Setup Time	0.6		μs
t_{DH}	Data Out Hold Time	100		ns

11. This parameter is tested initially and after a design or process change that affects the parameter.

Table 8. POWER UP TIMING (Notes 12, 13)

Symbol	Parameter	Min	Max	Units
t_{PUR}	Power-up to Read Operation		1	ms
t_{PUW}	Power-up to Write Operation		1	ms

Table 9. WIPER TIMING

Symbol	Parameter	Min	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable	5	10	μs
t_{WRL}	Wiper Response Time After Instruction Issued	5	10	μs

Table 10. WRITE CYCLE LIMITS

Symbol	Parameter	Min	Max	Units
t_{WR}	Write Cycle Time (see Figure 7)		5	ms

The write cycle is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

Table 11. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (Note 12)	Endurance	MIL−STD−883, Test Method 1033	100,000		Cycles
T_{DR} (Note 12)	Data Retention	MIL−STD−883, Test Method 1008	100		Years

12. This parameter is tested initially and after a design or process change that affects the parameter.
13. t_{PUR} and t_{PUW} are the delays required from the time VCC is stable until the specified operation can be initiated.

TYPICAL PERFORMANCE CHARACTERISTICS

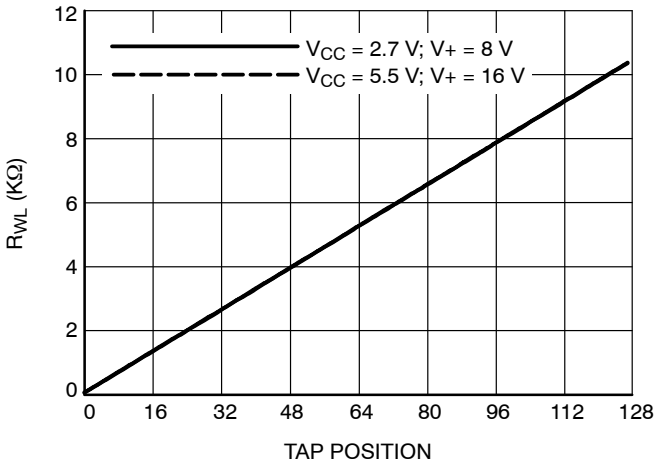


Figure 2. Resistance between R_W and R_L

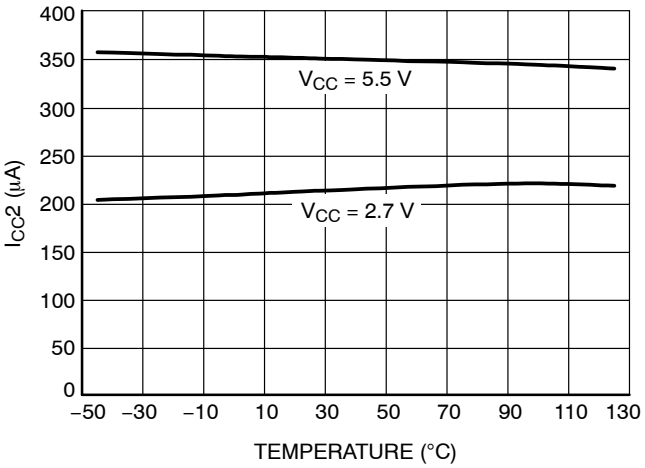


Figure 3. $I_{CC}2$ (NV Write) vs. Temperature

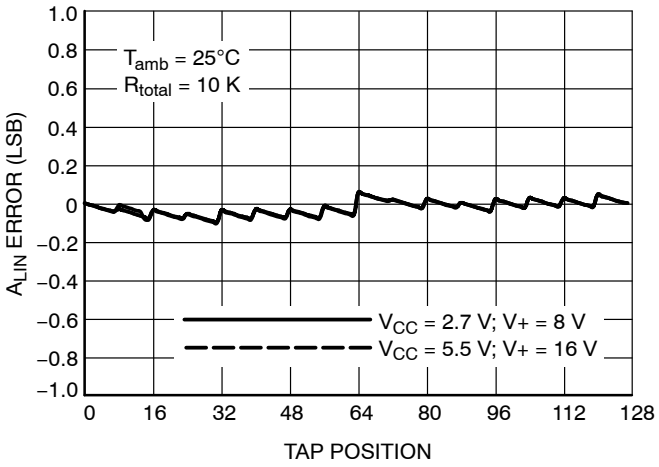


Figure 4. Absolute Linearity Error per Tap Position

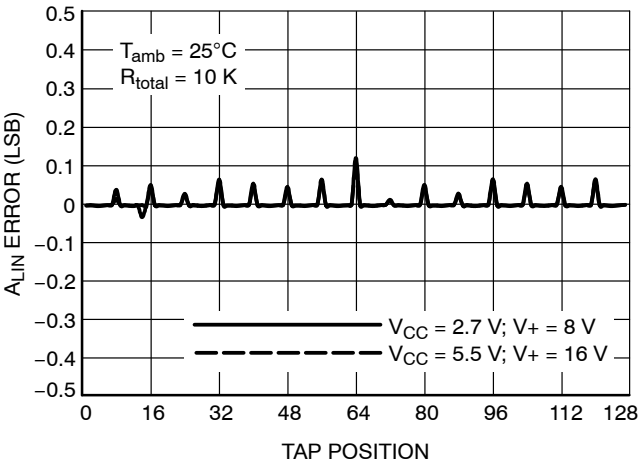


Figure 5. Relative Linearity Error

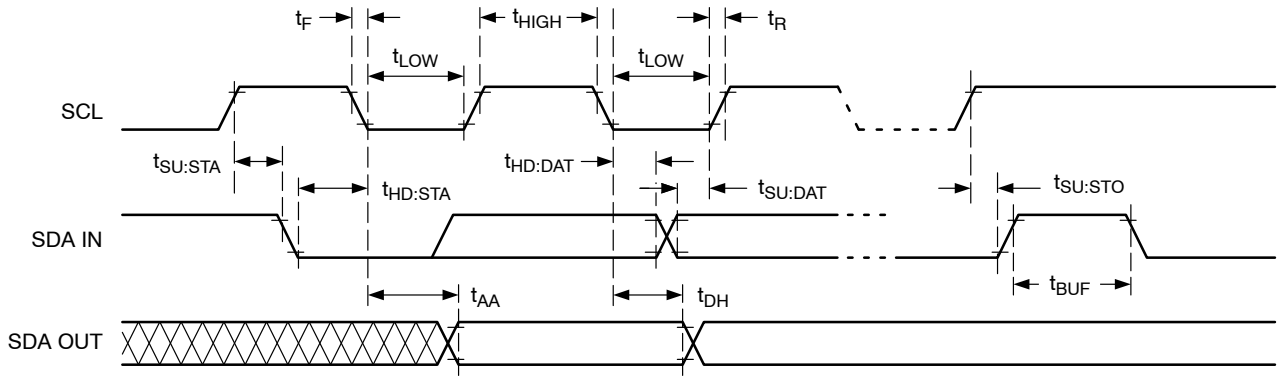


Figure 6. Bus Timing

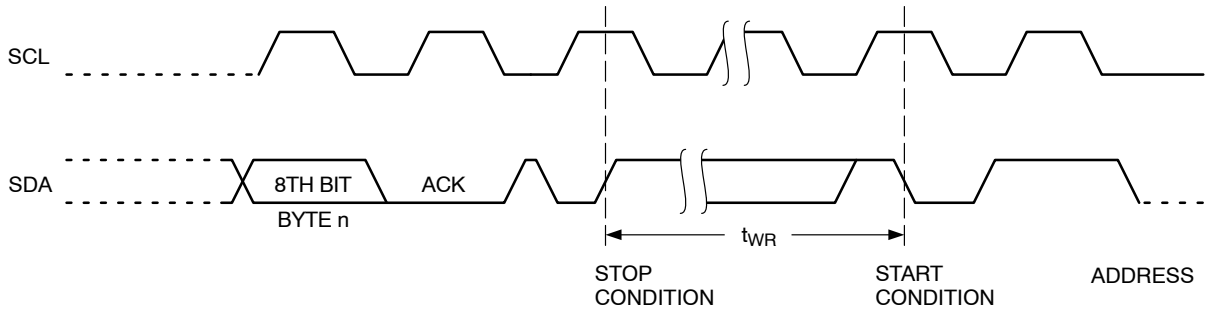


Figure 7. Write Cycle Timing

SERIAL BUS PROTOCOL

The following defines the features of the I^2C bus protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5132 will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT5132 monitors the SDA and SCL lines and will not respond until this condition is met (see Figure 8).

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition (see Figure 8).

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data (see Figure 9).

The CAT5132 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5132 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5132 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the STOP condition is issued to indicate the end of the write operation, the CAT5132 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the START condition followed by the slave address. If the CAT5132 is still busy with the write operation, no ACK will be returned. If the CAT5132 has completed the write operation, an ACK will be returned and the host can then proceed with the next instruction operation.

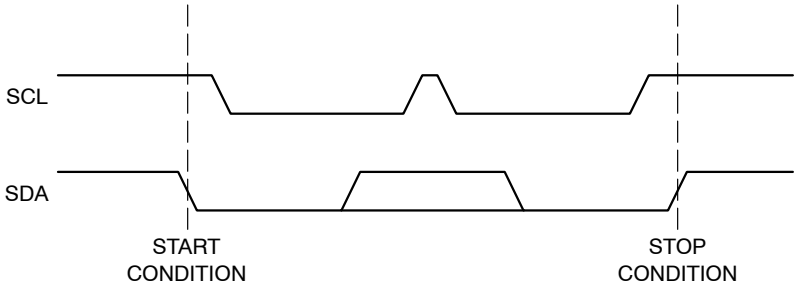


Figure 8. Start/Stop Condition

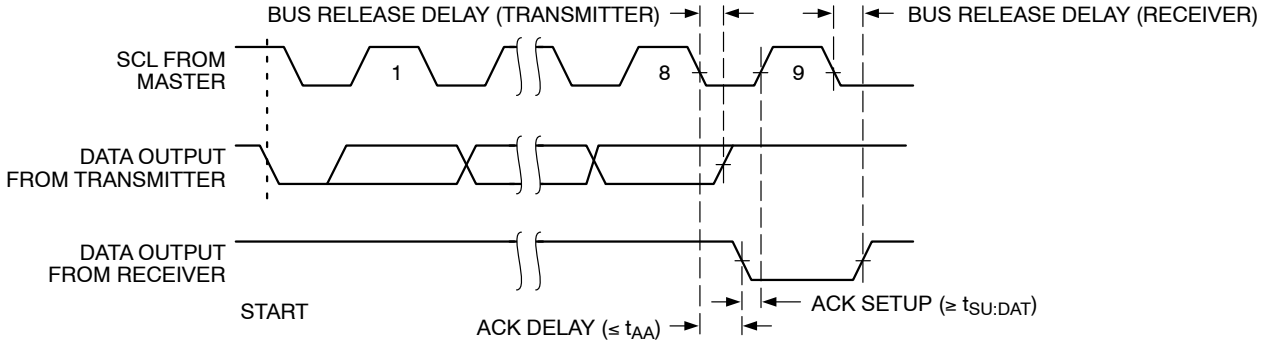


Figure 9. Acknowledge Condition

DEVICE DESCRIPTION

Access Control Register

The volatile register WCR and the non-volatile register DR are accessed only by addressing the volatile Access Register AR first, using the 3 byte I^2C protocol for all read and write operations (see Table 12). The first byte is the slave address/instruction byte (see details below). The second byte contains the address (02h) of the AR register. The data in the third byte controls which register WCR (80h) or DR (00h) is being addressed (see Figure 10).

Slave Address Instruction Byte Description

The first byte sent to the CAT5132 from the master processor is called the Slave Address Byte. The most significant five bits of the slave address are a device type identifier. For the CAT5132 these bits are fixed at 01010 (refer to Table 13).

The next two bits, A1 and A0, are the internal slave address and must match the physical device address which is defined by the state of the A1 and A0 input pins. Only the device with slave address matching the input byte will be accessed by the master. This allows up to 4 devices to reside on the same bus. The A1 and A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or Ground.

The last bit is the READ/WRITE bit and determines the function to be performed. If it is a “1” a read command is initiated and if it is a “0” a write is initiated. For the AR register only write is allowed.

After the Master sends a START condition and the slave address byte, the CAT5132 monitors the bus and responds with an acknowledge when its address matches the transmitted slave address.

Table 12. ACCESS CONTROL REGISTER

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address – 02h									WCR(80h) / DR(00h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	SP

Table 13. BYTE 1 SLAVE ADDRESS AND INSTRUCTION BYTE

Device Type Identifier					Slave Address		Read/$\overline{\text{Write}}$
ID4	ID3	ID2	ID1	ID0	A1	A0	R/$\overline{\text{W}}$
0	1	0	1	0	X	X	X
(MSB)							(LSB)

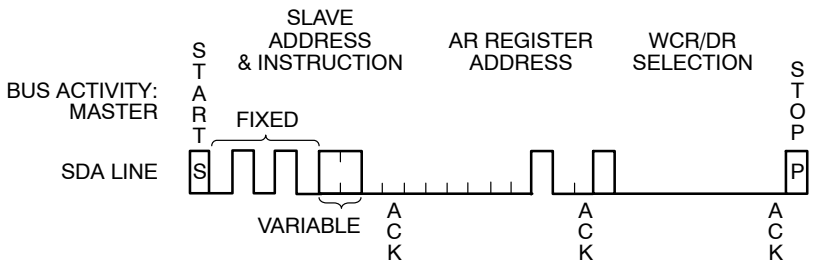


Figure 10. Access Register Addressing Using 3 Bytes

Wiper Control Register (WCR) Description

The CAT5132 contains a 7-bit Wiper Control Register which is decoded to select one of the 128 switches along its resistor array. The WCR is a volatile register and is written with the contents of the nonvolatile Data Register (DR) on power-up. The Wiper Control Register loses its contents when the CAT5132 is powered-down. The contents of the WCR may be read or changed directly by the host using a READ/WRITE command after addressing the WCR (see Table 12 to access WCR). Since the CAT5132 will only make use of the 7 LSB bits (The first data bit, or MSB, is ignored) on write instructions and will always come back as a “0” on read commands.

A write operation (see Table 14) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes the CAT5132 responds with an acknowledge. At this time the data is written only to volatile registers, then the device enters its standby state.

Table 14. WCR WRITE OPERATION

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address – 02h									WCR(80h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	WCR address – 00h								ACK	data byte								ACK	STOP
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	x	x	x	x	x	x	x	x	A	SP

An increment operation (see Table 15) requires a Start condition, followed by a valid increment address byte (01011), a valid address byte 00h. After each of the two bytes, the CAT5132 responds with an acknowledge. At this time if the data is high then the wiper is incremented or if the data is low the wiper is decremented at each clock. Once the stop is issued then the device enters its standby state with the WCR data as being the last inc/dec position. Also, the wiper position does not roll over but is limited to min and max positions.

Table 15. WCR INCREMENT/DECREMENT OPERATION

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address – 02h									WCR(80h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	WCR address – 00h								ACK	increment (1) / decrement (0) bits									STOP
ST	0	1	0	1	1	0	0	0	A	0	0	0	0	0	0	0	0	A	1	1	1	1	0	0	0	0		SP

A read operation (see Table 16) requires a Start condition, followed by a valid slave address byte for write, a valid address byte 00h, a second START and a second slave address byte for read. After each of the three bytes, the CAT5132 responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 16. WCR READ OPERATION

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address – 02h									WCR(80h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	WCR address – 00h								
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	

START	slave address byte									data byte									STOP
ST	0	1	0	1	0	0	0	1	A	0	X	X	X	X	X	X	X		SP

Data Register (DR)

The Data Register (DR) is a nonvolatile register and its contents are automatically written to the Wiper Control Register (WCR) on power-up. It can be read at any time without effecting the value of the WCR. The DR, like the WCR, only stores the 7 LSB bits and will report the MSB bit as a “0”. Writing to the DR is performed in the same fashion as the WCR except that a time delay of up to 5 ms is experienced while the nonvolatile store operation is being performed. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. The WCR is also written during a write to DR. After a DR WRITE is complete the DR and WCR will contain the same wiper position.

To write or read to the DR, first the access to DR is selected, see table 1 then the data is written or read using the following sequences.

A write operation (see Table 17) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes the CAT5132 responds with an acknowledge. At this time the data is written both to volatile and non-volatile registers, then the device enters its standby state.

Table 17. DR WRITE OPERATION

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address – 02h									DR(00h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	DR address – 00h								ACK	data byte								ACK	STOP
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	X	X	X	X	X	X	X	X	A	SP

A read operation (see Table 18) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a second Start and a second slave address byte for read. After each of the three bytes the CAT5132 responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 18. DR READ OPERATION

START	1st byte								ACK	2nd byte								ACK	3rd byte								ACK	STOP
	ID4	ID3	ID2	ID1	ID0	A1	A0	Wb		AR address – 02h									DR(00h) selection									
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	SP

START	slave address byte								ACK	DR address – 00h								
ST	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	

START	slave address byte									data byte									STOP
ST	0	1	0	1	0	0	0	1	A	0	X	X	X	X	X	X	X		SP

POTENTIOMETER OPERATION

Power-On

The CAT5132 is a 128-position, digital controlled potentiometer. When applying power to the CAT5132, V_{CC} must be supplied prior to or simultaneously with V+. At the same time, the signals on R_H, R_W and R_L terminals should not exceed V+. If V+ is applied before V_{CC}, the electronic switches are powered in the absence of the switch control signals, that could result in multiple switches being turned on. This causes unexpected wiper settings and possible current overload of the potentiometer. When V_{CC} is applied the device turns on at the mid-point wiper location (64) until the wiper register can be loaded with the nonvolatile memory location previously stored in the device. After the nonvolatile memory data is loaded into the wiper register the wiper location will change to the previously stored wiper position.

At power-down, it is recommended to turn-off first the signals on R_H, R_W and R_L, followed by V+ and, after that, V_{CC}, in order to avoid unexpected transmissions of the wiper and uncontrolled current overload of the potentiometer.

The end-to-end nominal resistance of the potentiometer has 128 contact points linearly distributed across the total resistor. Each of these contact points is addressed by the 7 bit wiper register which is decoded to select one of these 128 contact points.

Each contact point generates a linear resistive value between the 0 position and the 127 position. These values can be determined by dividing the end-to-end value of the potentiometer by 127. In the case of the 10 kΩ potentiometer ~79 Ω is the resistance between each wiper position. However in addition to the ~79 Ω for each resistive segment of the potentiometer, a wiper resistance offset must be considered. Table 19 shows the effect of this value and how it would appear on the wiper terminal.

This offset will appear in each of the CAT5132 end-to-end resistance values in the same way as the 10 kΩ example. However resistance between each wiper position for the 50 kΩ version will be ~395 Ω and for the 100 kΩ version will be ~790 Ω.

Table 19. POTENTIOMETER RESISTANCE AND WIPER RESISTANCE OFFSET EFFECTS

Position	Typical R_W to R_L Resistance for 10 kΩ Digital POT	
00	70 Ω or	0 Ω + 70 Ω
01	149 Ω or	79 Ω + 70 Ω
63	5,047 Ω or	4,977 Ω + 70 Ω
127	10,070 Ω or	10,000 Ω + 70 Ω
Position	**Typical R_W to R_H Resistance for 10 kΩ Digital POT**	
00	10,070 Ω or	10,000 Ω + 70 Ω
64	5,047 Ω or	4,977 Ω + 70 Ω
126	149 Ω or	79 Ω + 70 Ω
127	70 Ω or	0 Ω + 70 Ω

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