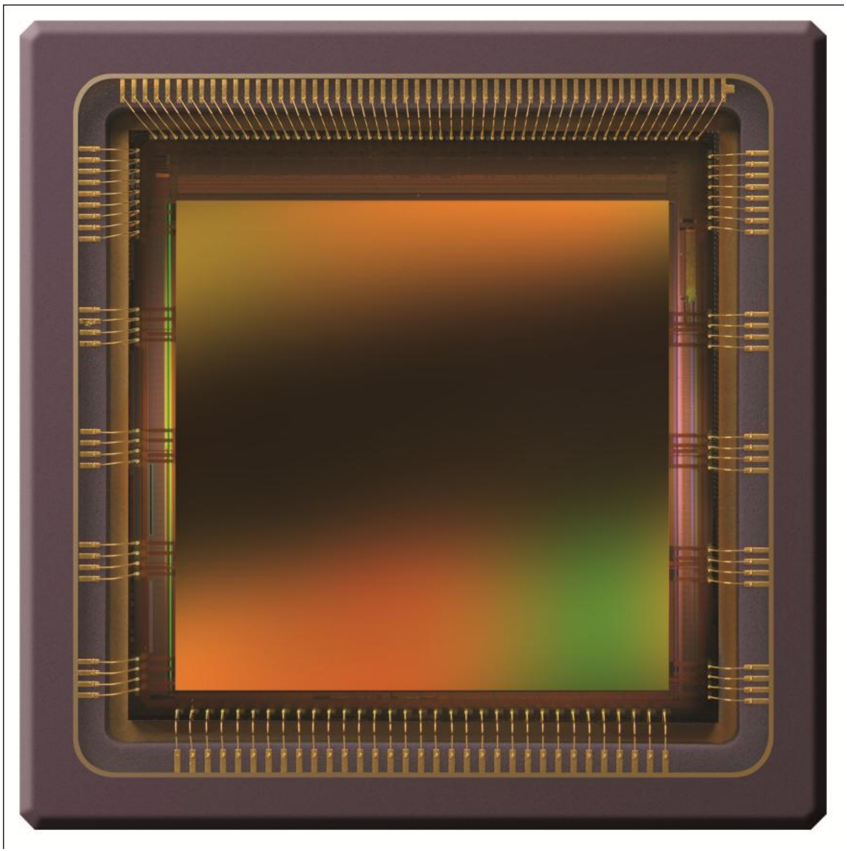
4.2 Megapixel machine vision CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
1	06/05/09	Origination
1.1	12/11/09	- Corrected register address of sub_s[7:0] to '35' (p 29/30/33)
1.2	11/01/10	Adjusted min input frequency (section 3.3) Changed 3.0V to 2.8V for Vpix
1.3	14/01/10	Adjusted pin width in package drawing
2	29/03/10	Added spectral response Added spectral response for color devices Updated specifications for version 2 devices Changed VDD18 to VDD20 Added ordering info Added handling and soldering procedures Removed "confidential" in footer Added recommended and adjustabel register settings
2.1	22/7/10	Frame rate calculation added
2.2	2/8/10	Read-out in 12 bit mode added
2.3	1/9/10	Added exposure time offset (0.65 x register73 x clk_per x 129)
2.4	17/9/10	Added Vtf_l1 to GND remark
2.5	19/10/10	Added E12 spectral response curve and part numbers

Disclaimer

Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV4000 is a high speed CMOS image sensor with 2048 by 2048 pixels (1 optical inch) developed for machine vision applications. The image array consists of 5.5µm x 5.5µm pipelined global shutter pixels which allow exposure during read out, while performing CDS operation. The image sensor has sixteen 10- or 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 480 Mbps maximum which results in 180 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- 2048 * 2048 active pixels on a 5.5µm pitch
- frame rate 180 Frames/sec
- row windowing capability
- X-Y mirroring function
- Master clocks: 5-48MHz and 50-480MHz (LVDS)
- 16 LVDS-outputs @480MHz multiplexable to 8, 4 and 2 at reduced frame rate
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- 10 bit ADC output at maximum frame rate, 12 bit ADC at reduced frame rate
- Multiple High Dynamic Range modes supported
- On chip temperature sensor
- On chip timing generation
- SPI-control
- Ceramic µPGA package (95 pins)
- 3.3V signaling
- Available in panchromatic and Bayer (RGB)

1.3 SPECIFICATIONS

- Full well charge: 13.5Ke$^-$
- Sensitivity: 4.64 V/lux.s (with microlenses)
- Dark noise: 13e$^-$ RMS
- Conversion factor: 0.075LSB/e$^-$ (10 bit mode) at unity gain
- SNR: 60 dB
- Extended dynamic range: Piecewise linear response or interleaved read-out
- Parasitic light sensitivity: 1/50 000
- Dark current: 125 e/s (@ 25C die temp)
- Fixed pattern noise: <1 LSB (10 bit mode, <0.1% of full swing, standard deviation on full image)
- Power consumption: 600mW

1.4 CONNECTION DIAGRAM

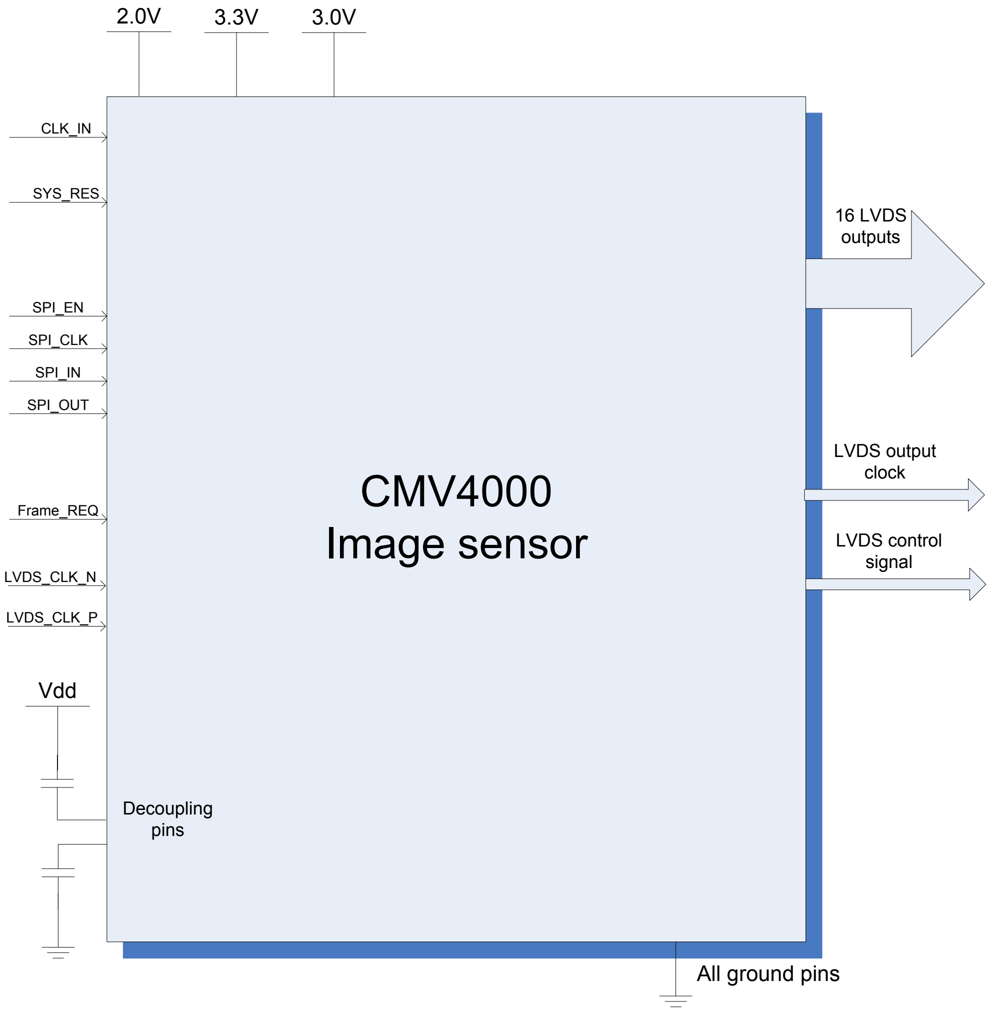


Figure 1: Connection diagram for the CMV4000 image sensor

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

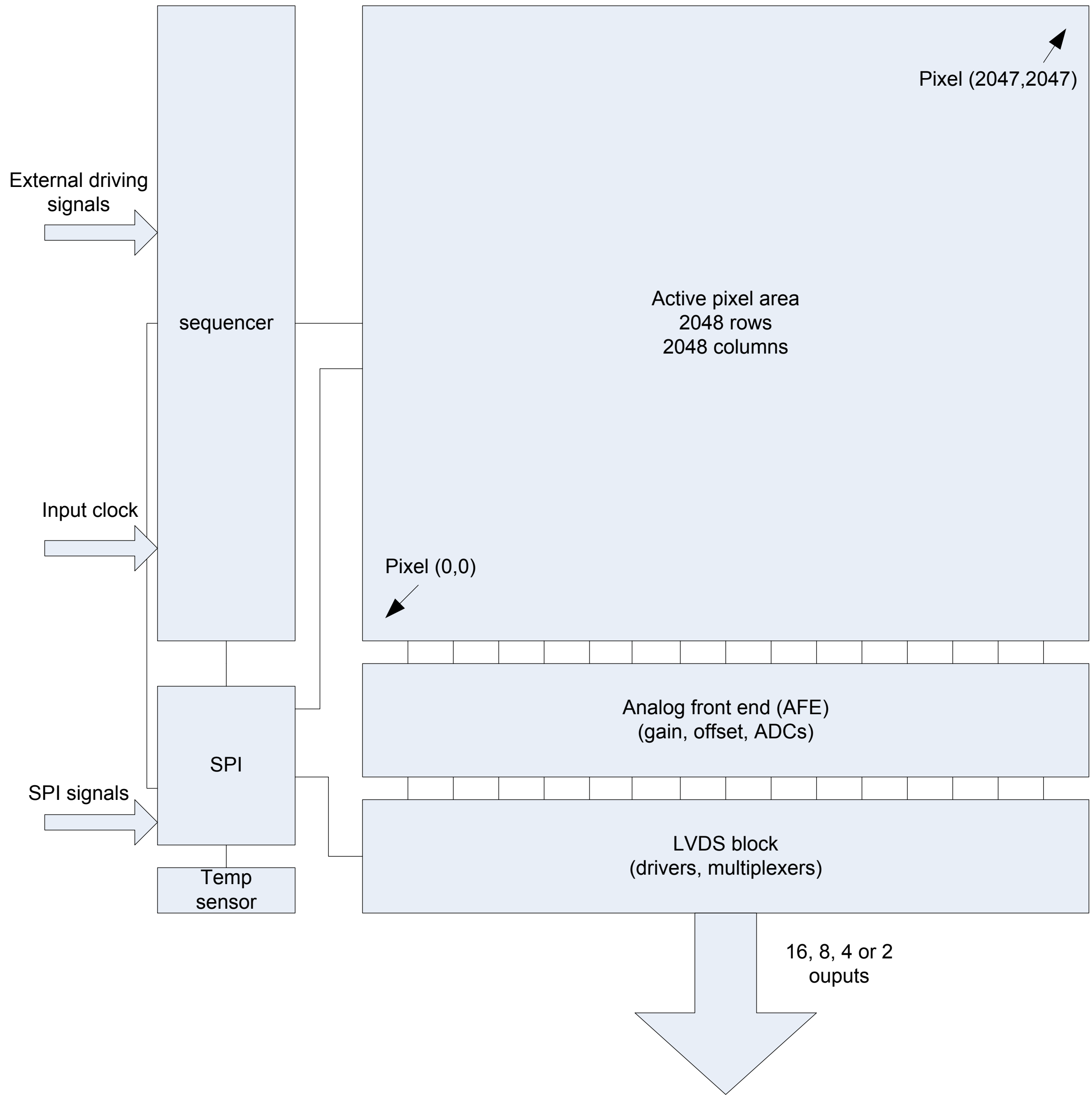


Figure 2: Sensor block diagram

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain of x1, x1.2, x1.4 and x1.6 is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 128 adjacent columns of the array. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 2048 x 2048 square global shutter pixels with a pitch of 5.5µm (5.5µm x 5.5µm). This results in an optical area of close to 1 optical inch (16mm). This means that off-the-shelve C-mount lenses can be used.

The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%).

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 10 or 12 bit value. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 480Mbps. The sensor has 18 LVDS output pairs:

- 16 Data channels
- 1 Control channel
- 1 Clock channel

The 16 data channels are used to transfer 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 4 of this document.

2.4 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.5 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming and SPI timing.

2.6 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 126 and 127 (in burst mode, see section 3.7.2 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements. A typical temperature sensor output vs temperature curve can be found below. The temperature sensor requires a running input clock (CLK_IN), the other functions of the image sensor can be operational or in standby mode.

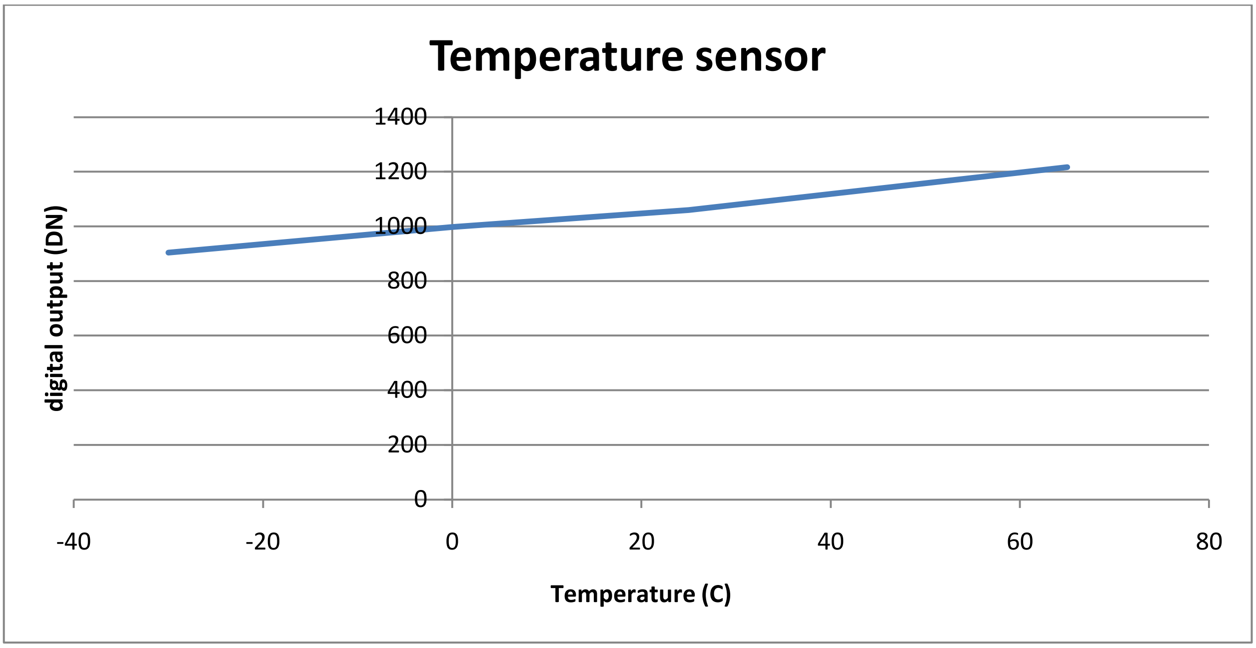


Figure 3: Typical output of the temperature sensor of the CMV4000

3 DRIVING THE CMV4000

3.1 SUPPLY SETTINGS

The CMV4000 image sensor has the following supply settings:

Supply name	Typical value	Range	Current nominal	Current peak
VDD20	2.0V	1.6V-2.1V	200mA	1A
VDD33	3.3V	3V-3.6V	100mA	0.5A
VDDpix	3.0V	2.3V-3.6V	20mA	0.6A
Vres_h	3.3V	3.0V-3.6V	NA	0.5A

See pin list for exact pin numbers for every supply.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor

Pin name	Description
CLK_IN	Master input clock, frequency range between 5 and 48 MHz
LVDS_CLK_N/P	High speed LVDS input clock, frequency range between 50 and 480 MHz
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
FRAME_REQ	Frame request pin. When a rising edge is detected on this pin the programmed number of frames is captured and sent by the sensor
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 48Mz)
T_EXP1	Input pin which can be used to program the exposure time externally. Optional
T_EXP2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. Optional

V_{IH}= 3.0V-3.3V
V_{IL}= 0.0V-0.3V

3.4 Input clock

The high speed LVDS input clock (LVDS_CLK_N/P) defines the output data rate of the CMV4000. The mastclock (CLK_IN) must be 10 or 12 times slower depending on the programmed bit mode setting. The maximum data rate of the output is 480Mbps which results in a LVDS_CLK_N/P of 480MHz and a CLK_IN of 48MHz in 10-bit mode and 40MHz in 12-bit mode. The minimum frequencies are 5MHz for CLK_IN and 50MHz for LVDS_CLK_N/P. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate.

3.5 Frame rate calculation

The frame rate of the CMV4000 is defined by 2 main factors.

1. Exposure time
2. Read out time

For ease of use we will assume that the exposure time is not longer than the read out time. By assuming this the frame rate is completely defined by the read out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 480Mbps
2. ADC mode: 10 or 12 bit
3. Number of lines read-out
4. Number of LVDS outputs used: max 16 outputs

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV4000. In normal operation (16 outputs @ 480Mbps, 10 bit and full resolution) this will result in 180 fps.

Total readout time is composed of two parts: FOT (frame overhead time) + image readout time

FOT = (FOT_REG_VALUE + (2 x 16/#outputs used)) x 129 x master clock period
==> When running the CMV4000 sensor at 48MHz with 16 outputs and default FOT settings this results in: 59us

Image read-out time = (129 x master clock period x 16/#outputs used) * nr_lines
==> When running the CMV4000 sensor at 48MHz with 16 outputs and reading 2048 lines this results in: 5.495ms

This results in a total read-out time of 59us + 5.495ms = 5.554ms ==> 180fps.

3.6 Start-up sequence

The following sequence should be followed when the CMV4000 is started up in default output mode (480Mbps, 10bit resolution).

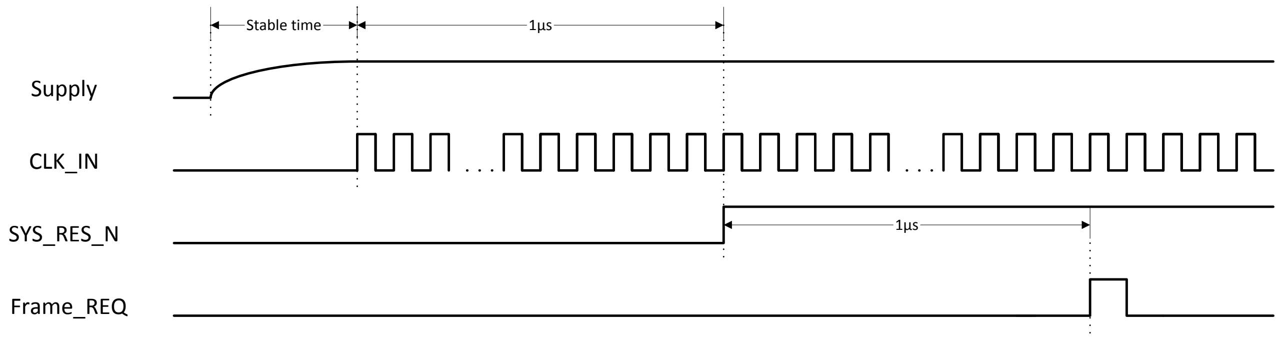


Figure 4: Start-up sequence for 480Mbps @ 10-bit

The masterclock (48MHz in for 480Mbps in 10-bit mode) should only start after the rise time of the supplies. The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the Frame_REQ pulse must be postponed until after the SPI upload has been completed.

When the CMV4000 will be used in 12-bit mode, an SPI upload is necessary to program the ADC and LVDS. In this case the start-up sequence looks like the diagram below.

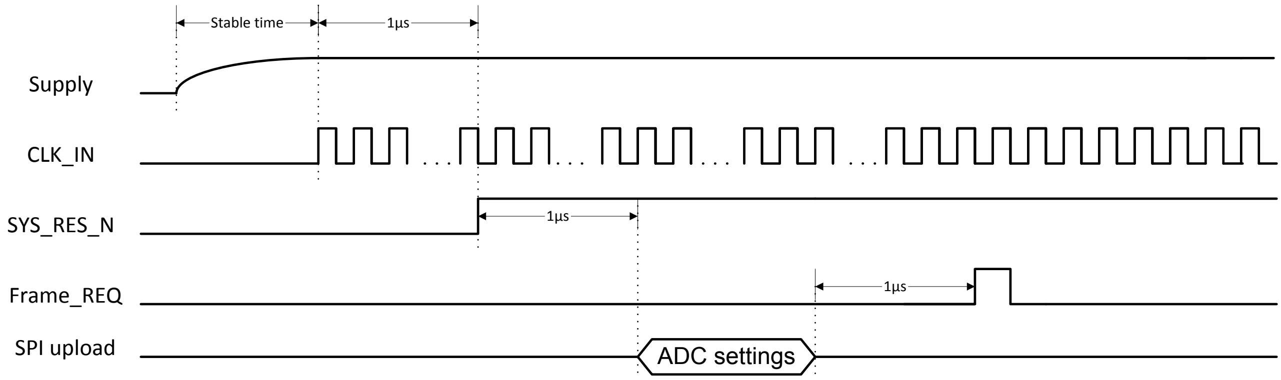


Figure 5: Start-up sequence for 12-bit mode

The following SPI registers (ADC and LVDS settings) should be uploaded in this mode:

1. LVDS settings (address 111) : set to 12 bit mode
2. ADC bit mode (address 112): set to 12 bit resolution

Note: As mentioned in section 3.3, for a lower output data rate only the input clocks need to be lowered.

3.7 Reset sequence

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

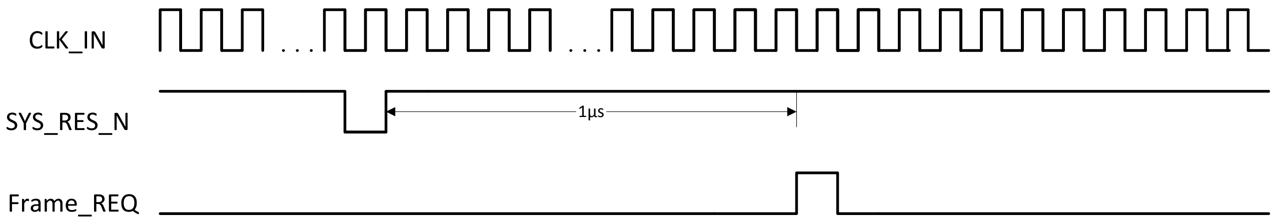


Figure 6: Reset sequence

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent.

When a switch from 10-bit to 12-bit mode (or vice versa) is necessary, the following sequence should be followed.

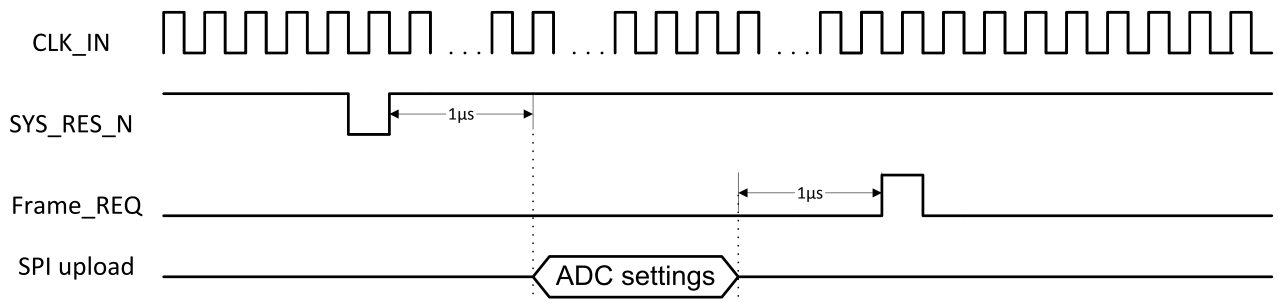


Figure 7: Reset sequence when changing bit mode

The following SPI registers (ADC settings) should be uploaded in this mode:

1. LVDS setting (address 111): set to desired bit resolution
2. ADC bit mode (address 112): set to desired bit resolution mode

Note: As mentioned in section 3.3, for a lower output data rate only the input clocks need to be lowered.

3.8 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

3.8.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

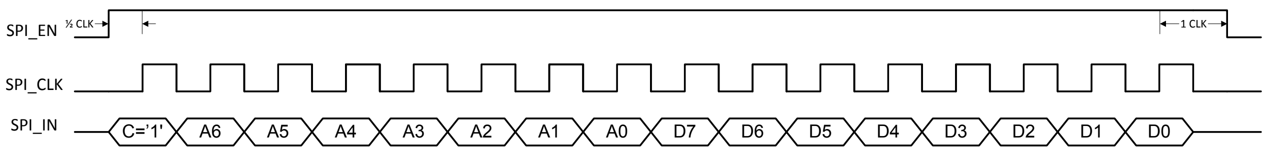


Figure 8: SPI write timing

The data is sampled by the CMV4000 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 48MHz. The SPI_EN signal has to be high for half a clock period before the first databit is sampled. SPI_EN has to remain high for 1 clock period after the last databit is sampled.

One write action contains 16 databits:

- One control bit: First bit to be sent, indicates whether a read ('0') or write ('1') will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

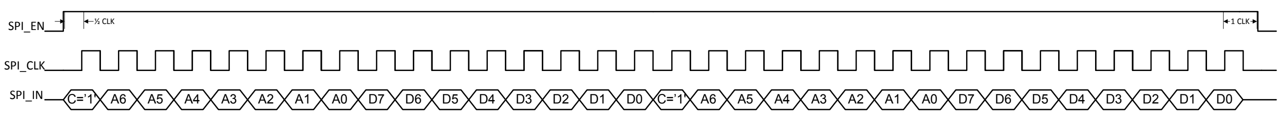


Figure 9: SPI write timing for 2 registersin burst

3.8.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

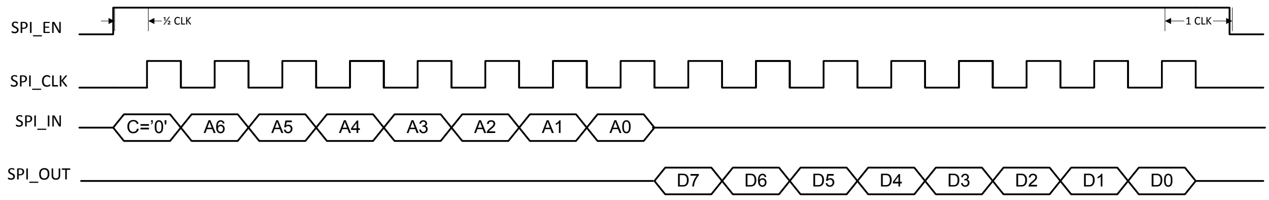


Figure 10: SPI read timing

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 126 and 127 should de read-out in burst mode (keep SPI_EN high)

3.9 REQUESTING A FRAME

After starting up the sensor (see section 3.5), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 70 and 71). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below.

3.9.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming the appropriate registers (address 42-44) of the CMV4000.After the high state of the FRAME_REQ pin is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one. See the diagram below for more details.

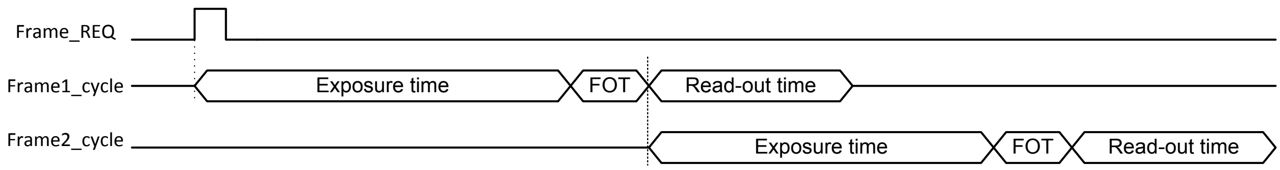


Figure 11: request for 2 frames in internal- exposure-time mode

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

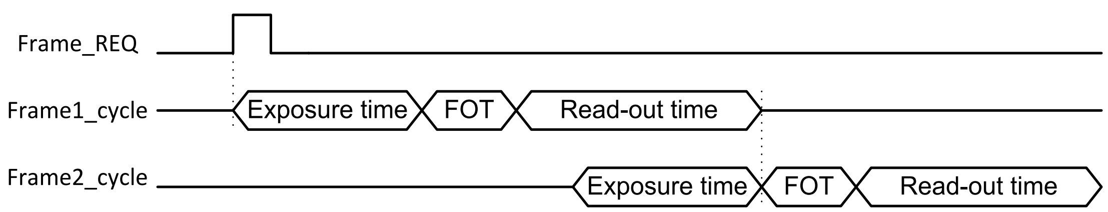


Figure 12: Request for 2 frames in internal exposure mode with exposure time < read-out time

3.9.2 EXTERNAL EXPOSURE TIME

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 41). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

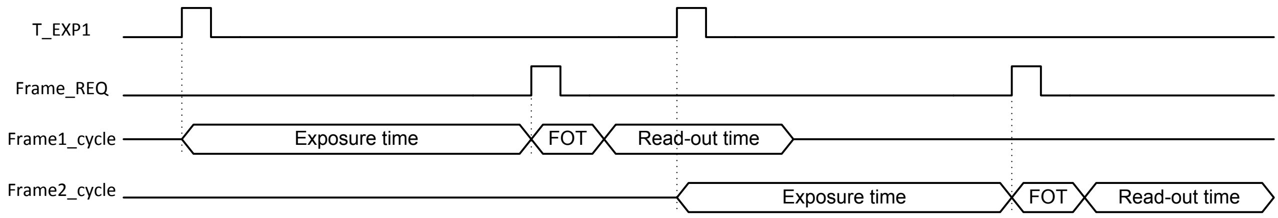


Figure 13: request for 2 frames using external-exposure-time mode

4 READING OUT THE SENSOR

4.1 LVDS DATA OUTPUTS

The CMV4000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the CMV4000 are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 16 data channels are used to transfer the 10-bit or 12-bit pixel data from the sensor to the receiver in the surrounding system.

The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480Mbps output data rate is used, the LVDS output clock will be 240MHz.

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 10-bit or 12-bit words that are transferred synchronous to the 16 data channels.

4.2 LOW-LEVEL PIXEL TIMING

The figures below show the timing for transfer of 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

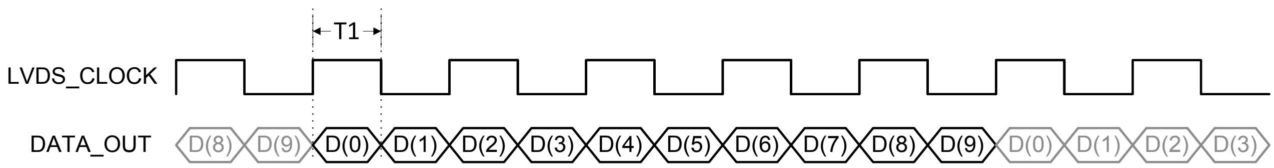


Figure 14: 10-bit pixel data on an LVDS channel

The time ‘T1’ in the diagram above is 1/10th of the period of the input clock (CLK_IN) of the CMV4000. When a frequency of 48MHz is used for CLK_IN (max in 10-bit mode) and 480MHz for LVDS_CLK_N/P, this results in a 240MHz LVDS_CLOCK.

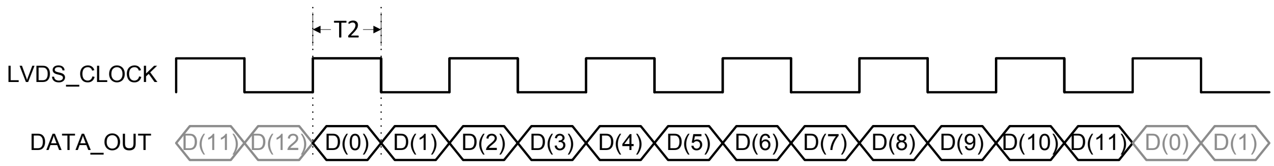


Figure 15: 12-bit pixel data on an LVDS channel

The time ‘T2’ in figure 14 is 1/12th of the period of the input clock (CLK_IN) of the CMV4000. When a frequency of 40MHz is used for CLK_IN (max in 12-bit mode) and 480MHz for LVDS_CLK_N/P, this results in a 240MHz LVDS_CLOCK.

4.3 READOUT TIMING

The readout of image data is grouped in bursts of 128 pixels per channel. Each pixel is either 10 or 12 bits of data (see section 4.2). One complete pixel period equals one period of the master clock input. For details on pixel remapping and pixel vs channel location please see section 4.4 of this document. An overhead time exists between two bursts of 128 pixels. This overhead time has the same length of one pixel read-out (i.e. the length of 10 or 12 bits at the selected data rate).

4.3.1 10 BIT MODE

In this section, the readout timing for the default 10 bit mode is explained. In this mode the maximum framerate of 180 fps can be reached.

4.3.1.1 16 OUTPUT CHANNELS

By default, all 16 data output channels are used to transmit the image data. This means that an entire row of image data is transferred in one slot of 128 pixel periods (16 x 128 = 2048). Next figure shows the timing for one LVDS channel.

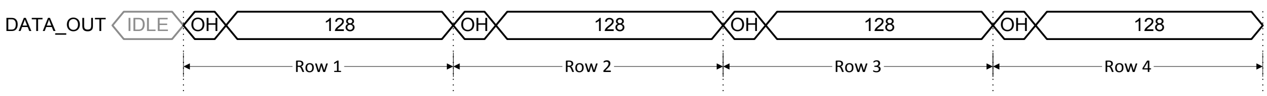


Figure 16: Output timing in default 16 channel mode

Only when 10 bit mode and 16 data outputs, running at 480Mbps, are used, the frame rate of 180fps can be achieved (default).

4.3.1.2 8 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 8 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (2*128) + (2*1) master clock periods. Next figure shows the timing for one LVDS channel.

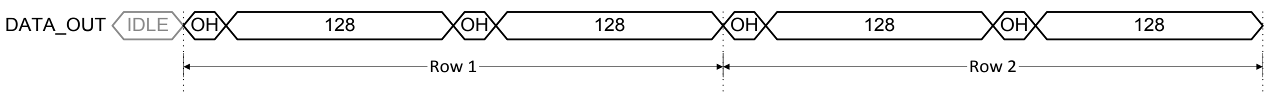


Figure 17: Output timing in 8 channel mode

In this 8 channel mode, the frame rate is reduced with factor of 2 compared to 16 channel mode.

4.3.1.3 4 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 4 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (4*128) + (4*1) master clock periods. Next figure shows the timing for one LVDS channel.

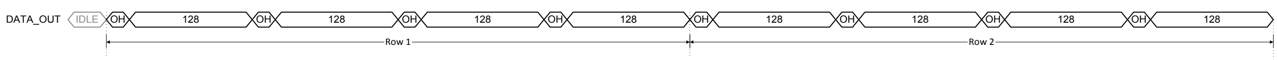


Figure 18: Output timing in of 4 channel mode

In this 4 channel mode, the frame rate is reduced with factor 4 compared to 16 channel mode.

4.3.1.4 2 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 2 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (8*128) + (8*1) master clock periods. Next figure shows the timing for one LVDS channel.

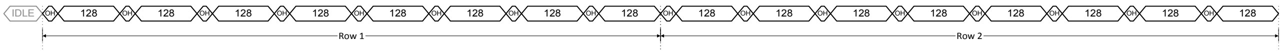


Figure 19: Output timing in 2 channel mode

In this 2 channel mode, the frame rate is reduced with factor of 8 compared to 16 channel mode.

4.3.2 12 BIT MODE

In 12 bit mode, the analog-to-digital conversion takes 4x longer to complete. This causes the framerate to drop to 70 fps when 480Mhz is used for LVDS_CLK_N/P. Due to this extra conversion time, the framerate in 16 channel mode is the same as in 8 and 4 channel mode.

4.3.2.1 16 OUTPUT CHANNELS

By default, all 16 data output channels are used to transmit the image data. This means that an entire row of image data is transferred in one slot of 128 pixel periods (16 x 128 = 2048). Next figure shows the timing for one LVDS channel.

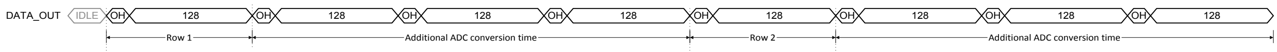


Figure 20: Output timing in default 16 channel mode

4.3.2.2 8 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 8 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (2*128) + (2*1) master clock periods. Next figure shows the timing for one LVDS channel.

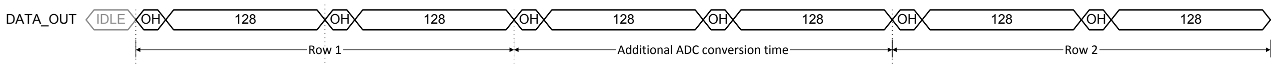


Figure 21: Output timing in 8 channel mode

4.3.2.3 4 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 4 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (4*128) + (4*1) master clock periods. Next figure shows the timing for one LVDS channel.

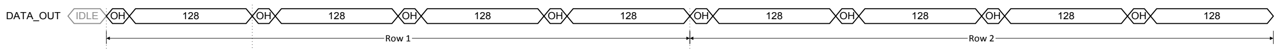


Figure 22: Output timing in of 4 channel mode

4.3.2.4 2 OUTPUT CHANNELS

The CMV4000 has the possibility to use only 2 LVDS output channels. This setting can be programmed in the register with address 72 (see section 5.7). In such multiplexed output mode, the readout of one row takes (8*128) + (8*1) master clock periods. Next figure shows the timing for one LVDS channel.

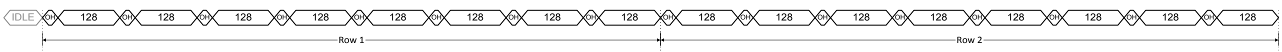


Figure 23: Output timing in 2 channel mode

In this 2 channel mode, the frame rate is reduced with factor of 2 compared to 16, 8 and 4 channel mode.

4.4 Pixel remapping

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

4.4.1 16 outputs

The figure below shows the location of the image pixels versus the output channel of the image sensor.

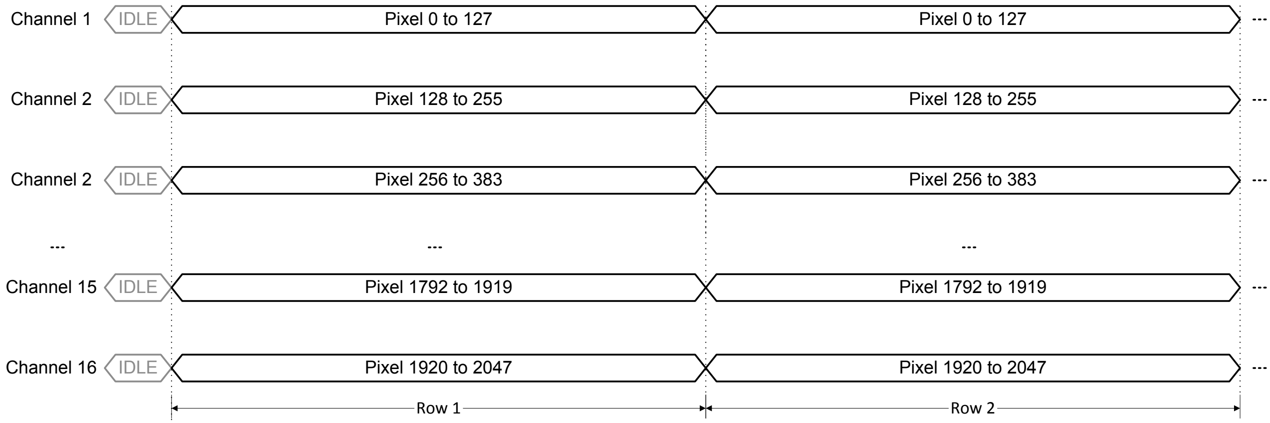


Figure 24: Pixel remapping for 16 output channels

16 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

4.4.2 8 outputs

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 8 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in two bursts. The time needed to read out one row is doubled compared to when 16 outputs are used. Channel 2, 4, 6…16 are not being used in this mode, so they can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

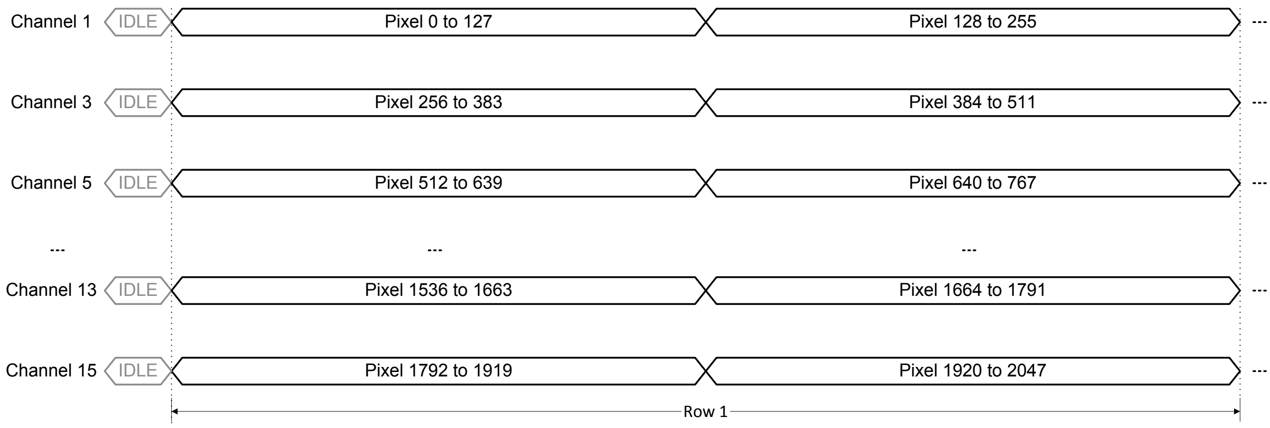


Figure 25: Pixel remapping for 8 output channels

4.4.3 4 OUTPUTS

When only 4 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 4 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in four bursts. The time needed to read out one row is 4x longer compared to when 16 outputs are used. Only channel 1, 5, 9 and 13 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out depends on the value in the corresponding register. By default there are 2048 rows being read out.

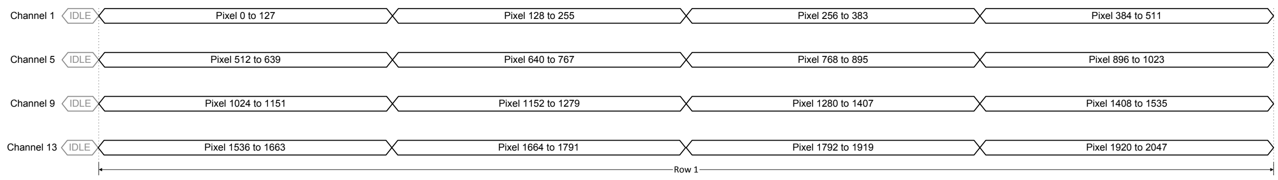


Figure 26: Pixel remapping for 4 output channels

4.4.4 2 OUTPUTS

When only 2 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 2 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 8 bursts. The time needed to read out one row is 8x longer compared to when 16 outputs are used. Only channel 1 and 9 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be readout depends on the value in the corresponding register. By default there are 2048 rows being read out.

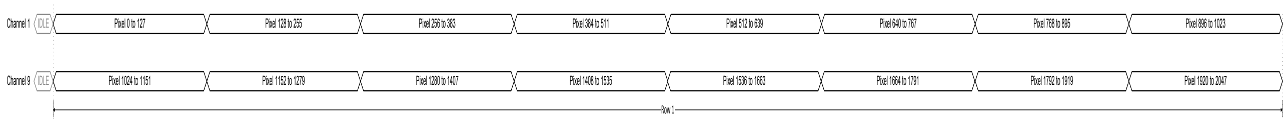


Figure 27: Pixel remapping for 2 output channels

4.5 CONTROL CHANNEL

The CMV4000 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 10-bit or 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the readout of a row
[2]	FVAL	Indicates the validity of the readout of a frame
[3]	SLOT	Indicates the overhead period before 128-pixel bursts (*)
[4]	ROW	Indicates the overhead period before the readout of a row (*)
[5]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[6]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[7]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[8]	‘0’	Constant zero
[9]	‘1’	Constant one
[10]	‘0’	Constant zero
[11]	‘0’	Constant zero

(*)Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

4.5.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the readout status.

Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the readout of a frame of 3 rows (default is 2048 rows). This example uses the default mode of 16 outputs in 10 bit mode.

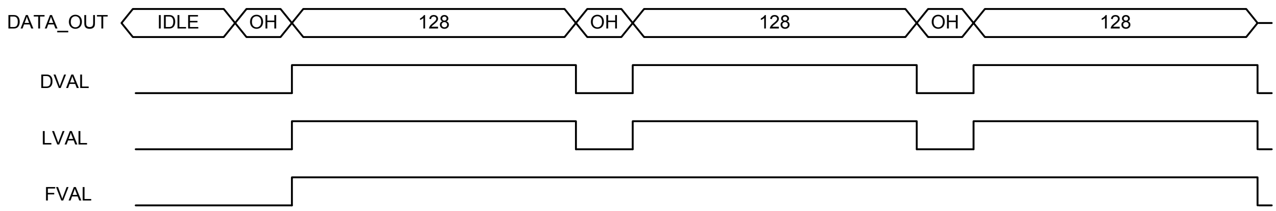


Figure 28: DVAL, LVAL and FVAL timing in 16 output mode

When only 8 outputs are used, the line read-out time is 2x longer. The control channel takes this into account and the timing in this mode looks like the diagram below. The timing extrapolates identically for 4 and 2 outputs.

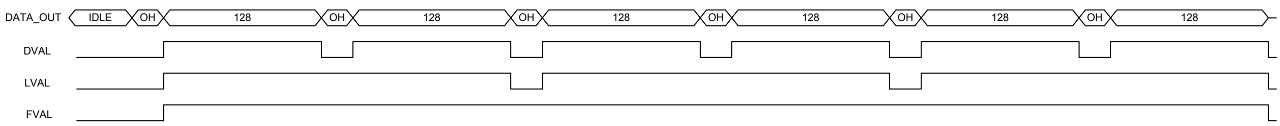


Figure 29: DVAL, LVAL and FVAL timing in 8 output mode

4.6 TRAINING DATA

To synchronize the receiving side with the LVDS outputs of the CMV4000, a known data pattern can be put on the output channels. This pattern can be used to “train” the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. Such a training pattern is put on all 16 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 128 pixels). The training pattern is a 10-bit or 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 78-79) that can be loaded through the SPI to change the contents of the 12-bit training pattern.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9].

The figure below shows the location of the training pattern (TP) on the data channels and control channels when the sensor is in idle mode and when a frame of 3 rows is read-out. The default mode of 16 outputs is selected.

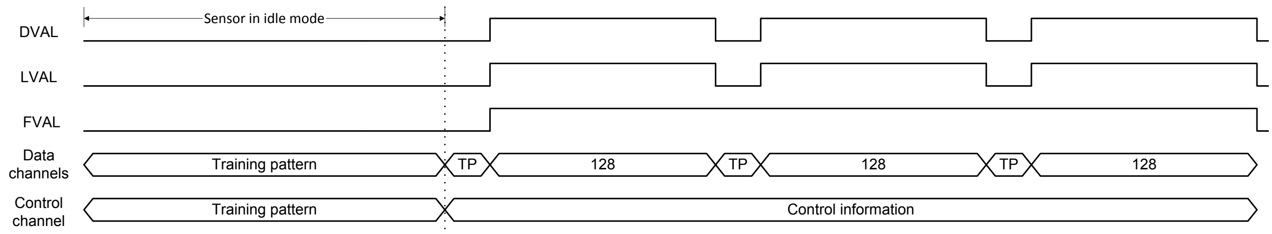


Figure 30: Training pattern location in the data and control channels.

5 IMAGE SENSOR PROGRAMMING

This section explains how the CMV4000 can be programmed using the on-board sequencer registers.

5.1 EXPOSURE MODES

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see section 3.8.2 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

The table below gives an overview of the registers involved in the exposure mode.

Exposure time settings			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_ext	41 bit[0]	0	0: Exposure time is defined by the value uploaded in the sequencer register (42-44) 1: Exposure time is defined by the pulses applied to the TEXP1 and FRAME_REQ pins.
Exp_time	42-44	2048	When the Exp_ext register is set to '0', the value in this register defines the exposure time according to the following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.

5.2 HIGH DYNAMIC RANGE MODES

The sensor has different ways to achieve high optical dynamic range in the grabbed image.

- Interleaved read-out: the odd and even rows have a different exposure time
- Piecewise linear response: pixels respond to light with a piecewise linear response curve.
- Multi-frame readout: Different frames are read-out with increasing exposure time

All the HDR modes mentioned above can be used in both the internal and external exposure time mode.

5.2.1 INTERLEAVED READ-OUT

In this HDR mode, the odd and even rows of the image sensors will have a different exposure time. This mode can be enabled by setting the register in the table below.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_dual	41 bit[1]	0	0: interleaved exposure mode disabled 1: interleaved exposure mode enabled

The surrounding system can combine the image of the odd rows with the image of the even rows which can result in a high dynamic range image. In such an image very bright and very dark objects are made visible without clipping. The table below gives an overview of the registers involved in the interleaved read-out when the internal exposure mode is selected.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	42-44	2048	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the even rows according following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the

			period of the master input clock.
Exp_time2	56-58	2048	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the odd rows according following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.

When the external exposure mode and interleaved read-out are selected, the different exposure times are achieved by using the T_EXP1 and T_EXP2 input pins. TEXP1 defines the exposure time for the even lines, while TEXP2 defines the exposure time for the odd lines. See the figure below for more details.

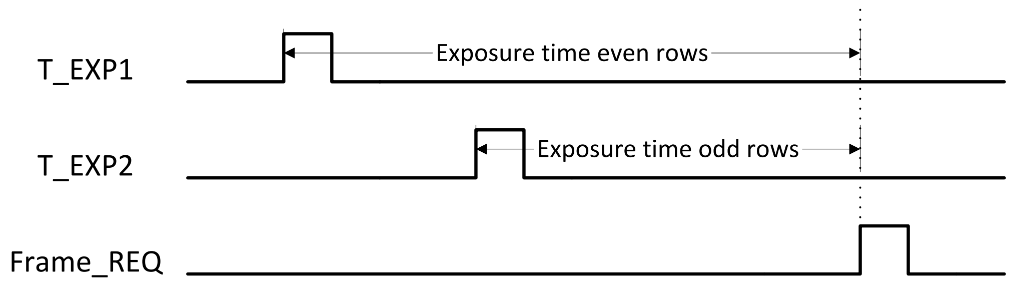


Figure 31: Interleaved read-out in external exposure mode

When a color sensor is used, the sequencer should be programmed to make sure it takes the Bayer pattern into account when doing interleaved read-out. This can be done by setting the appropriate register to '0'.

Color/mono			
Register name	**Register address**	**Default value**	**Description of the value**
Color	39	1	0: color sensor is used 1: monochrome sensor is used

5.2.2 PIECEWISE LINEAR RESPONSE

The CMV4000 has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve. More details can be found in the figure below.

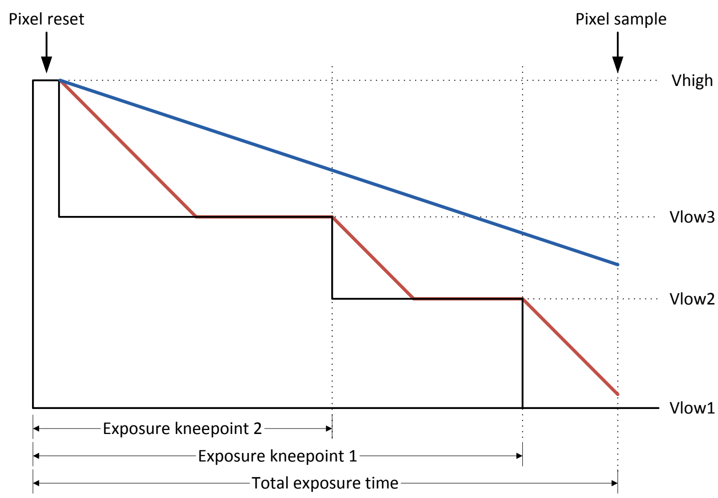


Figure 32: Piecewise linear response details

In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced and will have a normal response. The Vlow voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in the figure below can be achieved. The placement of the kneepoints in X is controlled by the Vlow programming, while the slope of the segments is controlled by the programmed exposure times.

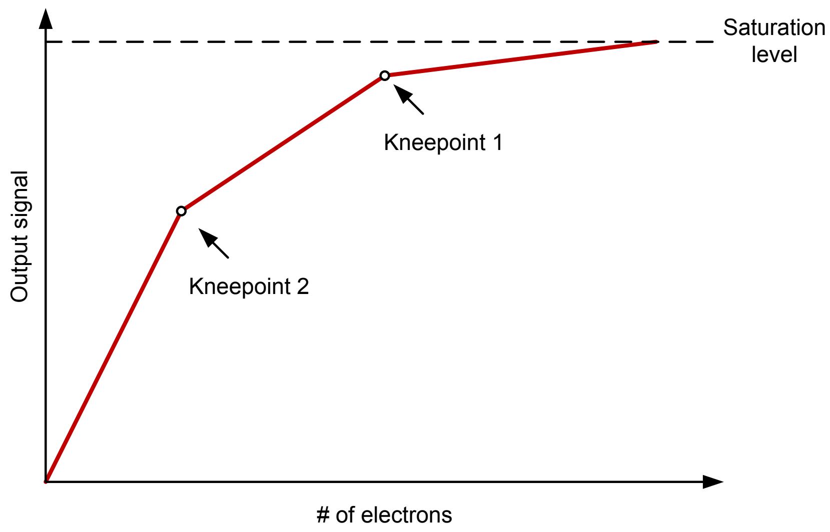


Figure 33: Piecewise linear response

5.2.2.1 PIECEWISE LINEAR RESPONSE WITH INTERNAL EXPOSURE MODE

The following registers need to be programmed when a piecewise linear response in internal exposure mode is desired.

HDR settings – multiple slope			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	42-44	2048	The value in this register defines the total exposure time according following formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.
Nr_slopes	54	1	The value in this register defines the number of slopes (min=1, max=3).
Exp_kp1	48-50	1	The value in this register defines the exposure time before kneepoint 1 is reached. Formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.
Exp_kp2	51-53	1	The value in this register defines the exposure time before kneepoint 2 is reached. Formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.
Vlow3	90	96	The value in this register defines the Vlow3 voltage (DAC setting).
Vlow2	89	96	The value in this register defines the Vlow2 voltage (DAC setting).

5.2.2.2 PIECEWISE LINEAR RESPONSE WITH EXTERNAL EXPOSURE MODE

When external exposure time is used and a piecewise linear response is desired, the following registers should be programmed.

HDR settings – multiple slope			
Register name	**Register address**	**Default value**	**Description of the value**
Nr_slopes	54	1	The value in this register defines the number of slopes (min=1, max=3).
Vlow3	90	96	The value in this register defines the Vlow3 voltage (DAC setting).
Vlow2	89	96	The value in this register defines the Vlow2 voltage (DAC setting).

The timing that needs to be applied in this external exposure mode looks like the one below.

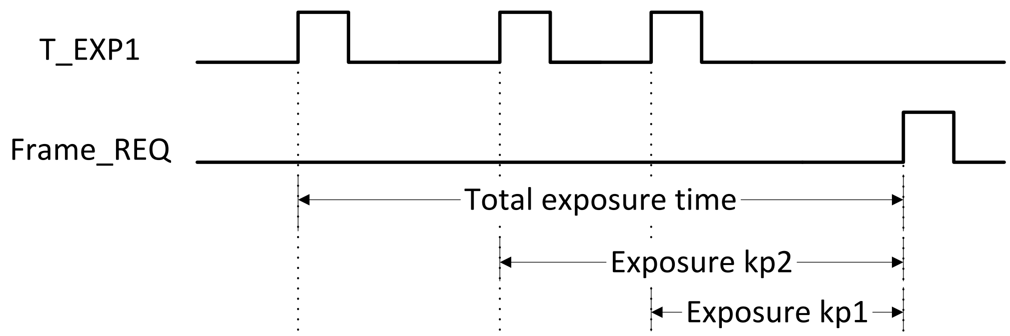


Figure 34: Piecewise linear response with external exposure time mode

Please note, that a combination of the piecewise linear response and interleaved read-out is not possible.

5.2.3 MULTI-FRAME READ-OUT

The sensor has the possibility to read-out multiple frames with increasing exposure time for each frame. The exposure time step and number of frames can be programmed using the appropriate registers. The frames grabbed in this mode, can be combined to create one high dynamic range image. This combination needs to be made by the receiving system.

The following registers should be used when this multi-frame read-out is selected. This mode only works with internal exposure time setting.

HDR settings – multi-frame read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	42-44	2048	The value in this register defines the exposure time of the first frame in the sequence. Formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.
Exp_step	45-47	0	The value in this register defines the step size for the increasing exposure times in multi-frame read-out. Formula: (0.65 x register73 x clk_per x 129) + (*Exp_time x 129 x clk_per)*, where clk_per is the period of the master input clock.
Exp_seq	55	1	The value in this register defines the number of frames to be read-out in multi-frame mode (min = 1, max = 255).

5.3 Windowing

To limit the amount of data or to increase the frame rate of the sensor, windowing in Y direction is possible. The number of lines and start address can be set by programming the appropriate registers. The CMV4000 has the possibility to read-out multiple (max=8) predefined subwindows in one read-out cycle. The default mode is to read-out one window with the full frame size (2048x2048).

5.3.1 Single window

When a single window is read out, the start address and size can be uploaded in the corresponding registers. The default start address is 0 and the default size is 2048 (full frame).

Windowing – single window			
Register name	**Register address**	**Default value**	**Description of the value**
start1	3-4	0	The value in this register defines the start address of the window in Y (min=0, max=2047)
Number_lines	1-2	2048	The value in this register defines the number of lines read-out by the sensor (min=1, max=2048)

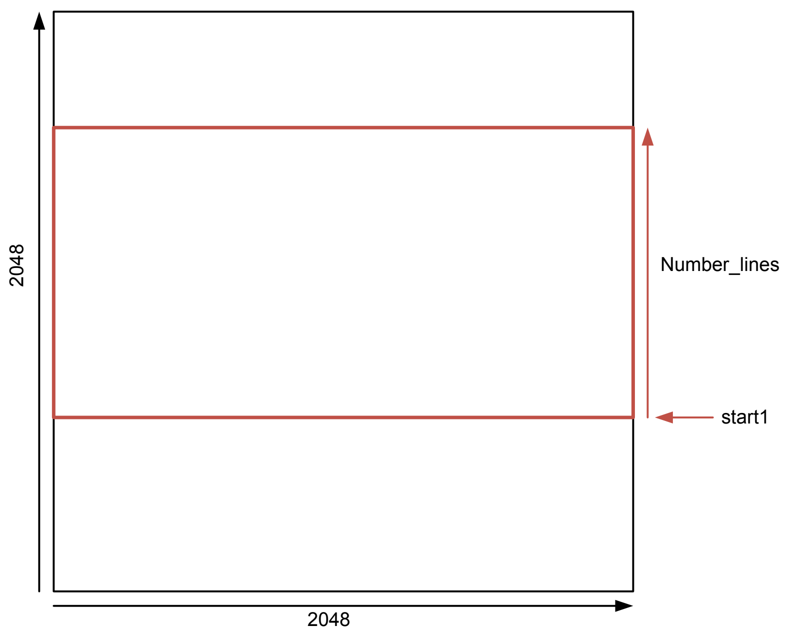


Figure 35: Single window settings

5.3.2 Multiple windows

The CMV4000 can read out a maximum of 8 different subwindows in one read-out cycle. The location and length of these subwindows must be programmed in the correct registers. The total number of lines to be read-out (sum of all windows) needs to be specified in the Number_lines register. The registers which need to be programmed for the multiple windows can be found in the table below.

Windowing – multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines	1-2	2048	The value in this register defines the total number of lines read-out by the sensor (min=1, max=2048)
start1	3-4	0	The value in this register defines the start address of the first window in Y (min=0, max=2047)
Number_lines1	19-20	0	The value in this register defines the number of lines of the

			first window (min=1, max=2048)
start2	5-6	0	The value in this register defines the start address of the second window in Y (min=0, max=2047)
Number_lines2	21-22	0	The value in this register defines the number of lines of the second window (min=1, max=2048)
start3	7-8	0	The value in this register defines the start address of the third window in Y (min=0, max=2047)
Number_lines3	23-24	0	The value in this register defines the number of lines of the third window (min=1, max=2048)
start4	9-10	0	The value in this register defines the start address of the fourth window in Y (min=0, max=2047)
Number_lines4	25-26	0	The value in this register defines the number of lines of the fourth window (min=1, max=2048)
start5	11-12	0	The value in this register defines the start address of the fifth window in Y (min=0, max=2047)
Number_lines5	27-28	0	The value in this register defines the number of lines of the fifth window (min=1, max=2048)
start6	13-14	0	The value in this register defines the start address of the sixth window in Y (min=0, max=2047)
Number_lines6	29-30	0	The value in this register defines the number of lines of the sixth window (min=1, max=2048)
start7	15-16	0	The value in this register defines the start address of the seventh window in Y (min=0, max=2047)
Number_lines7	31-32	0	The value in this register defines the number of lines of the seventh window (min=1, max=2048)
start8	17-18	0	The value in this register defines the start address of the eighth window in Y (min=0, max=2047)
Number_lines8	33-34	0	The value in this register defines the number of lines of the eighth window (min=1, max=2048)

Note: The default values will result in one window with 2048 lines to be read-out

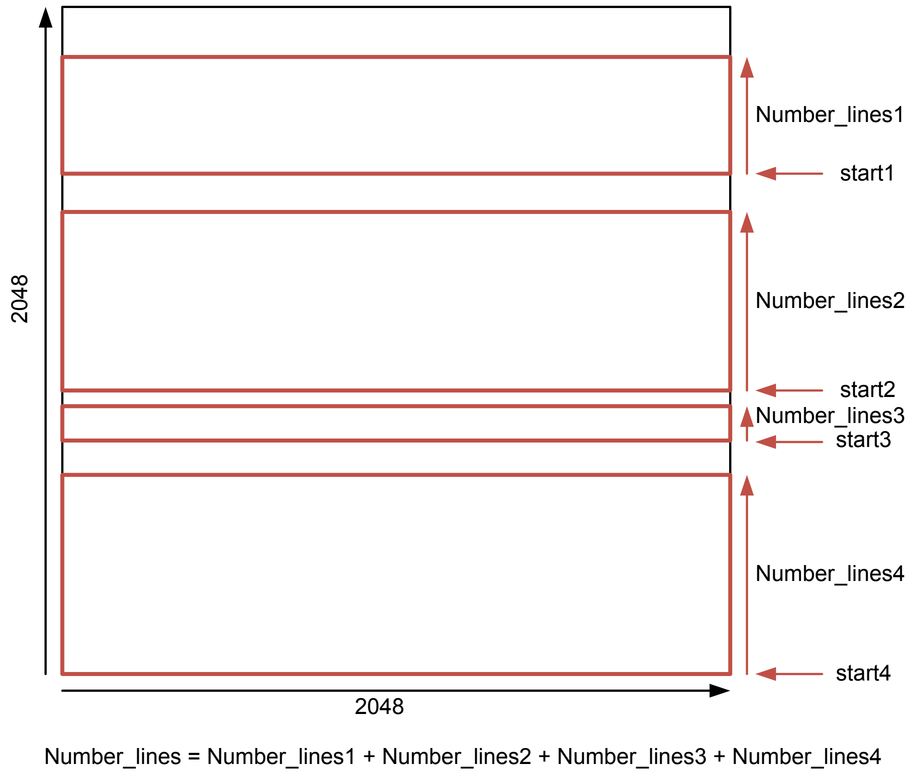


Figure 36: Example of 4 multiple frames read-out

5.4 IMAGE FLIPPING

The image coming out of the image sensor, can be flipped in X and/or Y direction. This means that if flipping is enabled in both directions the upper right pixel is read out first (instead of lower left). The following registers are involved in image flipping

Image flipping			
Register name	**Register address**	**Default value**	**Description of the value**
Image_flipping	40	0	0: No image flipping 1: Image flipping in X 2: Image flipping in Y 3: Image flipping in X and Y

5.5 IMAGE SUBSAMPLING

To maintain the same field of view but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers. These subsampling schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. The registers involved in subsampling are detailed below. A distinction is made between a simple and advanced mode (can be used for color devices). Subsampling can be enabled in every windowing mode.

5.5.1 SIMPLE SUBSAMPLING

Image subsampling - simple			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines	1-2	2048	The value in this register defines the total number of lines read-out by the sensor (min=1, max=2048)
Sub_s	35-36	0	Number of rows to skip (min=0, max=2046)
Sub_a	37-38	0	Identical to Sub_s

The figures below give two subsampling examples (skip 4x and skip 1x).

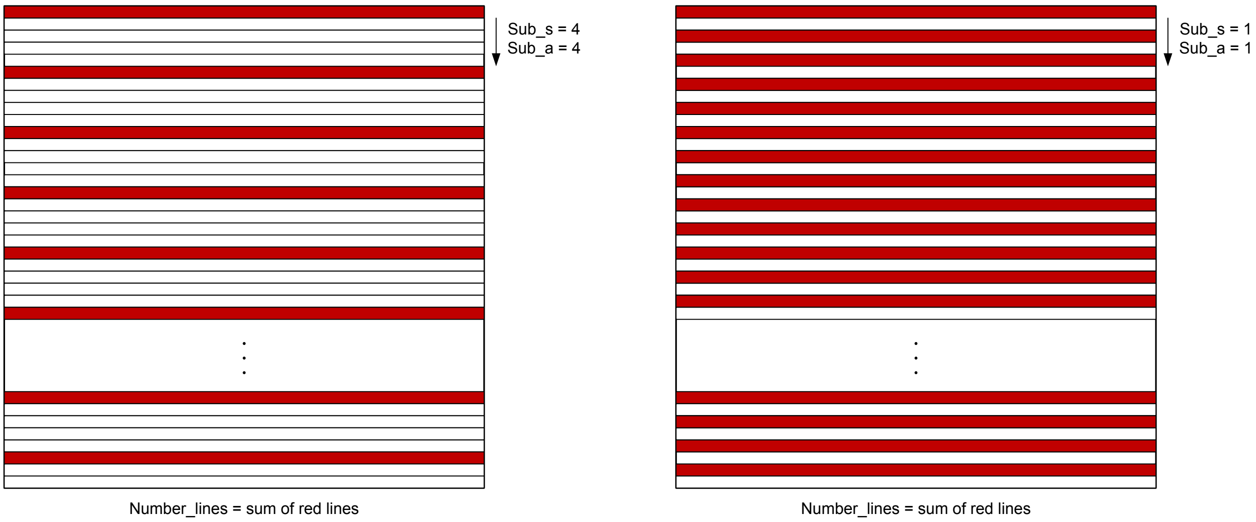


Figure 37: Subsampling examples (skip 4x and skip 1x)

5.5.2 ADVANCED SUBSAMPLING

When a color sensor is used, the subsampling scheme should take into account that a Bayer color filter is applied on the sensor. This Bayer pattern should be preserved when subsampling is used. This means that the number of rows to be skipped should always be a multiple of two. An advanced subsampling scheme can be programmed to achieve these requirements. Of course, this advanced subsampling scheme can also be programmed in a monochrome sensor. See the table of registers below for more details.

Image subsampling - advanced			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines	1-2	2048	The value in this register defines the total number of lines read-out by the sensor (min=1, max=2048)
Sub_s	35-36	0	Should be '0' at all times
Sub_a	37-38	0	Number of rows to skip, it should be an even number between (0 and 2046).

The figures below give two subsampling examples (skip 4x and skip 2x) in advanced mode.

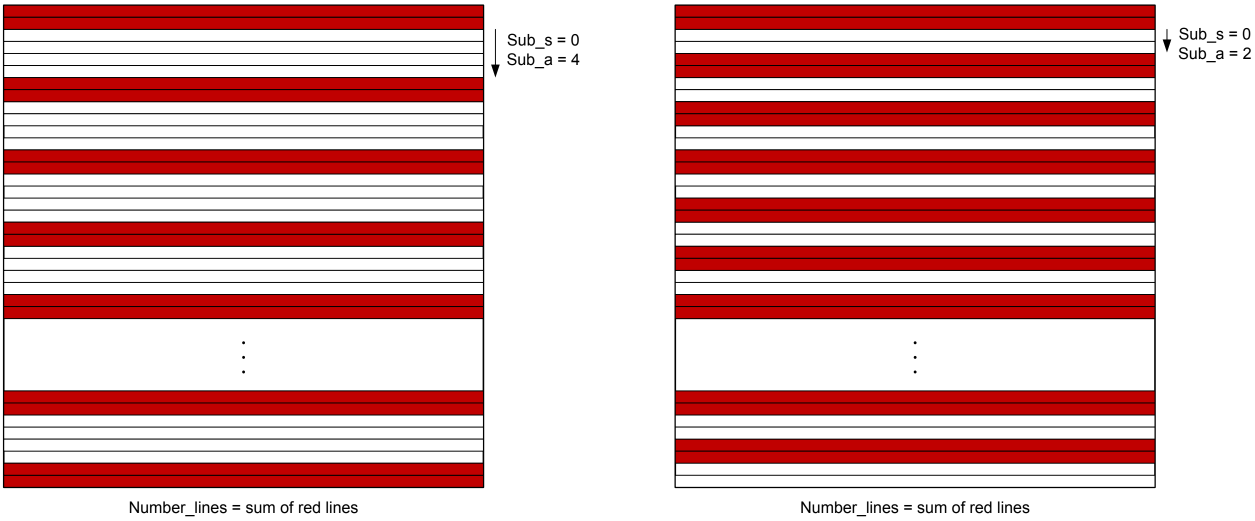


Figure 38: Subsampling examples in advanced mode (skip 4x and skip2x)

5.6 NUMBER OF FRAMES

When internal exposure mode is selected, the number of frames sent by the sensor after a frame request can be programmed in the corresponding sequencer register.

Number of frames			
Register name	**Register address**	**Default value**	**Description of the value**
Number_frames	70-71	1	The value in this register defines the number of frames grabbed and sent by the image sensor in internal exposure mode (min =1, max = 65548)

5.7 OUTPUT MODE

The number of LVDS channels can be selected by programming the appropriate sequencer register. The pixel remapping scheme and the read-out timing for each mode can be found in section 4 of this document.

Output mode			
Register name	**Register address**	**Default value**	**Description of the value**
Output_mode	72	0	0: 16 outputs 1: 8 outputs 2: 4 outputs 3: 2 outputs

5.8 Training pattern

As detailed in section 4.6, a training pattern is sent over the LVDS data channels whenever no valid image data is sent. This training pattern can be programmed using the sequencer register.

Training pattern			
Register name	**Register address**	**Default value**	**Description of the value**
Training_pattern	78-79	85	The 12 LSBs of this 16 bit word are sent in 12-bit mode. In 10 bit mode the 10 LSBs are sent.

5.9 10-bit or 12-bit mode

The CMV4000 has the possibility to send 12 bits or 10 bits per pixel. The end user can select the desired resolution by programming the corresponding sequencer register.

10-bit or 12-bit mode			
Register name	**Register address**	**Default value**	**Description of the value**
Bit_mode	111	1	0: 12 bits per pixel 1: 10 bits per pixel
ADC_Resolution	112	0	0: 10 bits per pixel 1: 11 bits per pixel 2: 12 bits per pixel

5.10 Data rate

During start-up or after a sequencer reset, the data rate can be changed if a lower speed than 480Mbps is desired. This can be done by applying a lower master input clock (CLK_IN) and high speed LVDS clock (LVDS_CLK_N/P) to the sensor. See section 3.4 for more details on the input clock. See section 3.6 for details on how the data rate can be changed. No registers should be changed when a data rate different from 480Mbps is used.

5.11 Power control

The power consumption of the CMV4000 can be regulated by disabling the LVDS data channels when they are not used (in 8, 4 or 2 outputs mode).

10-bit or 12-bit mode			
Register name	**Register address**	**Default value**	**Description of the value**
Channel_en	80-82	All '1'	Bit 0-15 enable/disable the data output channels Bit 16 enables/disables the clock channel Bit 17 enables/disables the control channel 0: disabled 1: enabled

5.12 Offset and gain

5.12.1 Offset

A digital offset can be applied to the output signal. This dark level offset can be programmed by setting the desired value in the sequencer register. Dark-level @ output = 70 + setting – 16383 (→ default dark-level = 10)

Offset			
Register name	**Register address**	**Default value**	**Description of the value**
Offset	100-101	16323	The value in this register defines the dark level offset applied to the output signal (min = 0, max = 16383)

5.12.2 Gain

An analog gain and ADC gain can be applied to the output signal. The analog gain is applied by a PGA in every column. The digital gain is applied by the ADC.

Gain			
Register name	**Register address**	**Default value**	**Description of the value**
PGA	102	0	0: x1 gain 1: x1.2 gain 2: x1.4 gain 3: x1.6 gain
ADC_gain	103	32	32

5.13 Recommended register settings

The following table gives an overview of the registers which have a required value which is different from their default start-up value. We strongly recommend to load these register settings after start-up and before grabbing an image.

Address	Name	Required Value
103	ADC_GAIN	44
84	I_col	4
85	I_col_prech	1
88	Vtf_l1	64
91	Vres_low	64
94	V_precharge	101
98	V_ramp1	109
99	V_ramp2	109
95	V_ref	106
117	Config1	1
115	Config2	1
82	Channel_en	7

5.13.1 Adjusting registers for optimal performance

Due to processing differences, the reponse and optical performance may differ slightly from sensor to sensor. To adjust this difference in response, the follwing registers should be tuned from sensor to sensor.

Address	Name	Required Value	Valid Range
103	ADC_GAIN	44	40-55
98	V_ramp1	109	102-115
99	V_ramp2	109	102-115

- ADC_gain: Due to processing differences, the AFE (analog front end) of the sensor may differ from device to device. This means that the total gain value (bit/e) of the sensor may differ from sensor to sensor. The ADC_gain register can be used to change the gain value (bit/e) from every sensor to match a desired value.
- V_ramp1/2: When column non-unifromities are observed with the default and recommended (section 5.13) register settings an adjustement of the V_ramp1/2 registers is advised. These registers set the starting voltage of the ramp used by the column ramp ADC. Adjusting this value will result in better column CDS (correlated double sampling) which will remove the column FPN from the image. Both values always should have the same value.

6 REGISTER OVERVIEW

The table below gives an overview of all the sensor registers. The registers with the remark “Do not change” should not be changed unless advised in section 5.13.

Address	Default	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Remark/Required value
0	0									Do not change
1	0	Number_lines[7:0]								
2	8	Number lines [15:8]								
3	0	Start1[7:0]								
4	0	Start1[15:8]								
5	0	Start2[7:0]								
6	0	Start2[15:8]								
7	0	Start3[7:0]								
8	0	Start3[15:8]								
9	0	Start4[7:0]								
10	0	Start4[15:8]								
11	0	Start5[7:0]								
12	0	Start5[15:8]								
13	0	Start6[7:0]								
14	0	Start6[15:8]								
15	0	Start7[7:0]								
16	0	Start7[15:8]								
17	0	Start8[7:0]								
18	0	Start8[15:8]								
19	0	Number_lines1[7:0]								
20	0	Number_lines1[15:8]								
21	0	Number_lines2[7:0]								
22	0	Number_lines2[15:8]								
23	0	Number_lines3[7:0]								
24	0	Number_lines3[15:8]								
25	0	Number_lines4[7:0]								
26	0	Number_lines4[15:8]								
27	0	Number_lines5[7:0]								
28	0	Number_lines5[15:8]								
29	0	Number_lines6[7:0]								
30	0	Number_lines6[15:8]								
31	0	Number_lines7[7:0]								
32	0	Number_lines7[15:8]								
33	0	Number_lines8[7:0]								
34	0	Number_lines8[15:8]								
35	0	Sub_s[7:0]								
36	0	Sub_s[15:8]								
37	0	Sub_a[7:0]								
38	0	Sub_a[15:8]								
39	1								Color	
40	0							Image_flipping[1:0]		
41	0							Exp_dual	Exp_ext	
42	0	Exp_time[7:0]								
43	8	Exp_time[15:8]								
44	0	Exp_time[23:16]								
45	0	Exp_step[7:0]								

46	0	Exp_step[15:8]	
47	0	Exp_step[23:16]	
48	1	Exp_kp1[7:0]	
49	0	Exp_kp1[15:8]	
50	0	Exp_kp1[23:16]	
51	1	Exp_kp2[7:0]	
52	0	Exp_kp2[15:8]	
53	0	Exp_kp2[23:16]	
54	1	Nr_slopes[1:0]	
55	1	Exp_seq[7:0]	
56	0	Exp_time2[7:0]	
57	8	Exp_time2[15:8]	
58	0	Exp_time2[23:16]	
59	0	Exp_step2[7:0]	
60	0	Exp_step2[15:8]	
61	0	Exp_step2[23:16]	
62	1		Do not change
63	0		Do not change
64	0		Do not change
65	1		Do not change
66	0		Do not change
67	0		Do not change
68	1	Nr_slopes2[1:0]	
69	1	Exp2_seq[7:0]	
70	1	Number_frames [7:0]	
71	0	Number_frames[15:8]	
72	0	Output_mode[1:0]	
73	10		Do not change
74	8		Do not change
75	8		Do not change
76	8		Do not change
77	0		Do not change
78	85	Training_pattern[7:0]	
79	0	Training pattern [11:8]	
80	255	Channel_en[7:0]	
81	255	Channel_en[15:8]	
82	3	Channel_en[17:16]	Set to 7
83	8		Do not change
84	8		Set to 4
85	8		Set to 1
86	8		Do not change
87	8		Do not change
88	96		Set to 64
89	96	Vlow2[7:0]	
90	96	Vlow3[7:0]	
91	96		Set to 64
92	96		Do not change
93	96		Do not change
94	96		Set to 101
95	96		Set to 106
96	96		Do not change
97	96		Do not change
98	96		Set to 109 (can differ from sensor to sensor)

99	96		Set to 109 (can differ from sensor to sensor)
100	195	Offset[7:0]	
101	63	Offset[13:8]	
102	0	PGA[1:0]	
103	32	ADC_gain[7:0]	Set to 44 (can differ from sensor to sensor
104	8		Do not change
105	8		Do not change
106	8		Do not change
107	8		Do not change
108	0		Do not change
109	1		Do not change
110	0		Do not change
111	1	Bit_mode[0]	
112	0	ADC_resolution[1:0]	
113	1		Do not change
114	0		Do not change
115	0		Set to 1
116	32		Do not change
117	8		Set to 1
118	0		Do not change
119	0		Do not change
120	0		Do not change
121	0		Do not change
122	0		Do not change
123	0		Do not change
124	0		Do not change
125	32		Do not change
126	0	Temp[7:0]	
127	0	Temp[15:8]	

Note: The default value of the “do not change” registers should not be overwritten unless recommended in section 5.13.

7 MECHANICAL SPECIFICATIONS

7.1 PACKAGE DRAWING

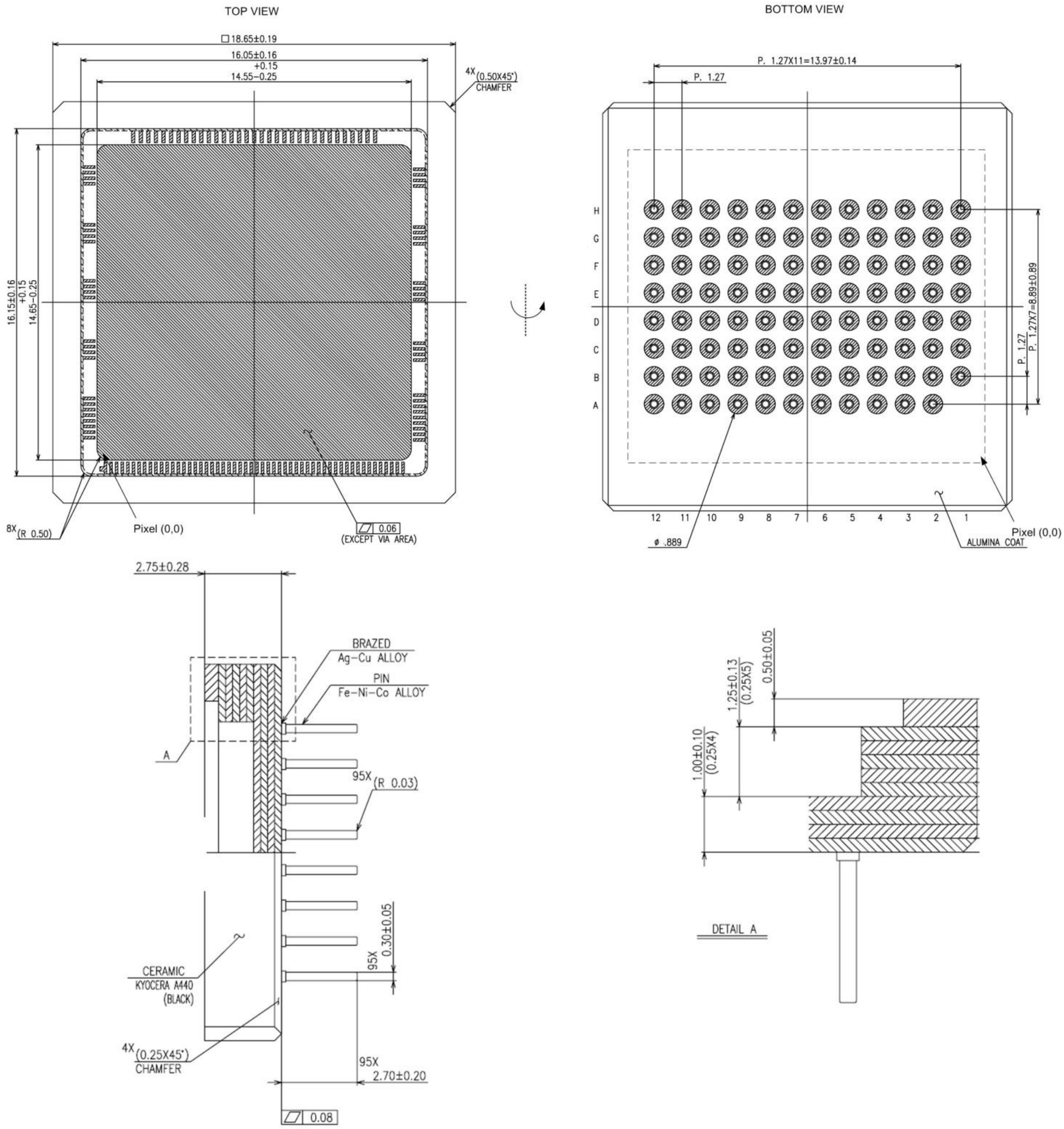


Figure 39: Package drawing of the CMV4000. All distances in mm.

7.2 Assembly drawing

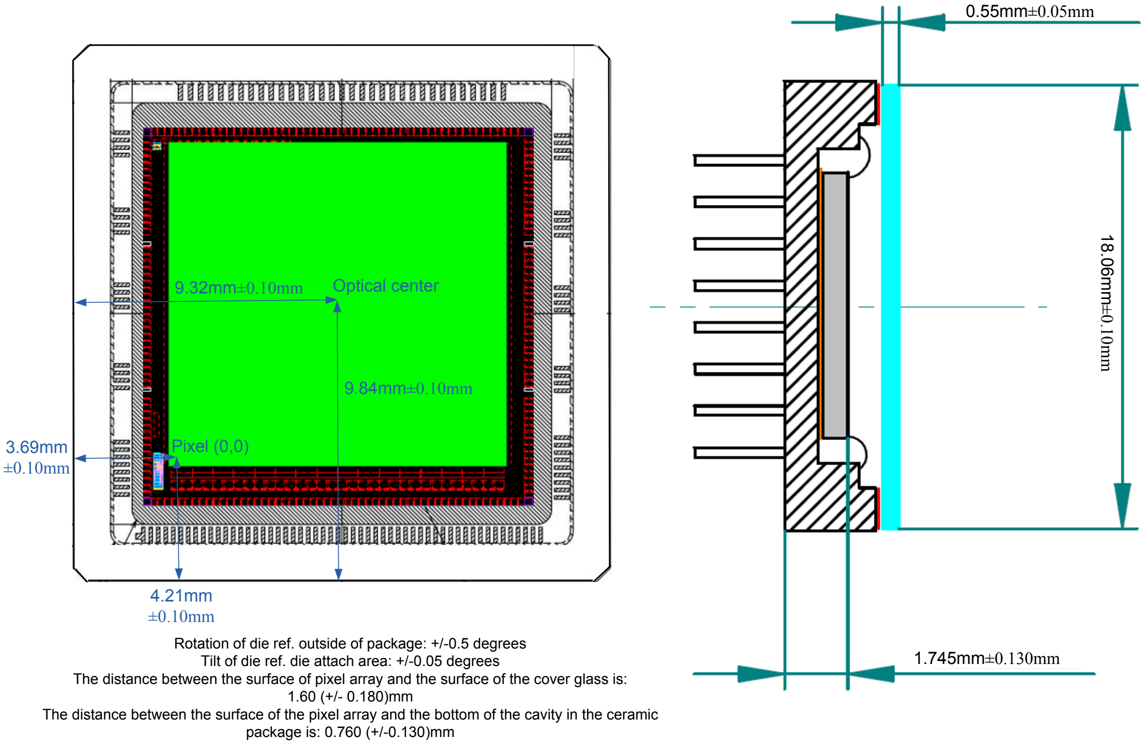


Figure 40: Assembly drawing of CMV4000.

7.3 Cover glass

The cover glass of the CMV4000 is plain D263 glass with a transmittance as shown in figure 37. Refraction index of the glass is 1.52. Scratch, bubbles and digs shall be less than or equal to 0.02 mm

When a color sensor is used an IR-cutoff filter should be placed in the optical path of the sensor.

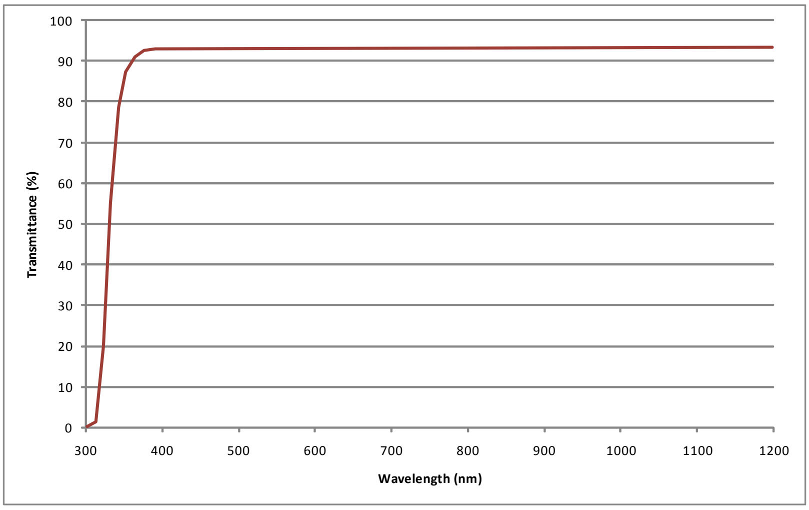


Figure 41: Transmittance curve of D263 cover glass

7.4 COLOR FILTERS

When a color version of the CMV4000 is used, the color filters are applied in a Bayer pattern. The color version of the CMV4000 always has microlenses. The typical spectral response of the CMV with color filters and D263 cover glass can be found below. The use of an IR cut-off filter in the optical path of the CMV4000 image sensor is necessary to obtain good color separation when using light with an NIR component.

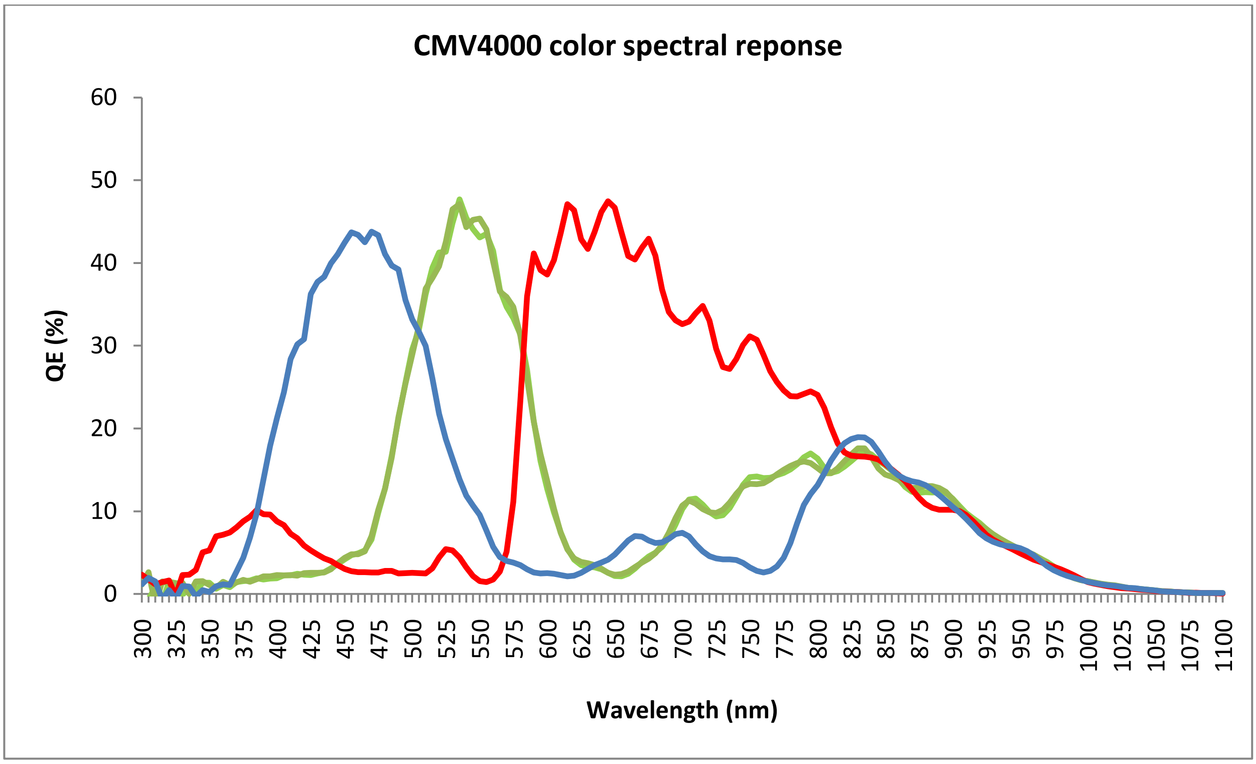


Figure 42: Typical spectral reponse of CMV4000 with RGB color filters and D263 cover glass

8 SPECTRAL RESPONSE

8.1 5µM EPI DEVICES

The typical spectral response of a monochrome CMV4000 with microlenses, with and without glass can be found below.

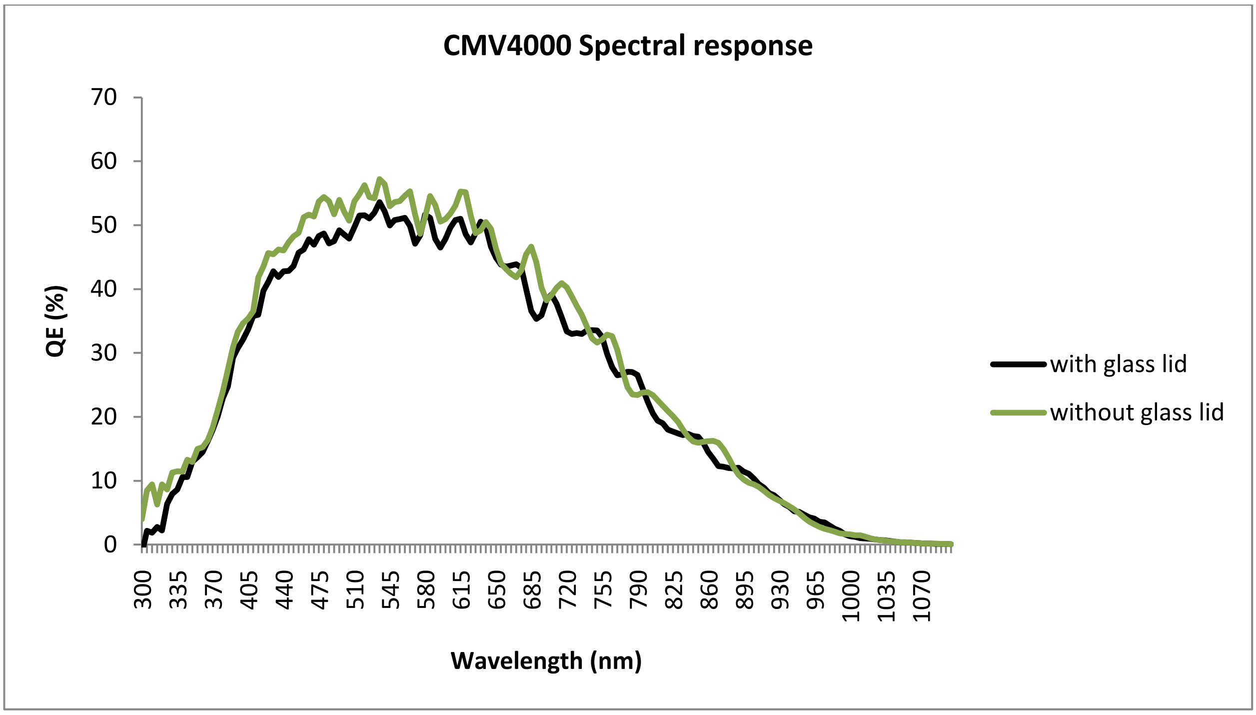


Figure 43: typical spectral response of the CMV4000

8.2 12µM EPI DEVICES

A variation from the standard CMV2000 image sensors is processed on 12 µm epi (E12) Si wafers. The thicker epi-layer wafer starting material increases significantly the QE for wavelengths above 600 nm. Around 900 nm the QE is about doubled and increases from 8% to 16%.

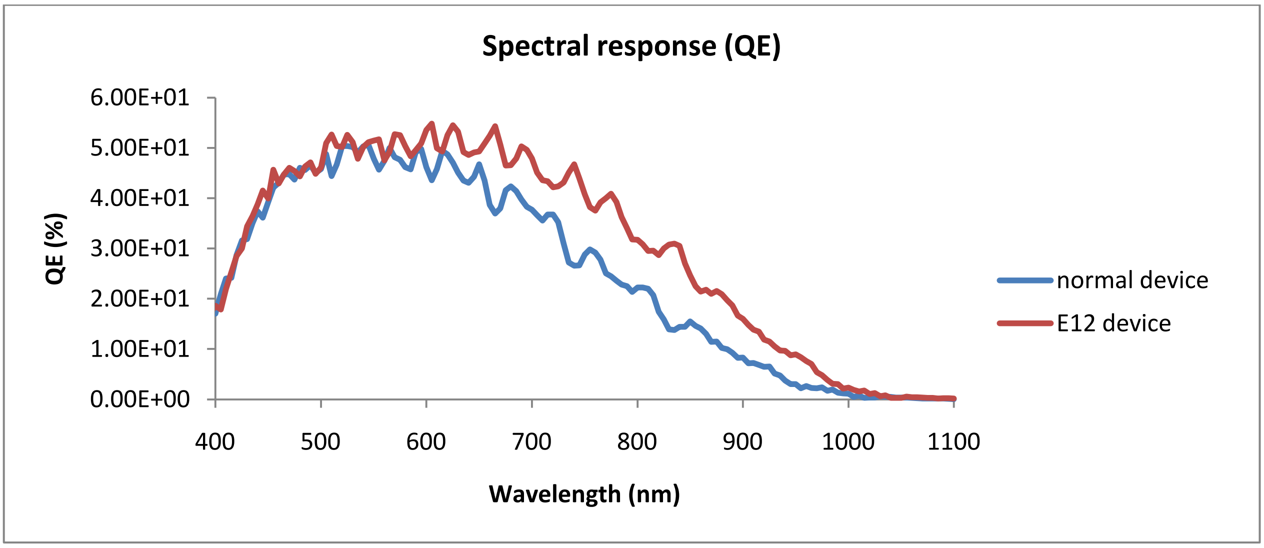


Figure 44: Response of E12 devices vs normal devices

9 PIN LIST

The pin list of the CMV4000 can be found below

Pin number	Pin name	Description	Type
A2	OUT2_N	LVDS negative data output channel 2	LVDS output
A3	OUT2_P	LVDS positive data output channel 2	LVDS output
A4	OUT5_N	LVDS negative data output channel 5	LVDS output
A5	OUT5_P	LVDS positive data output channel 5	LVDS output
A6	GND	Ground pin	Ground
A7	VDD20	2.0V supply	Supply
A8	OUT12_N	LVDS negative data output channel 12	LVDS output
A9	OUT12_P	LVDS positive data output channel 12	LVDS output
A10	OUT15_N	LVDS negative data output channel 15	LVDS output
A11	OUT15_P	LVDS positive data output channel 15	LVDS output
A12	GND	Ground pin	Ground
B1	OUTCTR_N	LVDS negative control output channel	LVDS output
B2	OUTCTR_P	LVDS positive control output channel	LVDS output
B3	OUT4_N	LVDS negative data output channel 4	LVDS output
B4	OUT4_P	LVDS positive data output channel 4	LVDS output
B5	OUT7_N	LVDS negative data output channel 7	LVDS output
B6	OUT7_P	LVDS positive data output channel 7	LVDS output
B7	OUT10_N	LVDS negative data output channel 10	LVDS output
B8	OUT10_P	LVDS positive data output channel 10	LVDS output
B9	OUT13_N	LVDS negative data output channel 13	LVDS output
B10	OUT13_P	LVDS positive data output channel 13	LVDS output
B11	OUTCLK_N	LVDS negative clock output channel	LVDS output
B12	OUTCLK_P	LVDS positive clock output channel	LVDS output
C1	GND	Ground pin	Ground
C2	OUT1_N	LVDS negative data output channel 1	LVDS output
C3	OUT1_P	LVDS positive data output channel 1	LVDS output
C4	OUT6_N	LVDS negative data output channel 6	LVDS output
C5	OUT6_P	LVDS positive data output channel 6	LVDS output
C6	GND	Ground pin	Ground
C7	VDD20	2.0V supply	Supply
C8	OUT11_N	LVDS negative data output channel 11	LVDS output
C9	OUT11_P	LVDS positive data output channel 11	LVDS output
C10	OUT16_N	LVDS negative data output channel 16	LVDS output
C11	OUT16_P	LVDS positive data output channel 16	LVDS output
C12	GND	Ground pin	Ground
D1	LVDS_CLK_P	LVDS input clock P	LVDS input
D2	LVDS_CLK_N	LVDS input clock N	LVDS input
D3	OUT3_N	LVDS negative data output channel 3	LVDS output
D4	OUT3_P	LVDS positive data output channel 3	LVDS output
D5	OUT8_N	LVDS negative data output channel 8	LVDS output
D6	OUT8_P	LVDS positive data output channel 8	LVDS output
D7	OUT9_N	LVDS negative data output channel 9	LVDS output
D8	OUT9_P	LVDS positive data output channel 9	LVDS output
D9	OUT14_N	LVDS negative data output channel 14	LVDS output
D10	OUT14_P	LVDS positive data output channel 14	LVDS output
D11	VREF	Ref for column amps (decouple with 100nF to ground)	Bias
D12	REF_ADC	Ref for ADC testing (decouple with 100nF to ground)	Bias
E1	CLK_IN	Master input clock	Digital input
E2	VDD33	3.3V supply	Supply
E3	GND	Ground pin	Ground

E4	VDD20	2.0V supply	Supply
E5	GND	Ground pin	Ground
E6	VDDpix	3.0V supply	Supply
E7	VDD20	2.0V supply	Supply
E8	VDD20	2.0V supply	Supply
E9	GND	Ground pin	Ground
E10	SG_ADC	Sig for ADC testing (decouple with 100nF to ground)	Bias
E11	Vramp1	Start voltage first ramp (decouple with 100nF to ground)	Bias
E12	Vramp2	Start voltage second ramp (decouple with 100nF to ground)	Bias
F1	GND	Ground pin	Ground
F2	FRAME_REQ	Frame request pin	Digital input
F3	SPI_IN	SPI data input pin	Digital input
F4	SPI_OUT	SPI data output pin	Digital output
F5	CMD_P_INV	decouple with 100nF to VDD33	bias
F6	Vpch_H	Precharge high voltage (decouple with 100nF to ground)	bias
F7	Vres_H	3.3V supply	Supply
F8	Vtf_l2	Transfer low voltage 2 (decouple with 100nF to ground)	Bias
F9	Col_load	decouple with 100nF to ground	Bias
F10	ramp	decouple with 100nF to VDD33	Bias
F11	DIO1	Diode 1 for test (not connected)	Test
F12	GND	Ground pin	Ground
G1	VDDpix	3.0V supply	Supply
G2	T_dig2	Test pin for digital signals	Digital output
G3	T_Exp2	Input pin for external exposure mode	Digital input
G4	SPI_EN	SPI enable input pin	Digital input
G5	CMD_P	decouple with 100nF to VDD33	bias
G6	CMD_N	decouple with 100nF to ground	bias
G7	Tana	Test pin for analog signals	Analog output
G8	Vtf_l1	Transfer low voltage 1 (connect to ground)	Bias
G9	Col_amp	decouple with 100nF to ground	Bias
G10	ADC	decouple with 100nF to VDD33	Bias
G11	Vbgap	decouple with 100nF to ground	Bias
G12	VDDpix	3.0V supply	Supply
H1	VDD33	3.3V supply	Supply
H2	T_dig1	Test pin for digital signals	Digital output
H3	T_Exp1	Input pin for external exposure mode	Digital input
H4	SPI_CLK	SPI clock input pin	Digital input
H5	SYS_RES_N	Input pin for sequencer reset	Digital input
H6	VDD33	3.3V supply	Supply
H7	GND	Ground pin	Ground
H8	Vres_L	Res low voltage (decouple with 100nF to ground)	Bias
H9	Vtf_l3	Transfer low voltage 3 (decouple with 100nF to ground)	bias
H10	COL_PC	decouple with 100nF to ground	Bias
H11	LVDS	decouple with 100nF to ground	Bias
H12	DIO2	Diode 2 for test (not connected)	Test

10 SPECIFICATION OVERVIEW

Specification	Value	Comment
Effective pixels	2048 x 2048	
Pixel pitch	5.5 x 5.5 μm^2	
Optical format	1”	
Full well charge	13.5 Ke-	Pinned photodiode pixel.
Conversion gain	0.075 LSB/e-	10 bit mode, unity gain
Sensitivity	4.64 V/lux.s 0.22 A/W	With microlenses
Temporal noise (analog domain)	13 e-	Pipelined global shutter (GS) with correlated double sampling (CDS)
Dynamic range	60 dB	
Pixel type	Global shutter pixel	Allows fixed pattern noise correction and reset (kTC) noise canceling through correlated double sampling.
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image.
Parasitic light sensitivity - Shutter efficiency	<1/50 000 >99.998%	
Color filters	Optional	RGB Bayer pattern
Micro lenses	Yes	
Fill Factor	42%	w/o micro lens
QE * FF	50%	@ 550 nm with micro lenses.
Dark current signal	125 e/s	@ 25C die temperature
DSNU	3 LSB/s	10 bit mode
Fixed pattern noise	<1 LSB RMS	<0.1% of full swing, 10 bit mode
PRNU	< 1% RMS of signal	
LVDS Output channel	16	Each data output running @ 480 Mbit/s. 8, 4 and 2 outputs selectable at reduced frame rate
Frame rate	180 frames/s	Using a 10bit/pixel and 480 Mbit/s LVDS. Higher frame rate possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	4 analog gain settings
Programmable Registers	Sensor parameters	Window coordinates, Timing parameters, Gain & offset, Exposure time, flipped readout in x and y direction …
Supported HDR modes	Multi-frame readout with different exposure time Interleaved integration times Piecewise linear	Successive frames are read out with increasing exposure times. The final image is a combination (externally) of these frames. Interleaved exposure times for different rows: Odd rows (double rows for color) have a different exposure compared to even rows (double rows for color). Final image is a combination of the two (through interpolation).

	response	Response curve with two kneepoints.
ADC	10 bit/12bit	Column ADC
Interface	LVDS	Serial output data + synchronization signals
I/O logic levels	LVDS = 1.8V Logic levels = 3.3V	
Supply voltages	2.0 & 3.3 V	3.3V for the pixel array and analog circuits 2.0V for digital circuits and the LVDS drivers
Clock inputs	CLK_IN LVDS_CLK_N/P	Between 5 and 48MHz Between 50 and 480MHz, LVDS
Power	600 mW	
Package	Ceramic package	Custom ceramic µPGA (95 pins)
Operating range	-30C to +70C	Dark current and noise performance will degrade at higher temperature
Cover glass	D263	Plain glass, no IR cut-off filter on color devices

11 ORDERING INFO

Part Number	Epi Thickness	Chroma	Microlens	Package	Glass
CMV4000-2E5M1PP	5 µm	mono	yes	ceramic 95p µPGA	plain
CMV4000-2E5C1PP	5 µm	RGB Bayer	yes	ceramic 95p µPGA	plain
CMV4000-E12M1PP	12µm	mono	yes	ceramic 95p µPGA	plain

On request the package and cover glass can be customized. For options, pricing and delivery time please contact info@cmosis.com

12 HANDLING AND SOLDERING PROCEDURE

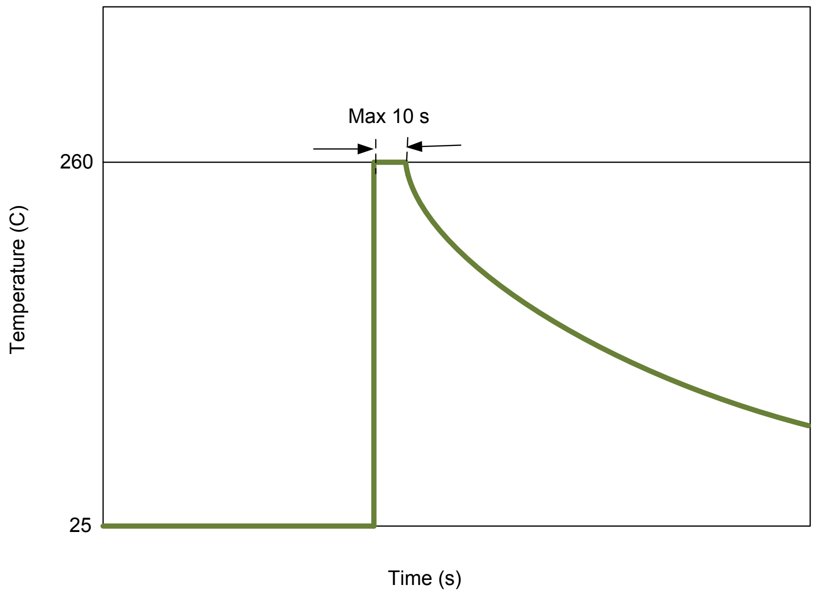
12.1 SOLDERING

12.1.1 MANUAL SOLDERING

Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350ºC with 270°C maximum pin temperature, 2 seconds maximum duration per pin. Avoid global heating of the ceramic package during soldering. Failure to do so may alter device performance and reliability.

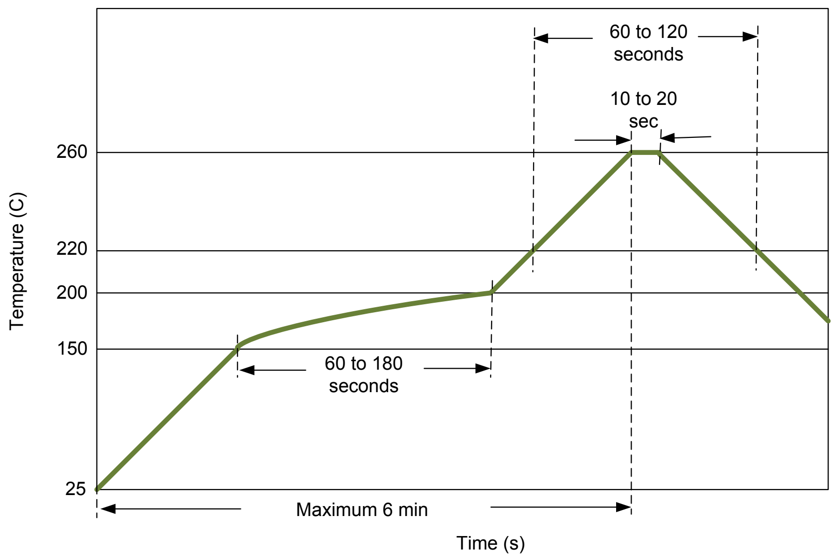
12.1.2 WAVE SOLDERING

Wave soldering is possible but not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. See the figure below for the wave soldering profile.



12.1.3 REFLOW SOLDERING

The figure below shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.



12.1.4 Soldering Recommendations

Image sensors with filter arrays (CFA) and micro-lens are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. Best solution will be flow soldering or manual soldering of a socket (through hole or BGA) and plug in the sensor at latest stage of the assembly/test process. The BGA solution allows more flexibility for the routing of the camera PCB.

12.2 Handling image sensors

12.2.1 ESD

The following are the recommended minimum ESD requirements when handling image sensors.

1. Ground workspace (tables, floors…)
2. Ground handling personnel (wrist straps, special footwear…)
3. Minimize static charging (control humidity, use ionized air, wear gloves…)

12.2.2 Glass cleaning

When cleaning of the cover glass is needed we recommend the following two methods.

1. Blowing off the particles with ionized nitrogen
2. Wipe clean using IPA (isopropyl alcohol) and ESD protective wipes.

12.2.3 Image sensor storing

Image sensors should be stored under the following conditions

1. Dust free
2. Temperature 20°C to 40°C
3. Humidity between 30% and 60%.
4. Avoid radiation, electromagnetic fields, ESD, mechanical stress

13 Additional Information

For any additional question related to the operation and specification of the CMV4000 imagers or feedback with respect to the present data sheet please contact techsupport@cmosis.com.