2:1 MIPI D-PHY (1.5 Gbps) 4 Data Lane Switch

FSA634

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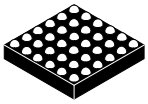

(Bottom View)

WLCSP36,
2.06x2.06x0.432
CASE 567XU

Description

The FSA634 is configured as a 4 data lane, MIPI D−PHY switch. This single pole double throw (SPDT) switch is optimized for switching between two high speed or low power MIPI sources. The FSA634 is designed for the MIPI specification and allows connection to a CSI or DSI module.

Features

- Switch Type: SPDT (10x)
- Signal Type: MIPI, D−PHY
- V_{CC}: 1.65 to 4.5 V
- Input Signal: 0 V to V_{CC}
- R_{ON}:
  - 5 Ω Typical HS MIPI
  - 5 Ω Typical LP MIPI
- ΔR_{ON}: 0.1 Ω Typical
- R_{ON_FLAT}: 0.06 Ω Typical
- I_{CCZ}: 0.5 μA Maximum
- I_{CC}: 32 μA Maximum
- O_{IRR}: −30 dB Typical
- Bandwidth: 1.9 GHz Typical
- Xtalk: −38 dB Typical
- C_{ON}: 4.3 pF Typical
- Skew: 3 ps Typical

Applications

- Cellular Phones, Smart Phones
- Tablets
- Laptops
- Displays

MARKING DIAGRAM

VJ = Specific Device Code
KK = Assembly Lot
X = Year
Y = Work Week
Z = Assembly Location

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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September, 2019 − Rev. 1

Publication Order Number:
FSA634/D

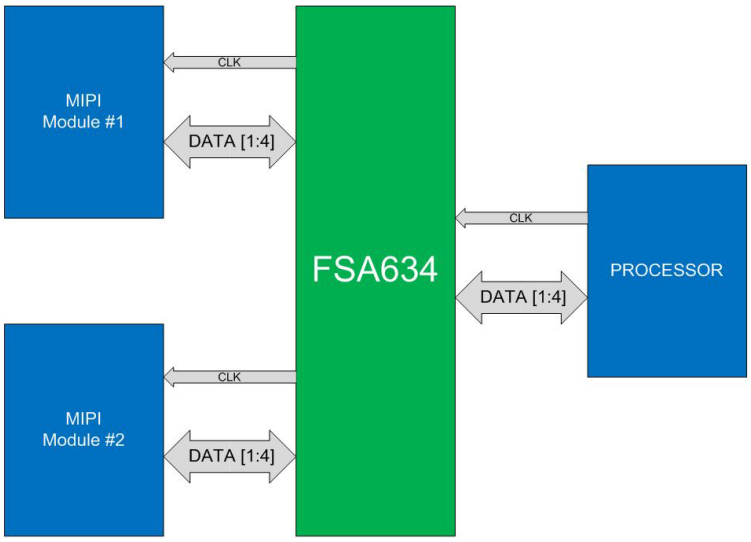
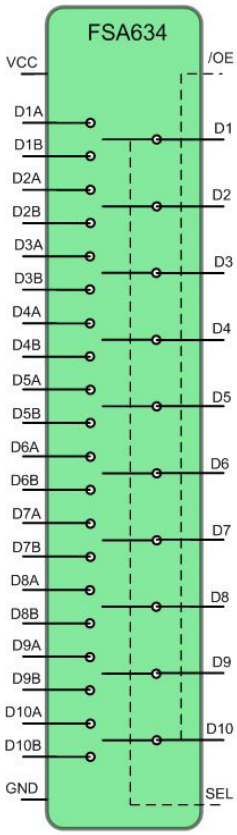


Figure 1. Typical Application

PIN DESCRIPTIONS



PIN NAME	DESCRIPTION		
Dn	Common Data Path		
DnA	Data Path A		
DnB	Data Path B		
/OE	Output Enable		
SEL	Control Pin	SEL=0	Dn = DnA
		SEL=1	Dn = DnB
VCC	Power		
GND	Ground		
NC	No Connect		

Figure 2. Analog Symbol

PIN DEFINITIONS

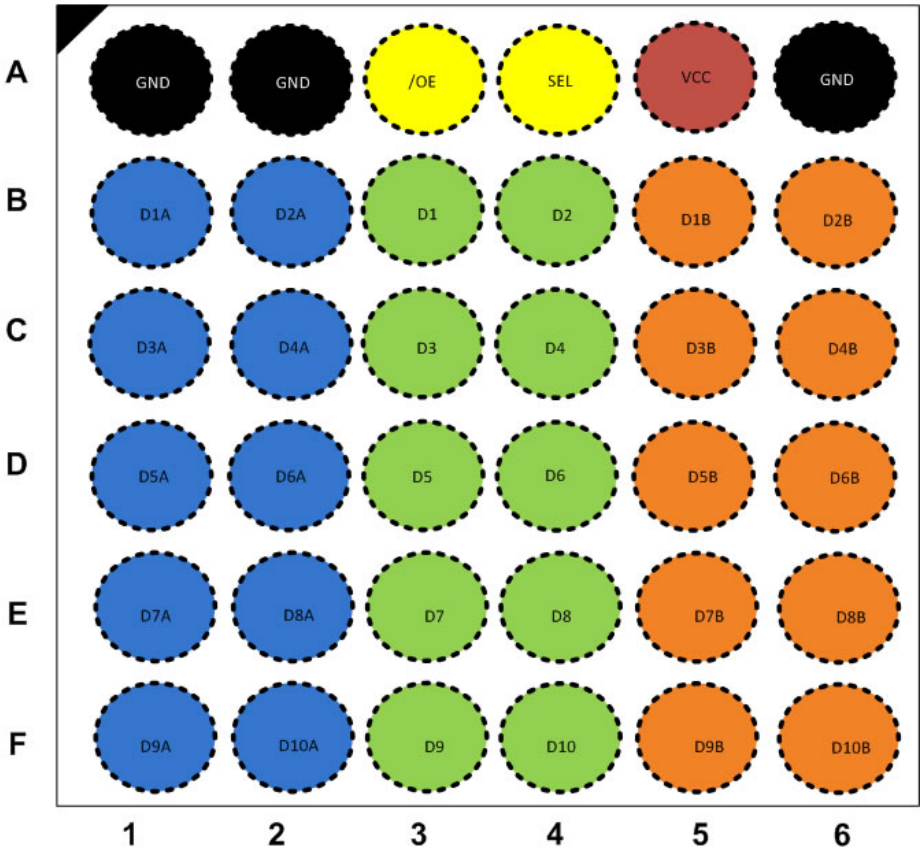


Figure 3. Top Through View

Table 1. BALL−TO−PIN MAPPINGS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A1	GND	C1	D3A	E1	D7A
A2	GND	C2	D4A	E2	D8A
A3	/OE	C3	D3	E3	D7
A4	SEL	C4	D4	E4	D8
A5	V_{CC}	C5	D3B	E5	D7B
A6	GND	C6	D4B	E6	D8B
B1	D1A	D1	D5A	F1	D9A
B2	D2A	D2	D6A	F2	D10A
B3	D1	D3	D5	F3	D9
B4	D2	D4	D6	F4	D10
B5	D1B	D5	D5B	F5	D9B
B6	D2B	D6	D6B	F6	D10B

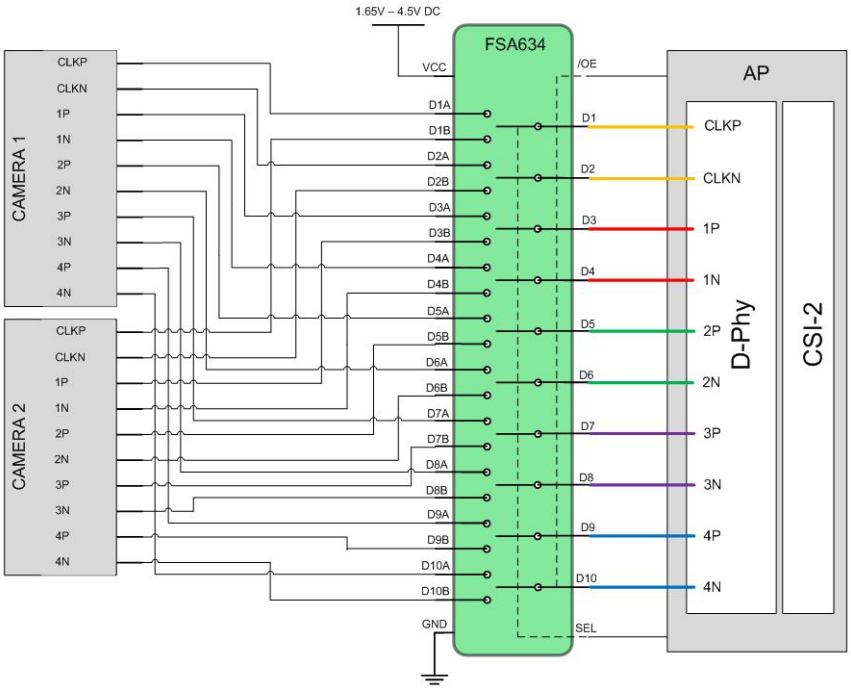


Figure 4. Suggested Configuration for 4 Lane D−PHY

TRUTH TABLE

SEL	/OE	Function
LOW	LOW	Dn = DnA
HIGH	LOW	Dn = DnB
X	HIGH	All Ports High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	5.25	V
V_{CNTRL}	DC Input Voltage (/OE, SEL) (Note 1)		−0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage (Note 1,2)		−0.3	V_{CC}	V
I_{IK}	DC Input Diode Current		−50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		−65	+150	°C
ESD	Human Body Model, JEDEC: JESD22−A114	All Pins	3.5		kV
	Charged Device Model, JEDEC: JESD22−C101		1.5		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		1.65	4.50	V
V_{CNTRL}	Control Input Voltage (SEL, /OE) (Note 3)		0	V_{CC}	V
V_{SW}	Switch I/O Voltage (Dn, DAn, DBn)	HS Mode	0	0.425	V
		LP Mode	0	1.3	V
T_A	Operating Temperature		−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The control inputs must be held HIGH or LOW; they must not float.

ELECTRICAL SPECIFICATION TABLE Typical values are at T_A = 25°C, V_{CC} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC ELECTRICAL PARAMETERS						
V_{IK}	Clamp Diode Voltage	I_{IN} = −18 mA, V_{CC} = 1.8 V			−1.2	V
V_{IH}	Input Voltage High	V_{CC} = 1.65 V to 4.50 V	1.0			V
V_{IL}	Input Voltage Low	V_{CC} = 1.65 V to 4.50 V			0.4	V
I_{IN}	Control Input Leakage (SEL,/OE)	V_{SW} = 0 V to V_{CC}, V_{CC} = 1.65 V to 4.50 V	−500		500	nA
$IN_{O(OFF)}$, $IN_{C(OFF)}$	Off Leakage Current of Port Dn, DnA, DnB	Dn = 0.3 V to V_{CC} − 0.3 V; DnA or DnB = Floating, 0.3 V, or V_{CC} − 0.3 V; /OE = 0 V; V_{CC} = 1.65 V to 4.5 V	−500		500	nA
$I_{A(ON)}$	On Leakage Current of Common Ports (Dn)	Dn = 0.3 V to V_{CC} − 0.3 V; DnA or DnB = Floating, 0.3 V, or V_{CC} − 0.3 V; /OE = 0 V; V_{CC} = 1.65 V to 4.5 V	−500		500	nA
I_{OFF}	Power−Off Leakage Current	Dn, DnA or DnB; V_{IN} = 0 V to 4.5 V; V_{CC} = 0 V	−500		500	nA
IOZ	Off−State Leakage	0 ≤ Dn, DnA, DnB ≤ 3.6 V, /OE = High, V_{CC} = 4.5 V	−500		500	nA
$R_{ON_MIPI_HS_1p8}$	Switch On Resistance for HS MIPI Applications (Note 5)	I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 1.8 V		5	12	Ω
$R_{ON_MIPI_HS_2p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 2.5 V		5	9	Ω
$R_{ON_MIPI_HS_3p6}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 3.6 V		5	9	Ω
$R_{ON_MIPI_HS_4p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 4.5 V		5	9	Ω
$R_{ON_MIPI_LP_1p8}$	Switch On Resistance for LP MIPI Applications (Note 5)	I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0 V, 0.6 V, 1.2 V, V_{CC} = 1.8 V		5	12	Ω
$R_{ON_MIPI_LP_2p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0 V, 0.6 V, 1.2 V, V_{CC} = 2.5 V		5	9	Ω
$R_{ON_MIPI_LP_3p6}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0 V, 0.6 V, 1.2 V, V_{CC} = 3.6 V		5	9	Ω
$R_{ON_MIPI_LP_4p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0 V, 0.6 V, 1.2 V V_{CC} = 4.5 V		5	9	Ω

ELECTRICAL SPECIFICATION TABLE Typical values are at T_A = 25°C, V_{CC} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC ELECTRICAL PARAMETERS						
$\Delta R_{ON_MIPI_HS_1p8}$	On Resistance Matching Between HS MIPI Channels	I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 1.8 V		0.10		Ω
$\Delta R_{ON_MIPI_HS_2p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 2.5 V		0.10		Ω
$\Delta R_{ON_MIPI_HS_3p6}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 3.6 V		0.10		Ω
$\Delta R_{ON_MIPI_HS_4p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 4.5 V		0.10		Ω
$\Delta R_{ON_MIPI_LP_1p8}$	On Resistance Matching Between LP MIPI Channels	I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 1.8 V		0.12		Ω
$\Delta R_{ON_MIPI_LP_2p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 2.5 V		0.12		Ω
$\Delta R_{ON_MIPI_LP_3p6}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 3.6 V		0.12		Ω
$\Delta R_{ON_MIPI_LP_4p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 4.5 V		0.12		Ω
$R_{ON_FLAT_MIPI_HS_1p8}$	On Resistance Flatness for HS MIPI Signals	I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 1.8 V		0.04		Ω
$R_{ON_FLAT_MIPI_HS_2p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 2.5 V		0.06		Ω
$R_{ON_FLAT_MIPI_HS_3p6}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 3.6 V		0.06		Ω
$R_{ON_FLAT_MIPI_HS_4p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.1 V, 0.2 V, 0.3 V, V_{CC} = 4.5 V		0.06		Ω
$R_{ON_FLAT_MIPI_LP_1p8}$	On Resistance Flatness for LP MIPI Signals	I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 1.8 V		0.18		Ω
$R_{ON_FLAT_MIPI_LP_2p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 2.5 V		0.28		Ω
$R_{ON_FLAT_MIPI_LP_3p6}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 3.6 V		0.28		Ω
$R_{ON_FLAT_MIPI_LP_4p5}$		I_{ON} = −10 mA, /OE = 0 V, SEL = V_{CC} or 0 V, DnA or DnB = 0.0 V, 0.6 V, 1.2 V, V_{CC} = 4.5 V		0.28		Ω
I_{CCZ}	Quiescent Hi−Z Supply Current	V_{IN} = 0 V or V_{CC}, I_{OUT} = 0 A, V_{CC} = 4.5 V			0.5	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 0 or V_{CC}, I_{OUT} = 0 A, V_{CC} = 2.5 V to 4.5 V		16	32	μA
I_{CC_1p8}		V_{IN} = 0 or V_{CC}, I_{OUT} = 0 A, V_{CC} = 1.8 V		15	25	μA
I_{CCT_4p5}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{SEL} = 1.65 V, /OE = 1.65 V, V_{CC} = 4.5 V			4	μA
I_{CCT_2p5}		V_{SEL} = 1.65 V, /OE = 1.65 V, V_{CC} = 2.5 V			0.1	μA
AC ELECTRICAL PARAMETERS						
t_{INIT}	Initialization Time V_{CC} to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 2.5 V to 4.5 V			100	μs
t_{INIT_1p8}		R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 1.8 V			150	μs
t_{EN}	Enable Turn−On Time, /OE to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 2.5 V to 4.5 V		120	200	ns
t_{EN_1p8}		R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 1.8 V		250	500	ns
t_{DIS}	Disable Turn−Off Time, /OE to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 2.5 V to 4.5 V		25	50	ns
t_{DIS_1p8}		R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 1.8 V		50	90	ns

ELECTRICAL SPECIFICATION TABLE Typical values are at T_A = 25°C, V_{CC} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AC ELECTRICAL PARAMETERS						
t_{ON}	Turn−On Time, SEL to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 2.5 V to 4.5 V, SEL = H to L, SEL = L to H			200	ns
t_{ON_1p8}		R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 1.8 V, SEL = H to L, SEL = L to H			300	ns
t_{OFF}	Turn−Off Time SEL to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 2.5 V to 4.5 V, SEL = H to L, SEL = L to H			200	ns
t_{OFF_1p8}		R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 1.8 V, SEL = H to L, SEL = L to H			300	
t_{BBM}	Break−Before−Make Time	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 1.2 V, V_{CC} = 1.65 V to 4.5 V	10	50		ns
OIRR	Off Isolation for MIPI (Note 5)	R_L = 50 Ω, f = 750 MHz, /OE = V_{CC}, V_{SW} = −1 dBm (200 mV_{PP}), V_{CC} = 1.65 V to 4.5 V		−30		dB
XTALK	Crosstalk for MIPI (Note 5)	R_L = 50 Ω, f = 750 MHz, V_{SW} = −1 dBm (200 mV_{PP}), V_{CC} = 1.65 V to 4.5 V		−38		dB
BW	Bandwidth at −3dB (Note 5)	R_L = 50 Ω, C_L = 0 pF, V_{CC} = 3 V		1.9		GHz
$t_{SK(O)}$	Channel−to−Channel Single−Ended Skew (Note 5)	TDR−Based Method (V_{SW} = 0.2 V_{PP}, C_L = C_{ON}), V_{CC} = 3.3 V		3	20	ps
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (Note 5)	TDR−Based Method (V_{SW} = 0.2 V_{PP}, C_L = C_{ON}), V_{CC} = 3.3 V		3	20	ps
CAPACITANCE						
C_{IN}	Control Pin Input Capacitance (Note 5)	V_{CC} = 0 V, f = 1 MHz		2.7		pF
C_{ON}	Out On Capacitance (Note 5)	V_{CC} = 3.3 V, /OE = 0 V, f = 1 MHz		4.3		pF
C_{OFF}	Out Off Capacitance (Note 5)	V_{CC} and /OE = 3.3 V, f = 1 MHz		1.9		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Guarantee Levels:

4. Guaranteed by Design. Characterized on the ATE or Bench.
5. Guaranteed by Design and Characterization, not Production Tested.

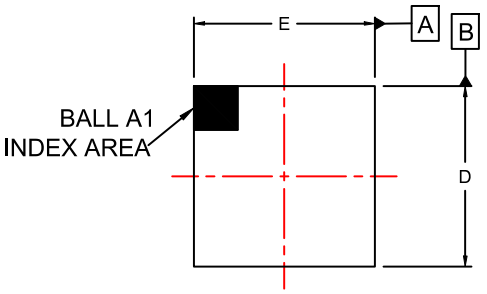
The table below pertains to the Packaging information on the following page.

ORDERING INFORMATION

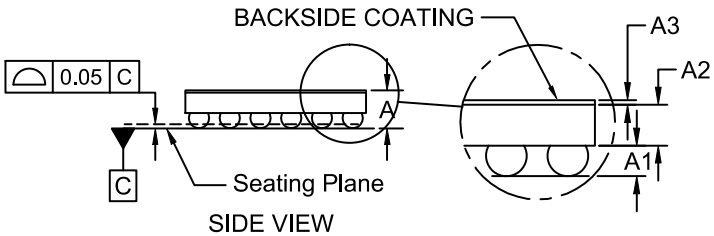
Part Number	Operating Temperature Range	Package	Top Mark
FSA634UCX	−40 to +85°C	36−Ball WLCSP, Non−JEDEC 2.06 x 2.06 mm, 0.35 mm Pitch	VJ

WLCSP36 2.06x2.06x0.432
CASE 567XU
ISSUE O

DATE 26 APR 2019



TOP VIEW



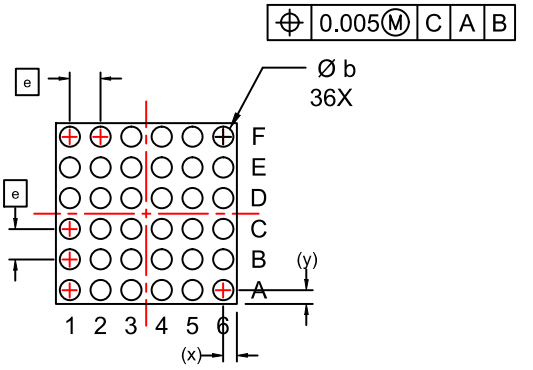
SIDE VIEW

DETAIL A

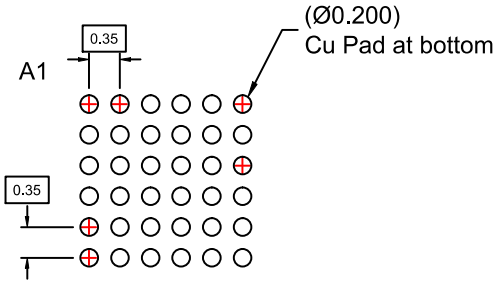
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.391	0.432	0.473
A1	0.154	0.174	0.194
A2	0.215	0.233	0.251
A3	0.022	0.025	0.028
b	0.211	0.231	0.251
D	2.03	2.06	2.09
E	2.03	2.06	2.09
e	0.35 BSC		
x	0.140	0.155	0.170
y	0.140	0.155	0.170



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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